

Semiconductors and integrated circuits

Part 5b March 1977

Consumer ICs

SEMICONDUCTORS AND INTEGRATED CIRCUITS

Part 5b

March 1977

General

Radio - Audio

Television

Index and maintenance type list

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of three series of handbooks each comprising several parts.

ELECTRON TUBES

BLUE

SEMICONDUCTORS AND INTEGRATED CIRCUITS

RED

COMPONENTS AND MATERIALS

GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

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ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a	Transmitting tubes for communication Tubes for r.f. heating Types PE05/25 – TBW15/25	December 1975
Part 1b	Transmitting tubes for communication Tubes for r.f. heating Amplifier circuit assemblies	January 1976
Part 2	Microwave products Communication magnetrons Magnetrons for microwave heating Klystrons Travelling-wave tubes Isolators, Circulators	May 1976
Part 3	Special Quality tubes Miscellaneous devices	January 1975
Part 4	Receiving tubes	March 1975
Part 5a	Cathode-ray tubes	August 1976
Part 5b	Camera tubes Image intensifier tubes	May 1975
Part 6	Products for nuclear technology Channel electron multipliers Neutron tubes	January 1977
Part 7a	Gas-filled tubes Thyratrons Industrial rectifying tubes	March 1977
Part 7b	Gas-filled tubes Segment indicator tubes Indicator tubes	March 1977
Part 8	TV picture tubes	October 1975
Part 9	Photomultiplier tubes Phototubes (diodes)	June 1976

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a	Rectifier diodes, thyristors, triacs		March 1976
	Rectifier diodes	Rectifier stacks	
	Voltage regulator diodes (> 1,5 W)	Thyristors	
	Transient suppressor diodes	Triacs	
Part 1b	Diodes		October 1975
	Small signal germanium diodes	Voltage regulator diodes (< 1,5 W)	
	Small signal silicon diodes	Voltage reference diodes	
	Special diodes	Tuner diodes	
Part 2	Low-frequency transistors		December 1975
Part 3	High-frequency and switching transistors		April 1976
Part 4a	Special semiconductors		June 1976
	Transmitting transistors	Dual transistors	
	Microwave devices	Microminiature devices for	
	Field-effect transistors	thick- and thin-film circuits	
Part 4b	Devices for optoelectronics		July 1976
	Photosensitive diodes and transistors	Photocouplers	
	Light emitting diodes	Infrared sensitive devices	
	Displays	Photoconductive devices	
Part 5a	Professional analogue integrated circuits		November 1976
Part 5b	Consumer integrated circuits		March 1977
	Radio - Audio		
	Television		
Part 6	Digital integrated circuits		May 1976
	LOC MOS HE family		
	GZ family		

COMPONENTS AND MATERIALS (GREEN SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1	Functional units, Input/output devices, Peripheral devices		November 1975
	High noise immunity logic FZ/30-Series	Circuit blocks 90-Series	
	Circuit blocks 40-Series and CSA70	Input/output devices	
	Counter modules 50-Series	Hybrid integrated circuits	
	NORbits 60-Series, 61-Series	Peripheral devices	
Part 2a	Resistors		February 1976
	Fixed resistors	Negative temperature coefficient thermistors (NTC)	
	Variable resistors	Positive temperature coefficient thermistors (PTC)	
	Voltage dependent resistors (VDR)	Test switches	
	Light dependent resistors (LDR)		
Part 2b	Capacitors		April 1976
	Electrolytic and solid capacitors	Ceramic capacitors	
	Paper capacitors and film capacitors	Variable capacitors	
Part 3	Radio, Audio, Television		January 1977
	FM tuners	Components for black and white television	
	Loudspeakers	Components for colour television	
	Television tuners and aerial input assemblies		
Part 4a	Soft ferrites		October 1976
	Ferrites for radio, audio and television	Ferroxcube potcores and square cores	
	Beads and chokes	Ferroxcube transformer cores	
Part 4b	Piezoelectric ceramics, Permanent magnet materials		December 1976
Part 5	Ferrite core memory products		July 1975
	Ferroxcube memory cores	Core memory systems	
	Matrix planes and stacks		
Part 6	Electric motors and accessories		September 1975
	Small synchronous motors	Miniature direct current motors	
	Stepper motors		
Part 7	Circuit blocks		September 1971
	Circuit blocks 100 kHz-Series	Circuit blocks for ferrite core memory drive	
	Circuit blocks 1-Series		
	Circuit blocks 10-Series		
Part 8	Variable mains transformers		February 1977
Part 9	Piezoelectric quartz devices		March 1976
Part 10	Connectors		November 1975

General

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PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.

The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.

Values cited as typical are given for information only.

For an explanation of the type designation code, see the section Type Designation. For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.

If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.

Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.

Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.

Dual in-line packages have a notch at one end to identify pin 1.

Take care not to mistake adventitious moulding marks for the pin 1 identification. Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.

Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE

The type number consists of three letters followed by a four digit serial number (sometimes augmented by a version letter).

First two letters:

Family circuits

The first two letters identify the family.

Solitary circuits

The first letter identifies the circuit as:

S-digital

T-analogue

U-mixed analogue/digital

The second letter has no special significance.

The third letter indicates the operating ambient temperature range or another significant characteristic. Letters B to F stand for the following temperature ranges: ¹⁾

B: 0 to +70 °C

C: -55 to +125 °C

D: -25 to +70 °C

E: -25 to +85 °C

F: -40 to +85 °C

When no temperature range is specified, the third letter is A. Other third letters identify special family versions or treatments (e.g. radiation hardened).

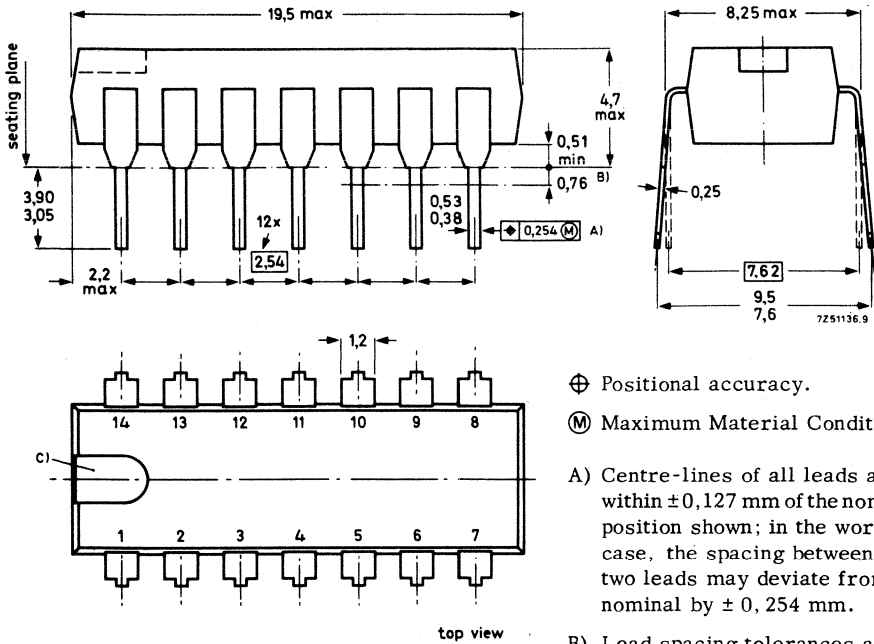
The serial number following the three letters may be either a 4-digit number or a proprietary type designation comprising a combination of letters and digits. Proprietary type designations consisting of less than 4 characters are extended to 4 by putting zeros (0) before them.

¹⁾ If a circuit is published for a wider temperature range, but does not qualify for another classification, the letter designating the nearest narrower temperature range is used.

Package outlines



14-LEAD DUAL IN-LINE; PLASTIC (SOT-27)



Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

⊕ Positional accuracy.

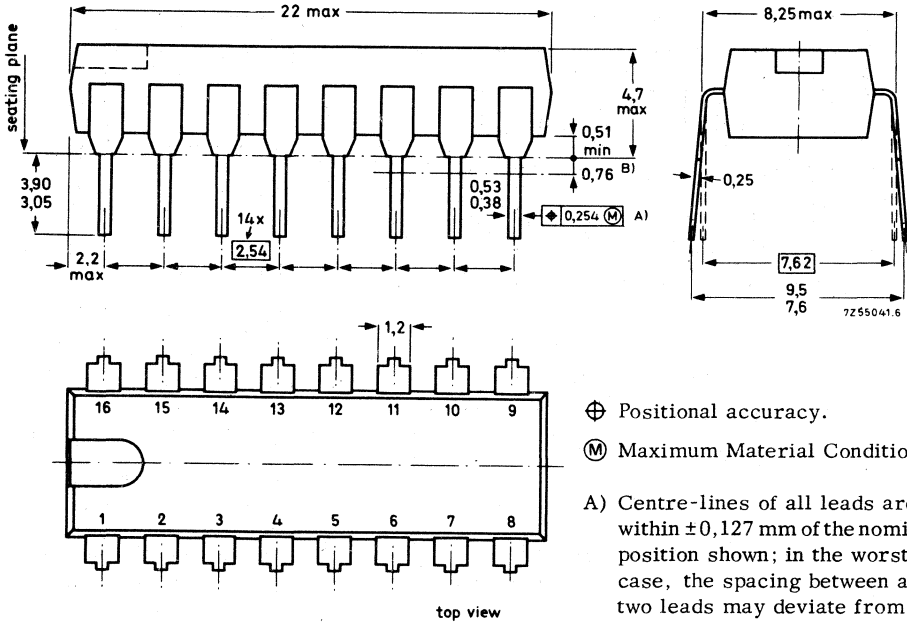
Ⓜ Maximum Material Condition.

A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

C) Index may be horizontal as shown, or vertical.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

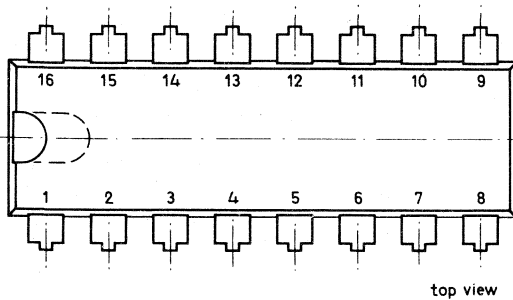
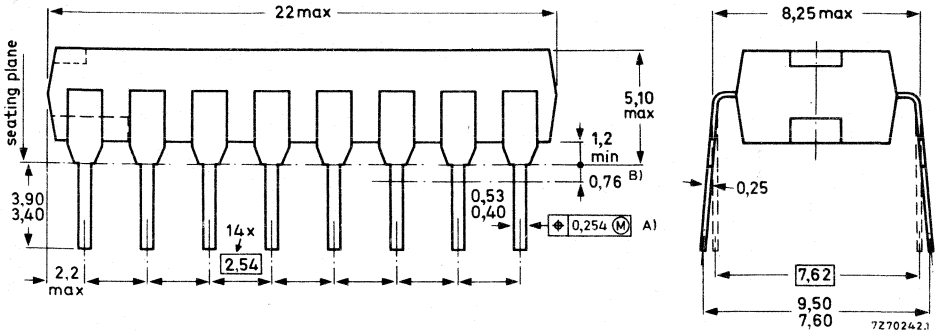
260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-38M and N)



- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

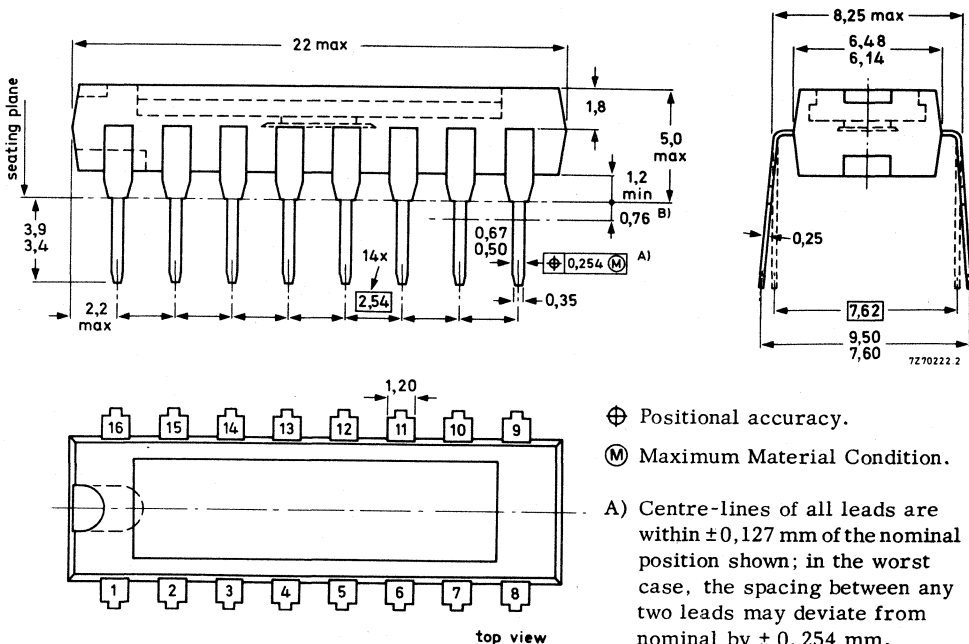
260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-69B)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

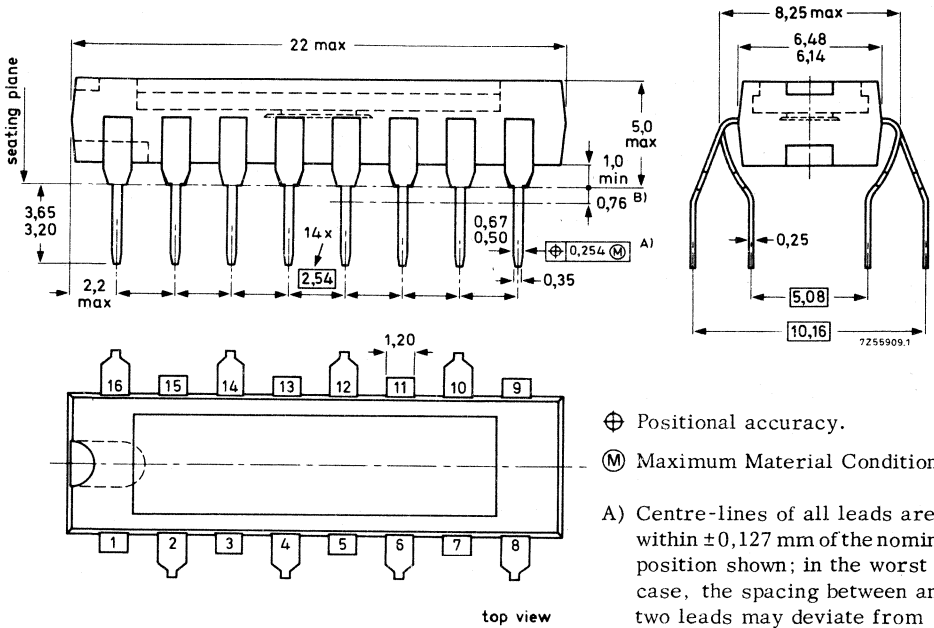
260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD QUADRUPLE IN-LINE; PLASTIC POWER (SOT-76B)



Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

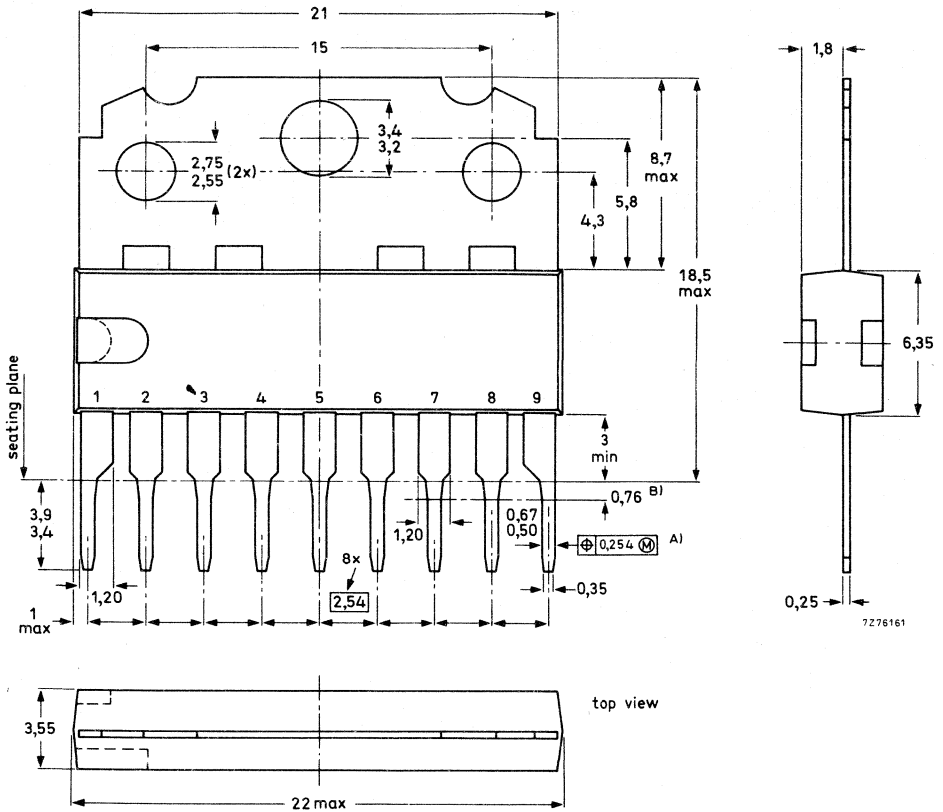
260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110A)



Dimensions in mm

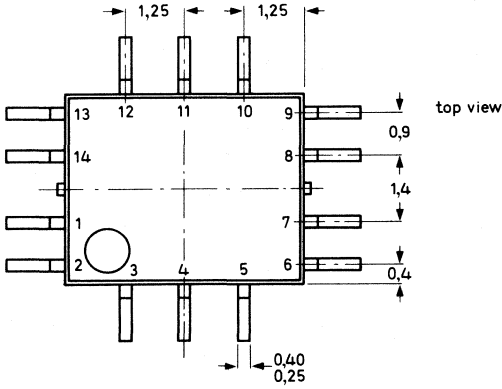
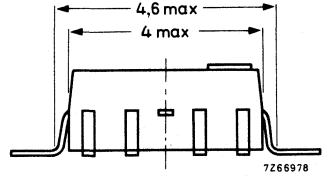
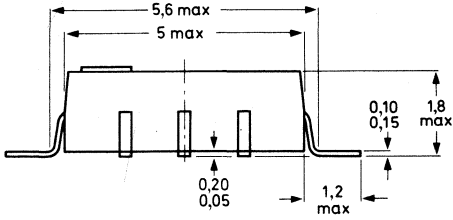
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

14-LEAD; PLASTIC (SOT-43)



Dimensions in mm

RATING SYSTEMS

ACCORDING TO I.E.C. PUBLICATION 134

1. DEFINITIONS OF TERMS USED

1.1 Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

1.2 Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

1.3 Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

1.4 Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

1.5 Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

2. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

p. t. o.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

3. DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

4. DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

NOTE

It is common use to apply the Absolute Maximum System in semiconductor published data.

LETTER SYMBOLS FOR LINEAR INTEGRATED CIRCUITS

General

The voltages and currents are normally related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a number. In appropriate cases voltages, currents etc. pertinent to one or more of the circuit elements (transistors, diodes) are given in which case symbols are based on the recommendations as published in I.E.C. Publication 148.

Quantity symbols

1. Instantaneous values of current, voltage and power, which vary with time are represented by the appropriate lower case letter.

Examples: i , v , p

2. Maximum (peak), average, d.c. and root-mean-square values are represented by the appropriate upper case letter.

Examples: I , V , P

Polarity of current and voltage

A current is defined to be positive when its conventional direction of flow is into the device.

A voltage is measured with respect to the reference terminal, which is indicated by the subscripts. Its polarity is defined to be positive when the potential is higher than that of the reference terminal.

Subscripts

For currents the number behind the quantity symbol indicates the terminal carrying the current.

Examples: I_2 , i_{14}

For voltages normally two number subscripts are used, connected by a hyphen. The first number indicates the terminal at which the voltage is measured and the second subscript the reference terminal.

Where there is no possibility of confusion the second subscript may be omitted.

Examples: V_{2-12} , v_{14-2} , V_5 , v_8

To distinguish between maximum (peak), average, d.c. and root-mean-square values the following subscripts are added:

For maximum (peak) values : M or m
For average values : AV or av
For root-mean-square values: (RMS) or (rms)
For d.c. values : no additional subscripts

The upper case subscripts indicate total values.

The lower case subscripts indicate values of varying components:

Examples: I_2 , I_{2AV} , $I_{2(rms)}$, $I_{2(RMS)}$

In appropriate cases quantity symbols are pertinent to single elements of a circuit (transistors or diodes), the normal subscripts for semiconductor devices can be used.

Examples: V_{CBO} , V_{be} , V_{CES} , I_C
 V_{DSS} , V_{GS} , I_D

List of subscripts:

E, e = Emitter terminal
B, b = Base terminal for bipolar transistors,
Substrate for MOS devices
C, c = Collector terminal
D, d = Drain terminal
G, g = Gate terminal
S, s = Source terminal for MOS devices
Substrate for bipolar transistor circuits
(BR) = Break-down
M, m = Maximum (peak) value
AV, av = Average value
(RMS), (rms) = R.M.S. value

Electrical Parameter Symbols

1. The values of four pole matrix parameters or other resistances, impedances, admittances, etc., inherent in the device, are represented by the lower case symbol with appropriate subscript.

Examples: h_i , z_f , y_o , k_r

Subscripts for Parameter Symbols

1. The static values of parameters are indicated by upper case subscripts.

Examples: h_{FE} , h_I

2. The small signal values of parameters are indicated by lower case subscripts.

Examples: h_i , z_o

3. The first subscript, in matrix notation identifies the element of the four pole matrix.

i (for 11) = input
o (for 22) = output
f (for 21) = forward transfer
r (for 12) = reverse transfer

$$\text{Examples: } V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

The voltage and current symbols in matrix notation are indicated by a single digit subscript.

The subscript 1 = input; the subscript 2 = output.

The voltages and currents in these equations may be complex quantities.

4. A second subscript is used only for separate circuit elements (e.g. transistors) to identify the circuit configuration:

e = common emitter
b = common base
c = common collector

5. If it is necessary to distinguish between real and imaginary parts of the four pole parameters, the following notation may be used:

$R_e(h_i)$ etc. ... for the real part
 $I_m(h_i)$ etc. ... for the imaginary part

LIST OF LETTER SYMBOLS IN ALPHABETICAL ORDER

Letter symbol	Definition
B	Bandwidth
b_i, b_o	Input, respectively output susceptance
C_i, C_o	Input, respectively output capacitance
CMMR	Common-mode rejection ratio
d	Distortion
F	Noise figure
f	Frequency
f_c	Cut-off frequency
f_o	Centre frequency, intermediate frequency
f_m	Modulation frequency
f_T	Transition frequency
g_i, g_o	Input, respectively output conductance
G_p	Power gain
G_{tr}	Transducer gain
G_v	Voltage gain
$h_F, h_{FB}, h_{FC}, h_{FE}$	DC current gain (output voltage held constant)
$h_f, h_{fb}, h_{fc}, h_{fe}$	Small signal current gain (output short-circuited to a.c.)
$I_3, I_B, I_C, I_E, I_D, I_Q, I_S$	Total d.c. current
$i_3, i_B, i_C, i_E, i_D, i_G, i_S$	Instantaneous total value of the current
$I_{3AV}, I_{BAV}, I_{CAV}, I_{EAV}$	Total average current
$I_{3M}, I_{BM}, I_{CM}, I_{EM}$	Maximum (peak) value of the total current
$I_{3m}, I_{bm}, I_{cm}, I_{em}$	Maximum (peak) value of the varying component of the current
I_{CBO}	Collector cut-off current (open emitter)
I_{CS}	Collector-substrate leakage current
I_{DSS}	Drain cut-off current (source short-circuited to gate)

Letter symbol	Definition
I_{EBO}	Emitter cut-off current
I_I, I_i	Input current of a specified circuit
I_{io}	Input offset current
I_O, I_o	Output current of a specified circuit
I_{OM}	Peak value of output current
$I_{O(p-p)}$	Peak to peak value of output current
I_{tot}	Total supply current
K_f	Small signal voltage gain
K_o	Output impedance (see K parameters)
K_r	Reverse current transfer ratio
M	Modulation depth
P_i, P_o	Input, respectively output power of a specified circuit
P_{tot}	Total power dissipation in the device
R_i, R_o	Input, respectively output resistance of a specified circuit
R_L	Load resistance
R_S	Source resistance
R_{th}	Thermal resistance
SVRR	Supply voltage rejection ratio
T_{amb}	Ambient temperature
T_{case}	Case temperature
T_{stg}	Storage temperature
$V_3, V_{3-4}, V_{BE}, V_{CB}$	Total value of the voltage (d.c.)
$v_3, v_{3-4}, v_{BE}, v_{CB}$	Instantaneous value of the total voltage
V_{BEsat}, V_{CEsat}	Saturation voltage at specified bottoming conditions
$V_{(BR)CBO}, V_{(BR)CEO}, V_{(BR)EBO}$	Breakdown voltage between the terminal of the first subscript and the reference terminal (second subscript) when the third terminal is open circuited
$V_{(BR)CS}$	Collector to substrate breakdown voltage
$V_{CBO}, V_{CEO}, V_{EBO}, V_{CS}, V_{1-3}$	Voltage of the terminal indicated with respect to the reference terminal (second subscript)

LETTER SYMBOLS

Letter symbol	Definition
V_i, V_o	Input, respectively output voltage of a specified circuit
V_{io}	Input offset voltage
$V_{i \text{ lim}}$	Input voltage at which limiting starts
V_N	Negative supply voltage
V_P	Positive supply voltage
V_n	Noise voltage
Y_i, Y_f, Y_o, Y_r	Input, transfer, output and feedback admittance
Z_i, Z_o	Input, respectively output impedance
η	Efficiency
$\varphi_i, \varphi_f, \varphi_o, \varphi_r$	Phase angle of input, transfer, output and feedback admittance

Radio - Audio



TYPE SELECTION

	hi-fi equipment	portables radios and radio/recorders	car radios	mains radios
a.m. channel receivers	TBA570A	TBA570A TBA700	TBA570A	TBA570A
f.m. channel receivers	TCA420A	TBA570A	TBA570A TCA420A	TBA570A
a.m./f.m. receiver circuits		TBA570A TBA700	TBA570A	TBA570A
Stereo decoders	TDA1005 TCA290A		TDA1005	
Stabilizer for electronic tuning	TCA530 TCA750			
d.c. controlled audio circuits	volume and balance	TCA730		TCA730
	tone	TCA740		TCA740
	quadruple signal- sources switch	TDA1028		
	stereo signal- sources switch	TDA1029		
a.f. power amplifiers	2 W audio amplifier		TCA760B	
	5 W audio power amplifier		TDA2611; TDA2611A	
	6 W audio power amplifier		TDA1010	
	10 W audio power amplifier (with thermal shut-down)		TDA1004A	
	stereo audio power amplifier up to 2 x 6 W		TDA1009	
Miscellaneous	hearing aid amplifier		OM200/S2	
	hearing aid amplifier		TAA370A	
	low level amplifier		TAA263	
	integrated MOST amplifier		TAA320	
	integrated MOST level sensor		TAA320A	
	recording preamplifier circuit		TDA1002	
	motor regulator and bias/erase oscillator circuit		TDA1003A	
	motor regulator with automatic tape-end indicator		TDA1006	
	bipolar frequency divider		SAJ110	
	magnetic field detector using Hall effect		TCA450A	

INTEGRATED AMPLIFIER for use in ear hearing aids

Monolithic integrated circuit amplifier in a plastic envelope, primarily intended for use in ear hearing aids.

QUICK REFERENCE DATA

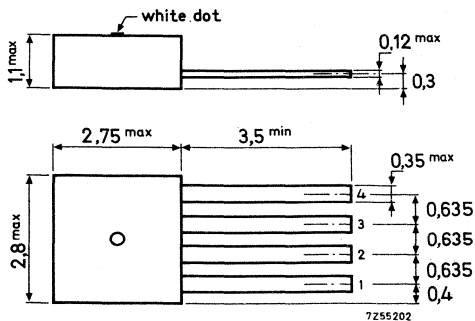
For meaning of symbols see test circuit on page 3

Supply voltage	V_{1-3}	max.	5 V
Supply current	I_2	max.	5 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	25 mW

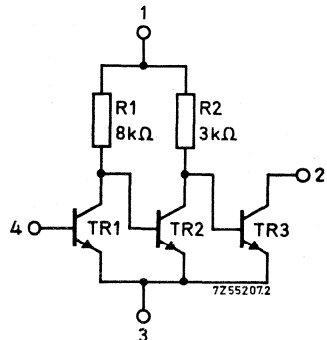
The following data are measured in test circuit on page 3

Total supply current	I_{tot}	typ.	1 mA
Transducer gain	G_{tr}	>	77 dB
		typ.	85 dB
Output power at $d_{tot} = 10\%$	P_o	>	0,2 mW
Cut-off frequency (-3 dB)	f_c	>	20 kHz

PACKAGE OUTLINE (Dimensions in mm)



CIRCUIT DIAGRAM



The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

For meaning of symbols test circuit on page 3.

Voltages

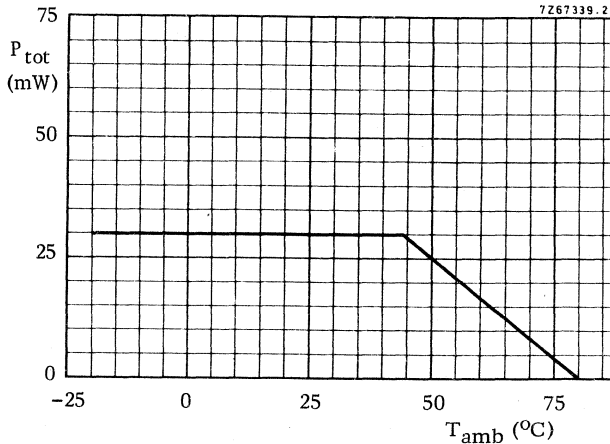
Supply voltage	V_{1-3}	max.	5 V
Output voltage	V_{2-3}	max.	5 V ¹⁾
Input voltage	$-V_{4-3}$	max.	5 V

Currents

Output current	I_2	max.	5 mA
Input current	I_4	max.	5 mA

Power dissipation

Power derating curve



Temperatures

Storage temperature	T_{stg}	-20 to +80 °C
Ambient temperature (see derating curve above)	T_{amb}	-20 to +80 °C

1) This value may be exceeded during inductive switch-off for transient energies < 10µWs.

CHARACTERISTICS at $V_{1-3} = 1,3 \text{ V}$; $I_2 = 0,7 \text{ mA}$ and $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified

Supply currents (no signal)

I_{tot}	<	1,1	mA
I_{J}	typ.	0,30	mA

Transducer gain at $f = 1 \text{ kHz}$

G_{tr}	>	77	dB	1)
	typ.	85	dB	

Total distortion at $f = 1 \text{ kHz}$

$P_o = 100 \text{ } \mu\text{W}$

d_{tot}	typ.	4	%
	<	6	%

$P_o = 200 \text{ } \mu\text{W}$

d_{tot}	<	10	%
------------------	---	----	---

Noise figure at $R_S = 5 \text{ k}\Omega$

$B = 400 \text{ to } 3200 \text{ Hz}$

F	typ.	2,5	dB	
	<	6	dB	2)

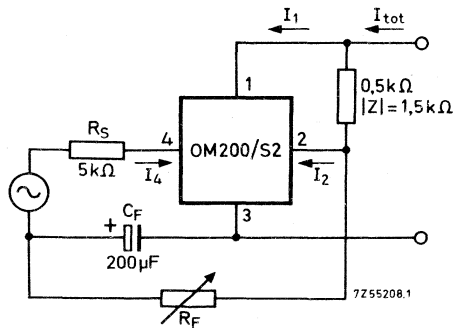
Cut-off frequency (-3 dB)

f_c	>	20	kHz
-------	---	----	-----

Value of R_F to adjust I_2 at $0,7 \text{ mA}$

R_F	170 to 1000	$\text{k}\Omega$
	typ.	400 $\text{k}\Omega$

Test circuit



Note

$I_2 = 0,7 \text{ mA}$; adjusted by means of R_F
 $V_{1-3} = 1,3 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

1) The transducer gain is defined as the ratio of the output power in the load $|Z| = 1,5 \text{ k}\Omega$ and the available input power of the source with $R_S = 5 \text{ k}\Omega$.

$$G_{\text{tr}} = \frac{P_o}{V_i^2 / 4 R_S}$$

2) Due to special processing and pre-measuring, the flutter-noise level is extremely low.

SOLDERING RECOMMENDATIONS

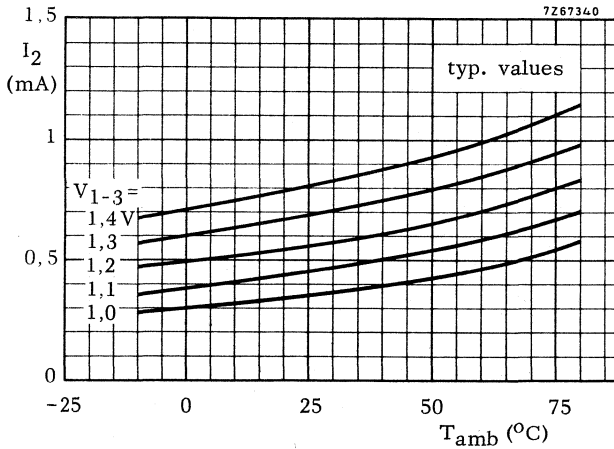
1. Iron soldering

At a maximum iron temperature of 300 °C the maximum permissible soldering time is 3 seconds, provided the solder spot is at least 0,5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

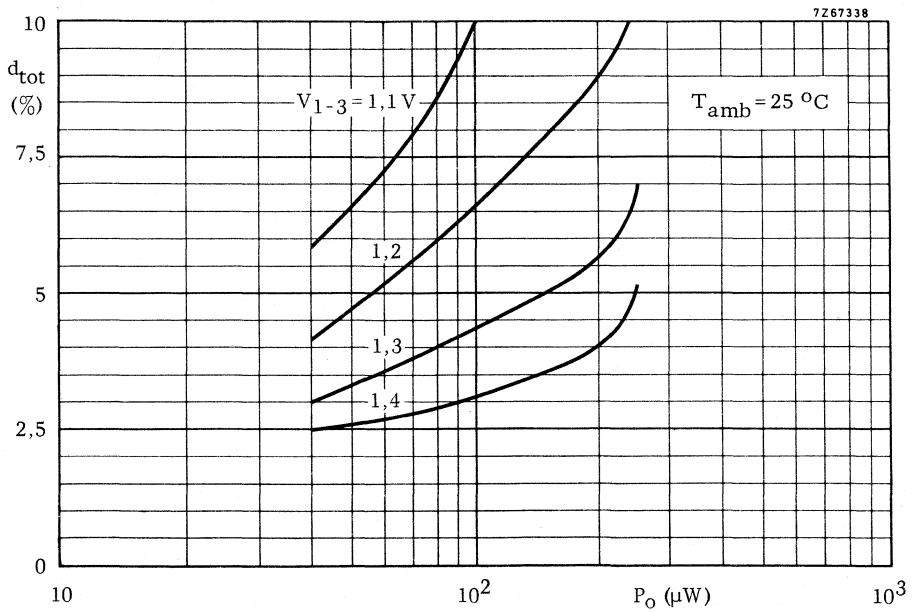
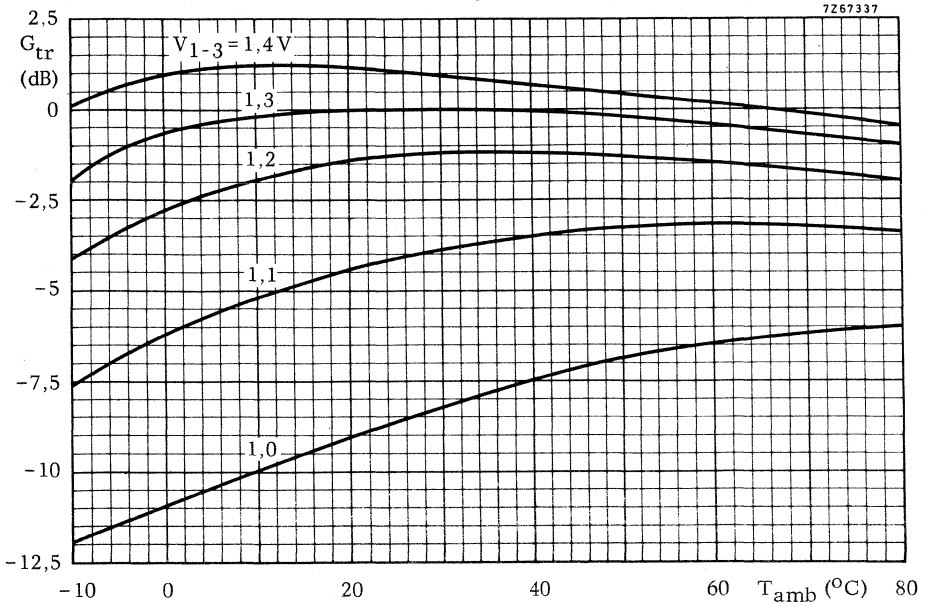
2. Dipsoldering

At a maximum solder temperature of 250 °C the maximum permissible soldering time is 3 seconds, provided the soldered spot is at least 0,5 mm from the seal.

CHARACTERISTICS



The graph applies to test circuit on page 3



BI-POLAR FREQUENCY DIVIDER

The SAJ110 is a monolithic integrated circuit in bipolar technique, consisting of 7 binary frequency dividers separated in groups of 2, 2, 1, 1 and 1, each section having its own trigger input.

The circuit consists of a d.c. flip-flop and can accept any input waveform, making the device particularly suitable for use in electronic organs. The output impedance is low and there is excellent separation between adjacent stages.

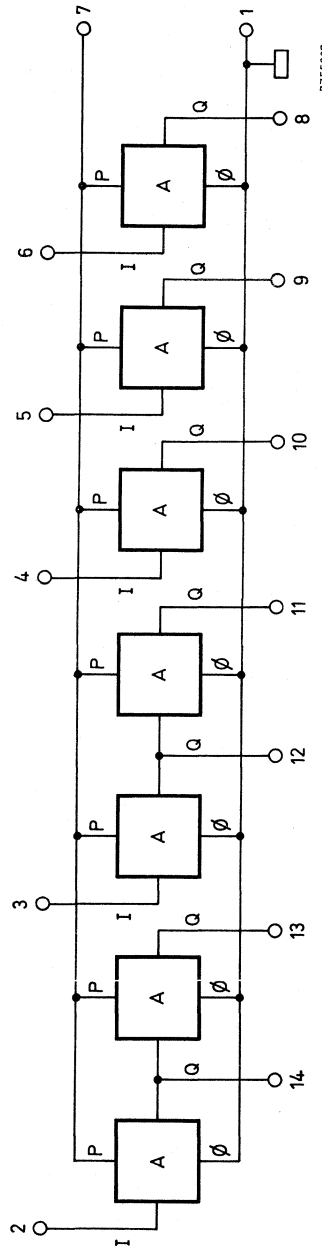
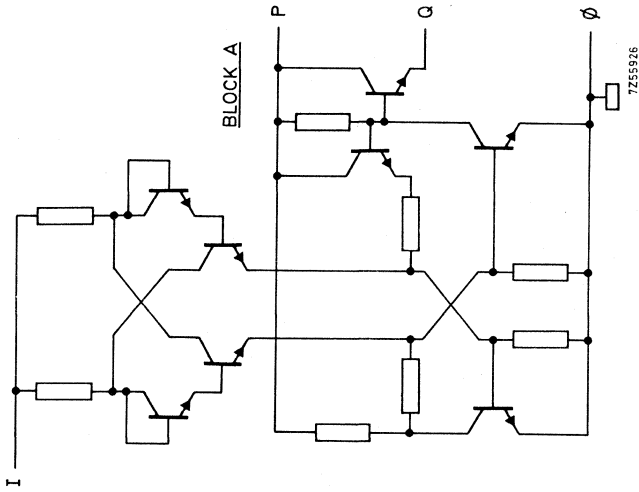
QUICK REFERENCE DATA				
Supply voltage	$V_{7-1} = V_P$	nom.	9	V
Ambient temperature	T_{amb}	nom.	25	°C

Input voltage levels	$\left\{ \begin{array}{l} V_{IL} \\ V_{IH} \end{array} \right.$	\leq	1	V
		\geq	6	V
		\leq	V_{7-1}	
Output voltage levels	$\left\{ \begin{array}{l} V_{OL} \\ V_{OH} \end{array} \right.$	\leq	0,1	V
		\geq	7,3	V
Output impedance (V_O in HIGH state)	$ Z_O $	typ.	120	Ω
Total power dissipation every output loaded with $R_L = 2,2 \text{ k}\Omega$	P_{tot}	typ.	200	mW

PACKAGE OUTLINE (see general section)

14-lead DIL; plastic.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Pin No. 2; 3; 4; 5; 6 voltage with respect to pin No. 1 (substrate)

$|V_I|$ max. V_{7-1} ¹⁾

Pin No. 7 (supply voltage)

$V_{7-1} = V_P$ 0 to +11 V

Pin No. 8; 9; 10; 11; 12; 13; 14 voltage

V_O 0 to +5 V

All other pins connected to pin No. 1 (substrate)

Temperature

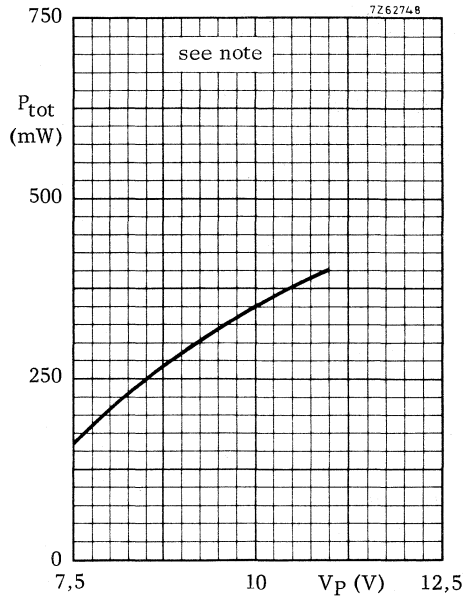
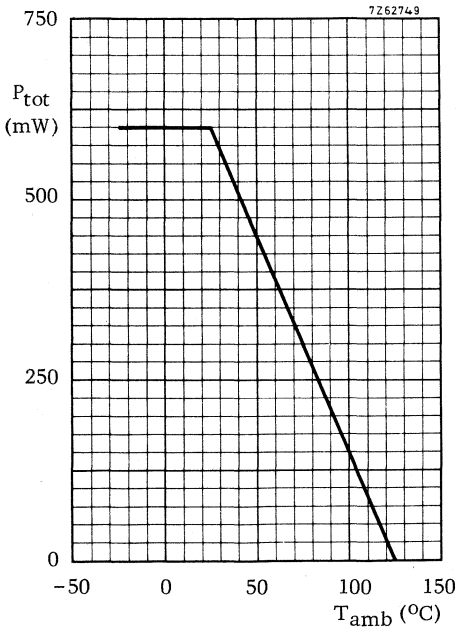
Storage temperature

T_{stg} -55 to +125 °C

Operating ambient temperature
(see derating curve below)

T_{amb} -25 to +125 °C

Total power dissipation



Note Power dissipation when all flip-flop outputs are operating at maximum dissipation (extreme condition). In organ practice the average power dissipation is less because the master oscillators cause the flip-flops to switch continuously.

¹⁾ Negative going input signals cause some distortion in the output pulse so that an optimal application using only positive going input signals as advised.

CHARACTERISTICS

Supply voltage $V_{7-1} = V_P$ 7, 5 to 11 V
typ. 9 V

CHARACTERISTICS at $V_P = 9$ V; $T_{amb} = 25$ °C; $R_L = 2,2$ k Ω (see Fig. 1 on page 5).

<u>Input voltage levels</u>	V_{IL}	\leq	1	V	1)
	V_{IH}		6 to V_P	V	1)
<u>Output voltage levels</u>	V_{OL}	\leq	0,1	V	2)
	V_{OH}	\geq	7,3	V	2)
<u>Change-over time</u>	t_c	\leq	0,2	μ s	3)
<u>Dynamic input impedance</u>	$ Z_i $	typ.	8	k Ω	4)
<u>Output impedance</u> (V_O in HIGH state)	$ Z_o $	typ.	120	Ω	
<u>Total power dissipation</u>	P_{tot}	typ.	200	mW	5)
<u>Supply current per divider</u>	I_7	\leq	3	mA	6)
<u>Output current</u> (per stage)	I_o	\leq	5	mA	7)
<u>Frequency range</u> (input)	f_I		20 Hz to 20	kHz	8)
<u>Resetting of divider at :</u>	I_o	typ.	50	mA	9)

1) See also Fig. 2 on page 5 and Fig. 4 on page 6.

2) See also Fig. 3 on page 5, Fig. 5 and Fig. 6 on page 6.

3) See also Fig. 3 on page 5.

4) See also Fig. 7 on page 6.

5) Typical value under condition that all flip-flop outputs are operating at max. dissipation.

6) Measured when output stage is in LOW state.

7) Occasional short circuiting pins 8, 9, 10, 11, 12, 13 and 14 is allowed; the output currents are internally limited to about 100 mA.

8) This range is based on requirements for applications in organs; in practice the frequency range is much larger (from d.c. to about 1 MHz).

9) Input voltage must be in LOW state.

CHARACTERISTICS (continued)

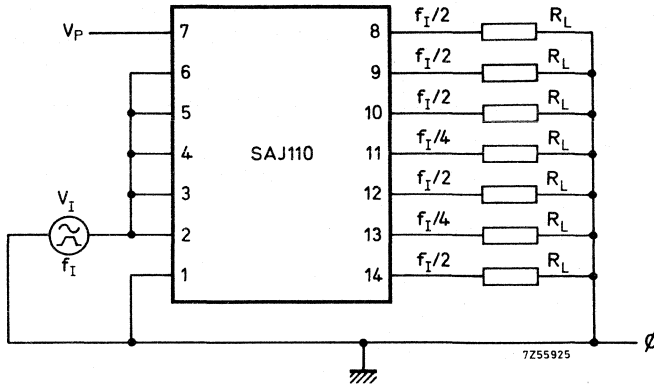


Fig. 1 Test circuit

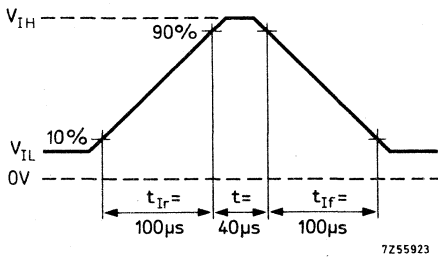


Fig. 2 Input voltage: V_I

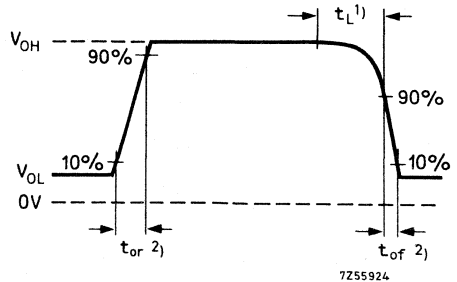
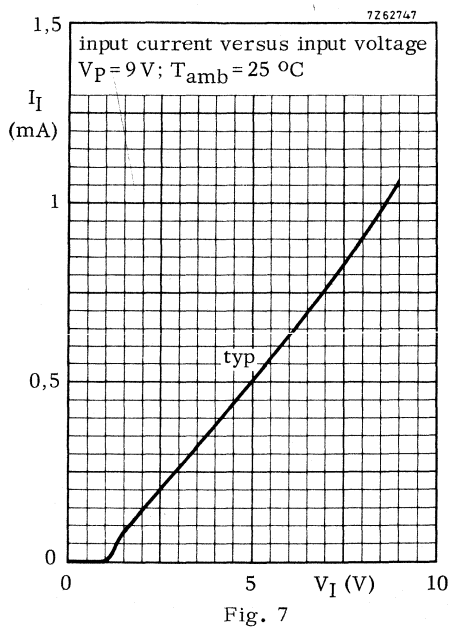
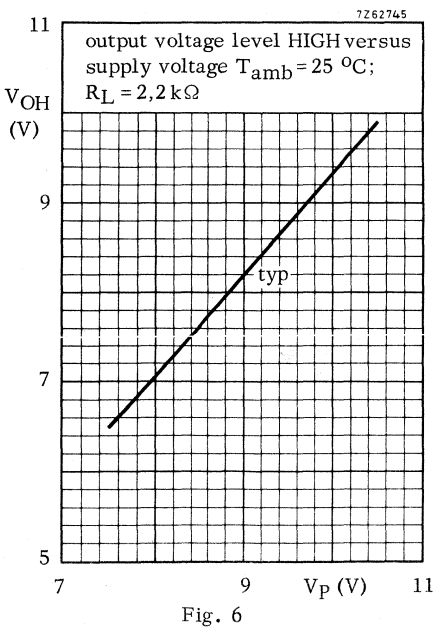
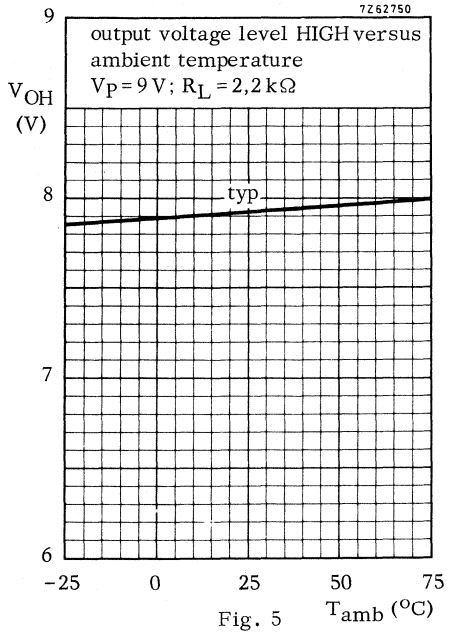
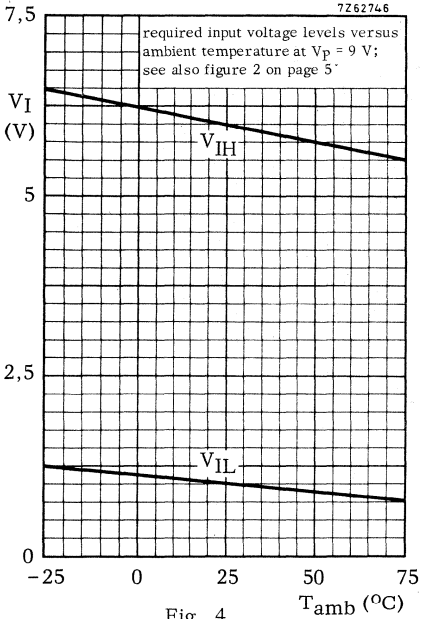


Fig. 3 Output voltage: V_O

- 1) t_L is depending on the slope of the input signal
- 2) change-over time: $t_c = \frac{t_{or} + t_{of}}{2}$



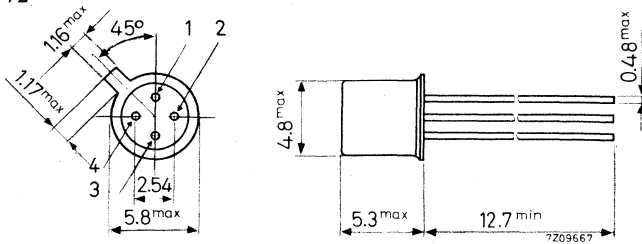
LOW-LEVEL AMPLIFIER

The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

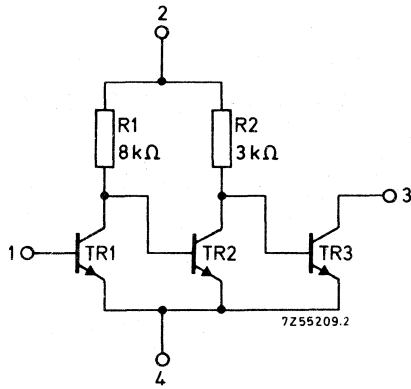
QUICK REFERENCE DATA			
Supply voltage	V_B	max.	8 V
Output voltage	V_{3-4}	max.	7 V
Output current	I_3	max.	25 mA
Transducer gain at $P_O = 10$ mW			
$R_L = 150 \Omega$; $f = 1$ kHz	G_{tr}	typ.	77 dB
Operating ambient temperature	T_{amb}	-20 to +100	°C

PACKAGE OUTLINE
TO-72

Dimensions in mm



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

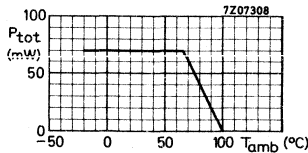
Supply voltage	V_B	max.	8 V
Output voltage	V_{3-4}	max.	7 V
Input voltage	$-V_{1-4}$	max.	5 V

Currents

Output current	I_3	max.	25 mA
Input current	I_1	max.	10 mA

Power dissipation

Total power dissipation up to $T_{amb} = 65^\circ\text{C}$	P_{tot}	max.	70 mW
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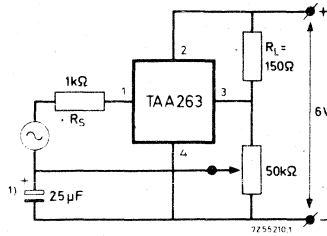
Temperatures

Storage temperature	T_{stg}	-55 to +125 °C
Operating ambient temperature (see derating curve above)	T_{amb}	-20 to +100 °C

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$

Test circuit:



Currents

Output current	I_3	typ.	12 mA
Total current drain (no signal)	$I_2 + I_3$	<	16 mA

Over-all small signal current gain

$f = 1\text{ kHz}$	$h_{f\text{ tot}}$	typ.	$5 \cdot 10^5$
--------------------	--------------------	------	----------------

Transducer gain

$f = 1\text{ kHz}; P_O = 10\text{ mW}$	G_{tr}	>	70 dB
		typ.	77 dB

Output power at $f = 1\text{ kHz}; d_{tot} = 10\%$
 $d_{tot} = 5\%$

P_O	>	10 mW
P_O	>	8 mW

Noise figure

$f = 400\text{ Hz to } 6\text{ kHz}$	F	typ.	5 dB
		<	10 dB
$f = 450\text{ kHz}; \Delta f = 5\text{ kHz}$	F	typ.	2.7 dB

¹⁾ $Z \leq 10\text{ }\Omega$ at $f = 1\text{ kHz}$

CHARACTERISTICS (continued)

 $T_{amb} = 25 \text{ }^{\circ}\text{C}$ y parameters (point 4 common connection) $V_B = 6 \text{ V}; I_3 = 3 \text{ mA}; V_{3-4} = 4.2 \text{ V}$ $f = 1 \text{ kHz}$

Input admittance

 $y_i = g_i$ typ. 20 $\mu\Omega^{-1}$

Transfer admittance

 $y_f = g_f$ typ. 11 Ω^{-1}

Output admittance

 $y_o = g_o$ typ. 60 $\mu\Omega^{-1}$ $f = 450 \text{ kHz}$

Input conductance

 g_i typ. 15 $\mu\Omega^{-1}$

Input capacitance

 C_i typ. 14 pF

Transfer admittance

 $|y_f|$ typ. 9.4 Ω^{-1}

Phase angle of transfer admittance

 Φ_f typ. 125°

Output conductance

 g_o typ. 20 $\mu\Omega^{-1}$

Output capacitance

 C_o typ. 13 pF

INTEGRATED MOST AMPLIFIER

The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.

The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).

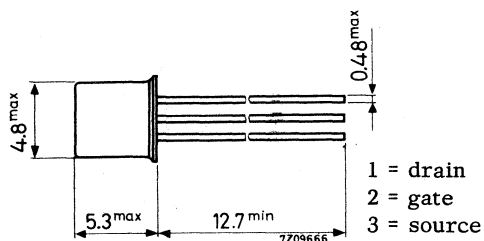
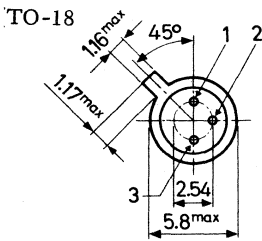
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

QUICK REFERENCE DATA

Drain-source voltage ($V_{GS} = 0$)	$-V_{DSS}$	max.	20 V
Drain current	$-I_D$	max.	25 mA
Gate-source voltage $-I_D = 10$ mA; $-V_{DS} = 10$ V	$-V_{GS}$	typ.	11 V
Gate-source resistance $-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	>	100 G Ω
Transfer admittance at $f = 1$ kHz $-I_D = 10$ mA; $-V_{DS} = 10$ V	$ y_{fs} $	typ.	75 m Ω^{-1}

PACKAGE OUTLINE

Dimensions in mm

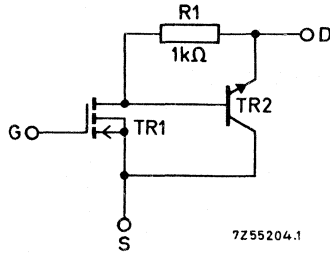


bottom view

Source connected to the case

Accessories available: 56246, 56263

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Drain-source voltage ($V_{GS} = 0$)	$-V_{DSS}$	max.	20 V
Gate-source voltage ($I_D = 0$)	$-V_{GSO}$	max.	20 V
Non repetitive peak gate-source voltage ($t \leq 10$ ms)	$-V_{GSM}$	max.	100 V

Current

Drain current	$-I_D$	max.	25 mA
---------------	--------	------	-------

Power dissipation

Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
---	-----------	------	--------

Temperatures

Storage temperature	T_{stg}	-55 to +125 °C
Operating ambient temperature (see derating curve on page 8)	T_{amb}	-20 to +125 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0.5 °C/mW
--------------------------------------	---------------	---	-----------

CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Drain current

$-V_{DS} = 20\text{ V}; V_{GS} = 0$

$-I_{DSS}$ typ. 5 nA
 < 1 μA

Gate-source voltage ¹⁾

$-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$

$-V_{GS}$ typ. 11 V
 9 to 14 V

Gate-source resistance

$-V_{GS}$ up to 20 V; T_j up to 125 $^\circ\text{C}$

r_{GS} > 100 $\text{G}\Omega$

Equivalent noise voltage

$-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$
B = 50 Hz to 15 kHz

v_n typ. 25 μV

y parameters at $f = 1\text{ kHz}$

$-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$

Transfer admittance

$|y_{fs}|$ typ. 75 $\text{m}\Omega^{-1}$
 40 to 120 $\text{m}\Omega^{-1}$

Input capacitance

C_{is} typ. 8 pF

Feedback capacitance

$-C_{rs}$ typ. 1.5 pF

Output conductance

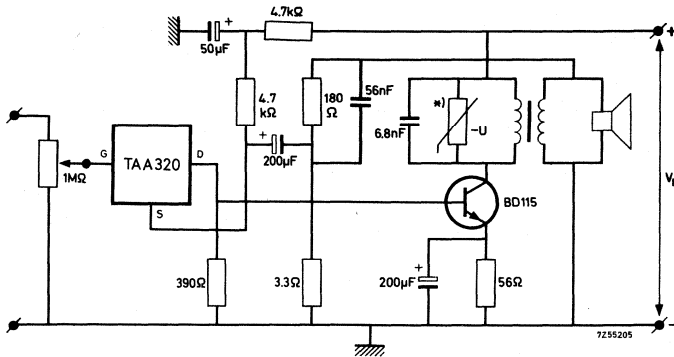
g_{os} typ. 0.65 $\text{m}\Omega^{-1}$

NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

1) $-V_{GS}$ decreases about 6 mV/ $^\circ\text{C}$ with increasing ambient temperature at a constant $-I_D$.

APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115



* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

Supply voltage	V_B	=	100 V
Collector current of BD115	I_C	typ.	50 mA
Drain current of TAA320	$-I_D$	typ.	9.5 mA
Primary d.c. resistance of output transformer			140 Ω
Primary inductance of output transformer			2.7 H
A.C. collector load for BD115			1.8 k Ω

Performance at $f = 1$ kHz; feedback = 16 dB

Output power at $d_{tot} = 10\%$

(on primary of the output transformer)

P_O typ. 2.6 W

Input voltage for $P_O = 50$ mW

$V_i(\text{rms})$ typ. 13.5 mV

Input voltage for $P_O = 2$ W

$V_i(\text{rms})$ typ. 86 mV

Total distortion at $P_O = 2$ W

d_{tot} typ. 3.6 %

Minimum frequency response (-3 dB)

60 Hz to 20 kHz

Signal-noise ratio at $P_O = 2$ W

typ. 73 dB

Mounting instruction for BD115

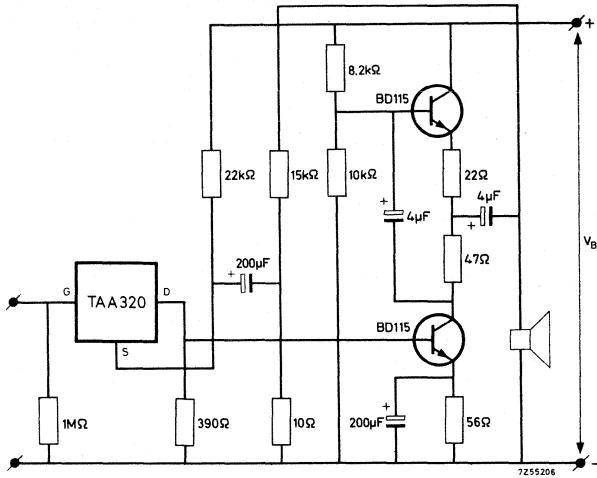
Proper continuous operation is ensured up to $T_{amb} = 50$ °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 cm² with a clamping washer of type 56218.

If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 cm².

Recommended diameter of hole in heatsink: 7.7 mm.

APPLICATION INFORMATION (continued)

4 W audio amplifier with TAA320 and 2 transistors of type BD115.

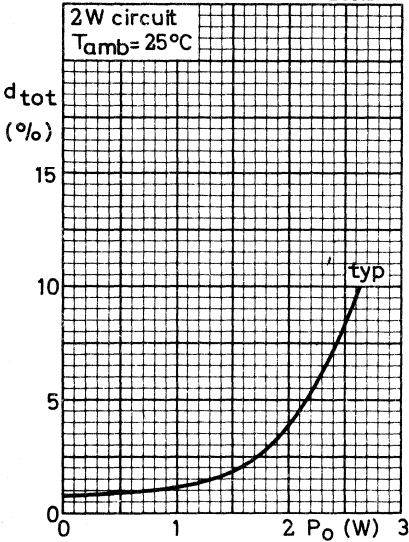


Supply voltage	V_B	=	200 V
Collector current of a BD115	I_C	typ.	52 mA
Drain current of TAA320	$-I_D$	typ.	8.6 mA

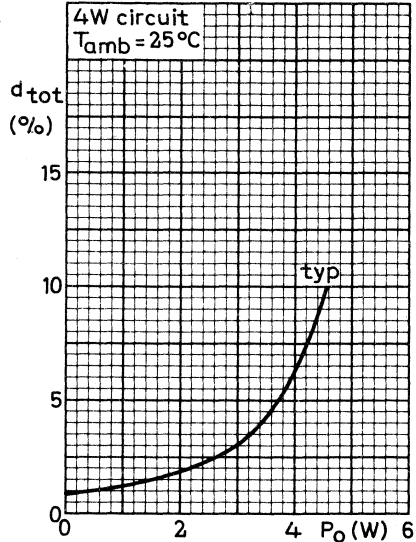
Performance at $f = 1$ kHz; feedback = 12 dB

Output power at $d_{tot} = 10\%$	P_O	typ.	4.5 W
Input voltage for $P_O = 50$ mW	$V_{i(rms)}$	typ.	7.5 mV
Input voltage for $P_O = 4$ W	$V_{i(rms)}$	typ.	67 mV
Total distortion at $P_O = 4$ W	d_{tot}	typ.	6 %
Minimum frequency response (-3 dB)			50 Hz to 20 kHz
Signal-noise ratio at $P_O = 4$ W		typ.	73 dB
Mounting instruction for BD115 see page 4			

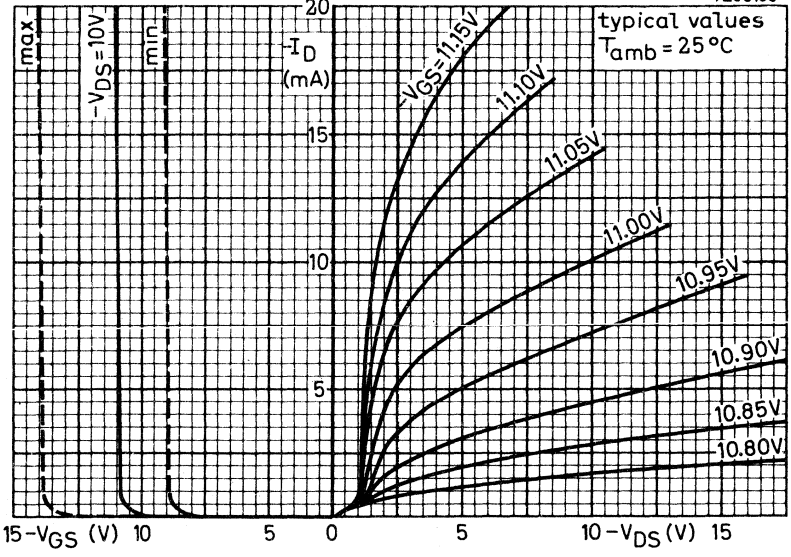
7Z08127

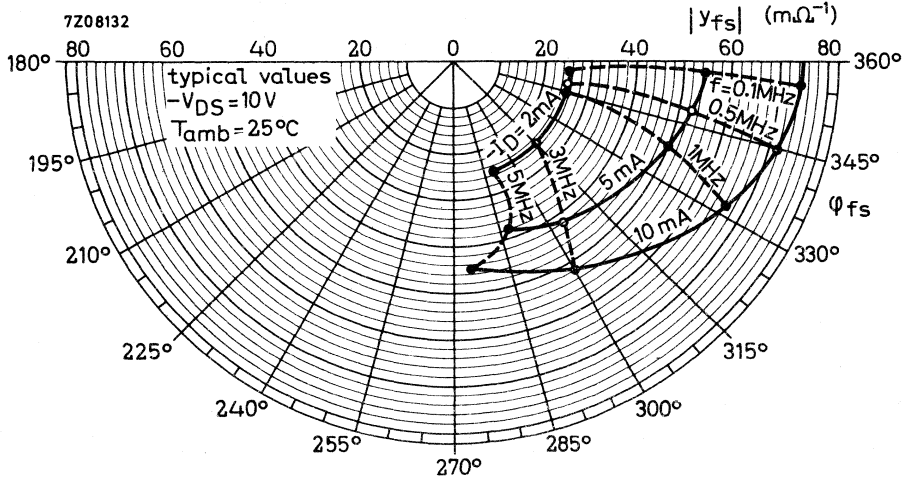
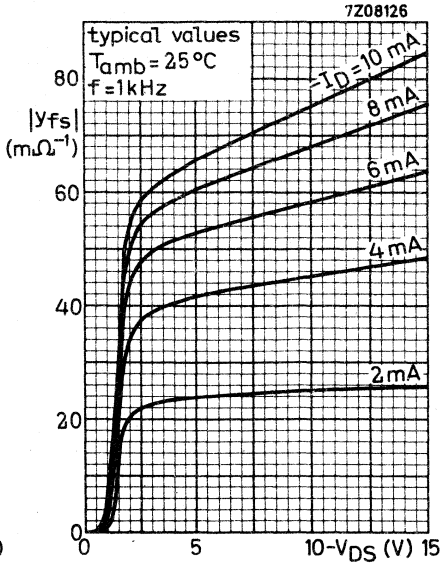
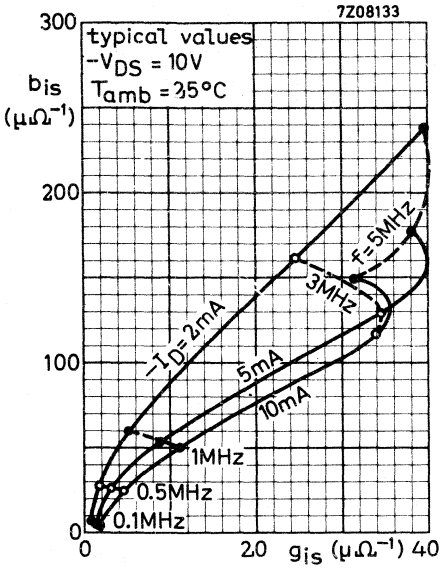


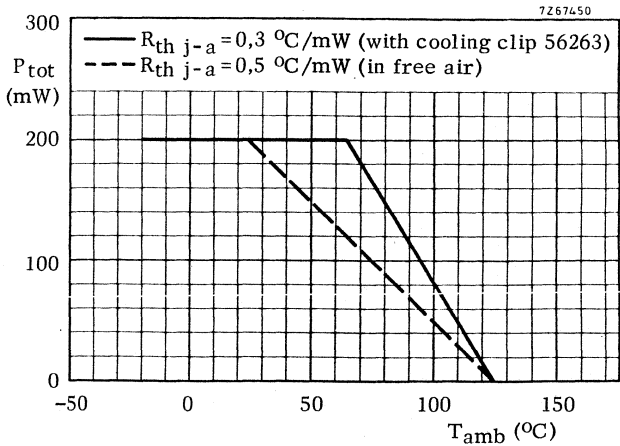
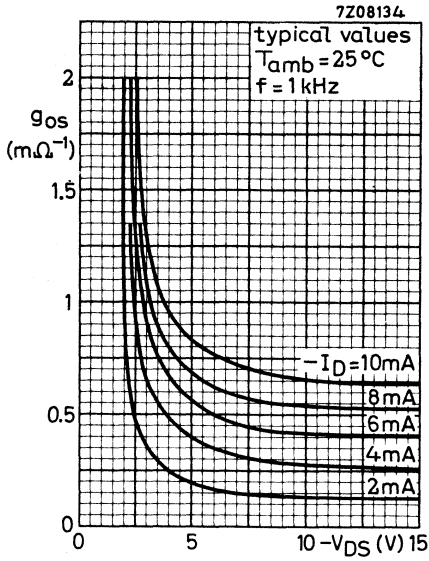
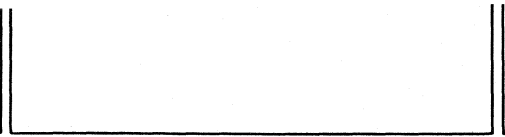
7Z08128



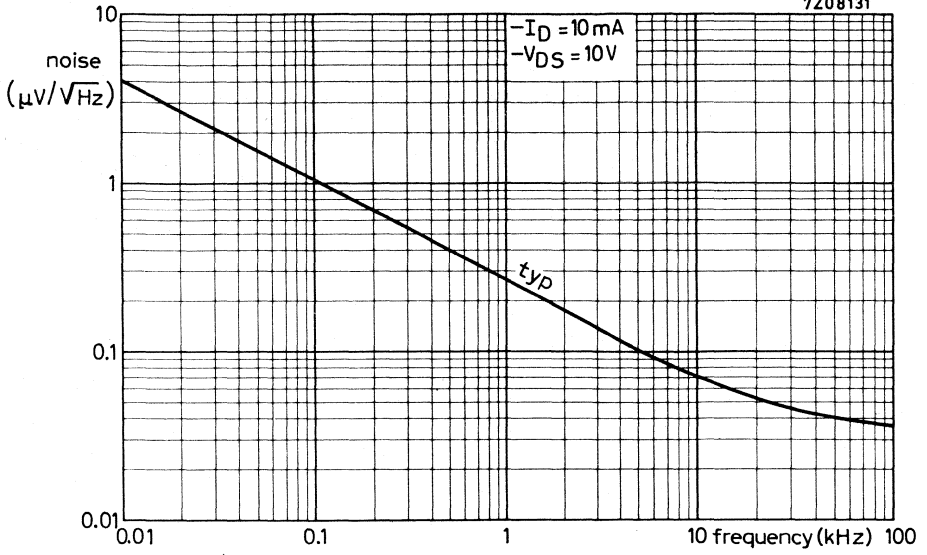
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7208131



INTEGRATED MOST LEVEL SENSOR

The TAA320A is a silicon monolithic integrated circuit, consisting of a p-channel enhancement type MOS transistor and an n-p-n transistor, in a TO-18 metal envelope. The device is intended for level sensors with a very high input resistance (e. g. timing circuits, thermostats, liquid level sensors, flame control circuits).

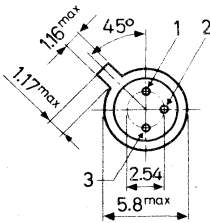
QUICK REFERENCE DATA

Drain-source voltage ($V_{GS} = 0$)	$-V_{DSS}$	max.	20	V
Drain current	$-I_D$	max.	60	mA
Gate-source voltage ¹⁾				
$-I_D = 10 \text{ mA}; -V_{DS} = 10 \text{ V}$	group 1: $-V_{GS}$	typ.	10,6	V
			10,0 to 11,2	V
	group 2: $-V_{GS}$	typ.	11,3	V
			10,7 to 11,9	V
	group 3: $-V_{GS}$	typ.	12,0	V
			11,4 to 12,6	V
	group 4: $-V_{GS}$	typ.	12,7	V
			12,1 to 13,3	V
Gate cut-off current at $T_{amb} = 25 \text{ }^\circ\text{C}$				
$-V_{GS} = 20 \text{ V}; I_D = 0$	$-I_{GSO}$	typ.	1	pA
$-V_{GS} = 20 \text{ V}; V_{DS} = 0$	$-I_{GSS}$	typ.	1	pA

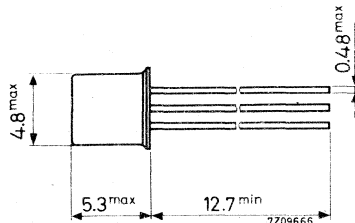
PACKAGE OUTLINE

Dimensions in mm

TO-18



bottom view



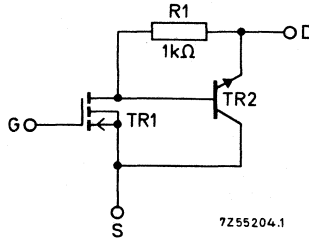
- 1 = drain
- 2 = gate
- 3 = source

source connected to the case

Accessories available on request: 56246; 56263

¹⁾ For explanation of the group codification see note b on page 3.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

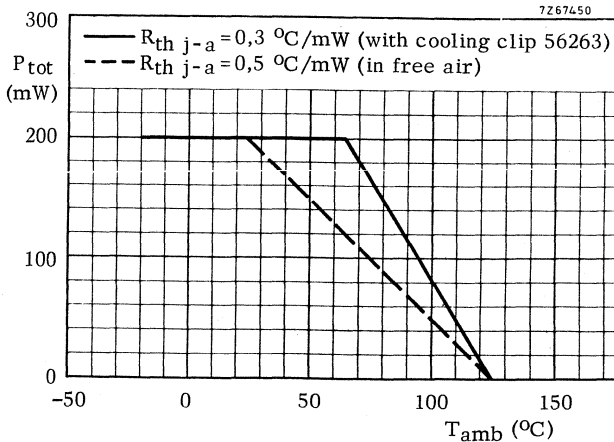
Drain-source voltage ($V_{GS} = 0$)	$-V_{DSS}$	max.	20 V
Gate-source voltage ($I_D = 0$)	$-V_{GSO}$	max.	20 V
Non-repetitive peak gate-source voltage ($t \leq 10$ ms)	$\pm V_{GSM}$	max.	100 V

Current

Drain current	$-I_D$	max.	60 mA
Peak drain current ($t < 200$ ms; $\delta 0,001$)	$-I_{DM}$	max.	100 mA

Temperatures

Storage temperature	T_{stg}	-65 to +125 °C
Operating ambient temperature (see curve below)	T_{amb}	-20 to +125 °C



CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specifiedDrain current

$-V_{DS} = 20\text{ V}; V_{GS} = 0$	$-I_{DSS}$	typ. <	5 1	nA μA
-------------------------------------	------------	-----------	--------	---------------------

Drain-source voltage ¹⁾

$-I_D = 10\text{ mA}; -V_{GS} = 20\text{ V}$	$-V_{DS}$	<	1	V
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$-I_D = 60\text{ mA}; -V_{GS} = 20\text{ V}$	$-V_{DS}$	<	1,5	V
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Gate-source voltage (see note b)

$-I_D = 10\text{ mA}; -V_{DS} = 10\text{ V}$	group 1: $-V_{GS}$	typ. 10,0 to 11,2	10,6 V	V
--	--------------------	----------------------	-----------	---

	group 2: $-V_{GS}$	typ. 10,7 to 11,9	11,3 V	V
--	--------------------	----------------------	-----------	---

	group 3: $-V_{GS}$	typ. 11,4 to 12,6	12,0 V	V
--	--------------------	----------------------	-----------	---

	group 4: $-V_{GS}$	typ. 12,1 to 13,3	12,7 V	V
--	--------------------	----------------------	-----------	---

Gate cut-off current

$-V_{GS} = 20\text{ V}; I_D = 0$	$-I_{GSO}$	typ.	1	pA ²⁾
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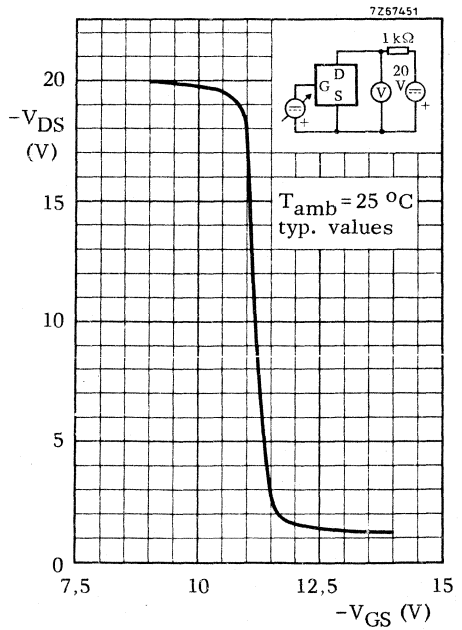
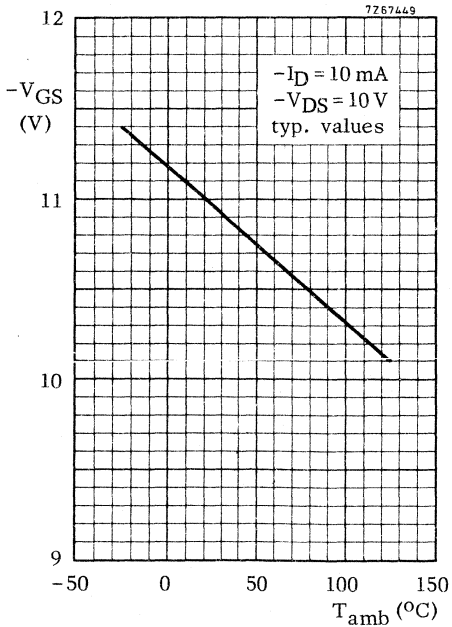
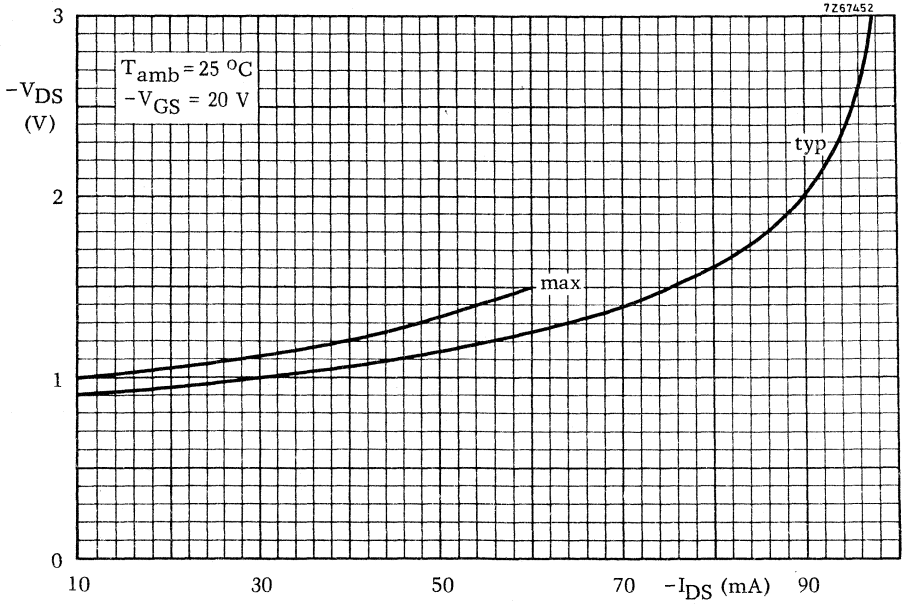
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	typ.	1	pA ²⁾
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NOTES

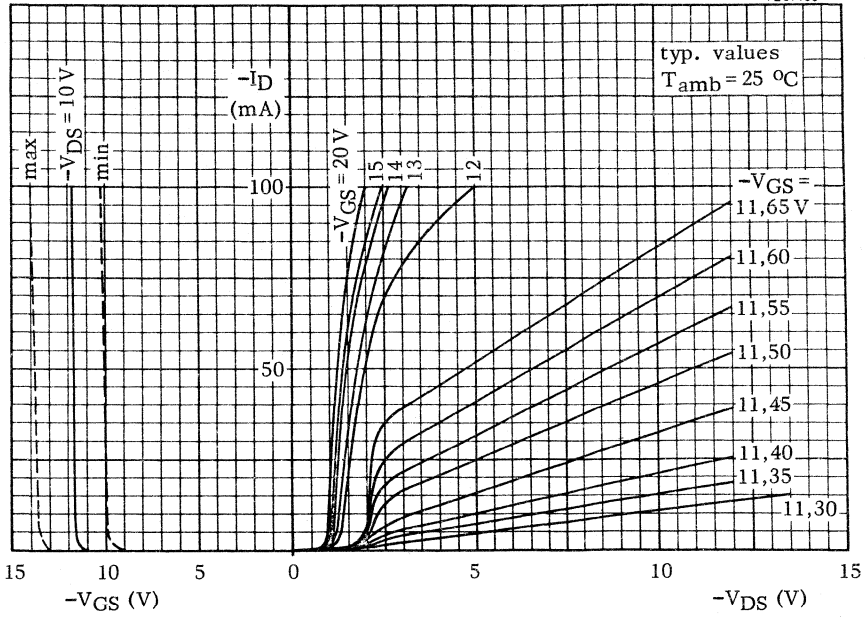
- The leads are short-circuited by a clip to protect the oxide layer against damage due to accumulation (or build-up) of electrostatic charge on the high resistance gate electrode. The clip should not be removed until after the device is mounted.
- As a service to the customer the $-V_{GS}$ group to which a device belongs is identified by a numerical suffix (1, 2, 3 or 4), however, individual groups cannot be ordered separately.

1. See also upper graph on page 4.

2. Being dependent on handling and ambient humidity, the quoted value applies only up to the time of shipping.
Efficient drying treatment is advised before the device is mounted, provided the application requires this low current.



7Z67495



INTEGRATED AM/FM RADIO RECEIVER CIRCUIT

The TBA570A is for use in small low-cost a. m. portable receivers as well as in high quality battery or mains-fed a. m. and a. m./f. m. receivers.

The IC incorporates: a. m. mixer, oscillator, i. f. amplifier, a. g. c. amplifier, a. m. detector and capacitor, f. m./i. f. limiting amplifier and stable base bias for f. m. front-end, and an audio preamplifier and driver.

The unique integrated audio part has an internally limited bandwidth (18 kHz) and negligible h. f. radiation back to the ferrite rod. This makes the TBA570A ideally suitable for small size a. m. receivers because print layout is not critical. The driver stage can directly drive complementary output stages ($P_O = 6$ W max.), or operate as a post amplifier ($V_O = 500$ mV).

In its standard applications, the TBA570A can replace the TBA570.

QUICK REFERENCE DATA

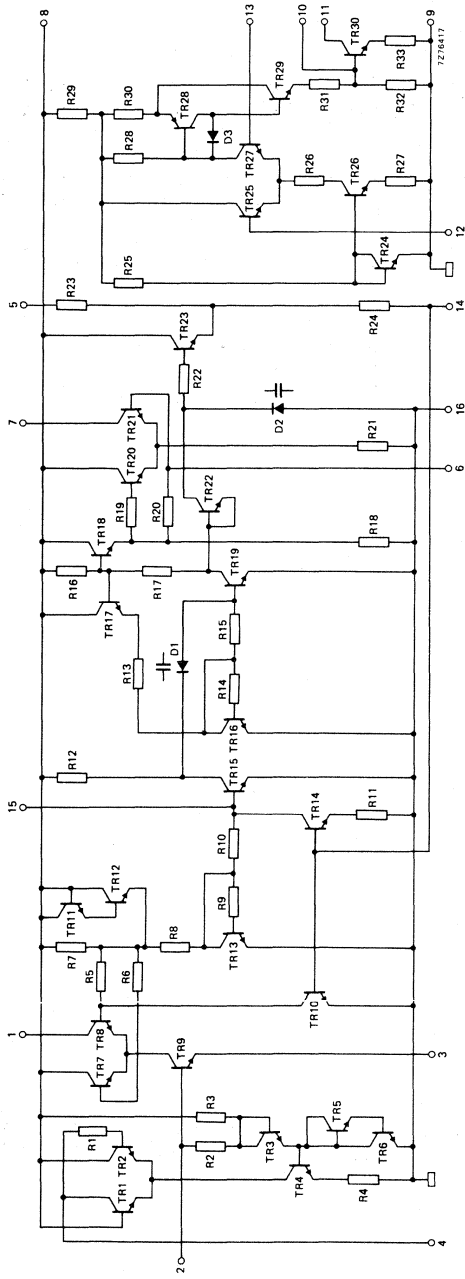
Applicable supply voltage range of receiver	V_P	2, 7 to 18	V
Ambient temperature	T_{amb}	25	°C
Supply voltage at pin 8	V_{8-16}	nom. 5, 3	V

Total quiescent current except output stages, driver stage TR30 and f. m. front-end	I_{tot}	typ. 9	mA
A.M. performance (at pin 2)			
R. F. input voltage; S/N = 26 dB	V_i	typ. 18	μ V
for $P_O = 50$ mW (adjustable)	V_i	typ. 2	μ V
A. G. C. range; change of r. f. input voltage for 10 dB expansion in audio range		typ. 65	dB
R. F. signal handling; $d_{tot} = 10\%$; $m = 0, 8$		typ. 150	mV
F.M. performance (at pin 2)			
R. F. input voltage; 3 dB before limiting	V_i	typ. 50	μ V
Audio performance			
Output driver current (peak value)	I_{11M}	< 100	mA
Input impedance (at pin 12)	$ Z_{12-16} $	typ. 100	k Ω

PACKAGE OUTLINES (see general section)

TBA570A : 16-lead DIL; plastic.

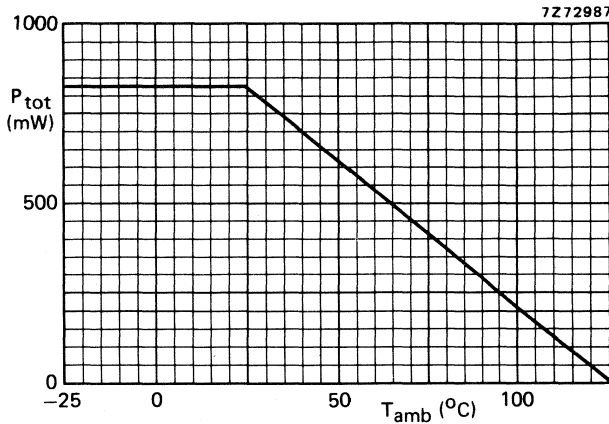
TBA570AQ : 16-lead QIL; plastic.



CIRCUIT DIAGRAM

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Pin 11 voltage	V_{11-9}	max.	18	V
Pin 8 voltage	V_{8-16}	max.	8	V
Pin 11 current (peak value)	I_{11M}	max.	100	mA
Total power dissipation	see derating curve below			
Storage temperature	T_{stg}	-55 to +125	°C	
Operating ambient temperature; $V_{8;4;7;1-16} = 8\text{ V}$; $I_{11M} = 100\text{ mA}$; see also derating curve below	T_{amb}	-20 to +85	°C	



DESIGN DATA

Characteristics of integrated components are determined by process and layout data.

Pins not under measuring condition should not be connected.

Voltages with respect to pin 9 and 16 (tolerated minimum : 0 V)

Pins 1 and 7	$V_{1-9(16)}$ } $V_{7-9(16)}$ }	max.	18	V
Pin 4	$V_{4-9(16)}$	max.	8	V
Pin 8	$V_{8-9(16)}$	max.	8	V
Pin 3	$V_{3-9(16)}$	max.	3	V
Pin 5	$V_{5-9(16)}$	max.	4	V
Pin 14	$V_{14-9(16)}$	max.	1	V

Currents (tolerated minimum : 0 mA)

Pins 2, 6, 12, 13 and 15	$I_2; I_6; I_{12}$ } $I_{13}; I_{15}$ }	max.	80	µA
Pin 10	I_{10}	max.	5	mA

D.C. CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$

Saturation voltage of driver stage

$I_C = 50\text{ mA}; I_B = 2,5\text{ mA}$

$V_{11-16sat}$	typ.	1,0	V
	<	1,5	V

Collector breakdown voltage of driver stage

$I_C = 25\text{ mA}; R_{BE} = 7\text{ k}\Omega$

$V_{11-16(BR)}$	>	18	V
-----------------	---	----	---

D. C. current gain of driver stage

$I_C = 50\text{ mA}$

h_{FE}	>	25	
----------	---	----	--

Total quiescent current

except driver stage collector current;

f. m. front-end;

discrete output stages: $V_{8-16} = 5,3\text{ V}$

$V_{8-16} = 4,2\text{ V}$

I_{tot}	typ.	9	mA
I_{tot}	typ.	8	mA

Applicable supply voltage range of receiver

V_P		2,7 to 18	V ¹⁾
-------	--	-----------	-----------------

Base bias voltage for f. m. front-end

total external load current at pin 2: $-I_2 = 150\mu\text{A}$

V_{2-16}	typ.	1,2	V
------------	------	-----	---

A.C. CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}; V_{8-16} = 5,3\text{ V}; I_E (TR9) = 1\text{ mA}$

		0,45	1	10,7	MHz
Input conductance at pin 2	g_{ie} typ.	-	0,4	0,5	mA/V
Output conductance at pin 1	g_{oe} typ.	6	-	90	$\mu\text{A}/\text{V}$
Input conductance at pin 15	g_{ie} typ.	0,35	-	0,7	mA/V

¹⁾ Adjustable by a dropping resistor in the V_P -line; see also maximum tolerated voltages for pins 1, 4, 7 and 8 in design data on page 3.

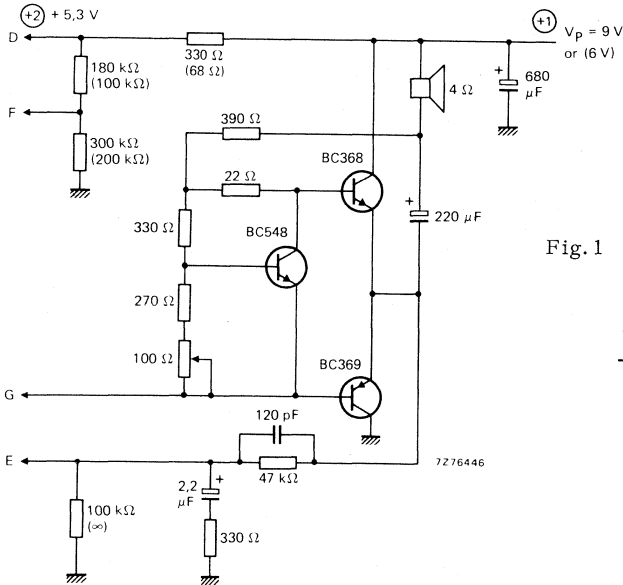


Fig. 1 Output stage for $V_P = 9\text{ V}$ or 6 V (resistor values between parentheses).

V_P	R_L	P_O at $d_{tot} = 10\%$
9 V	4 Ω	1,8 W
6 V	4 Ω	0,6 W

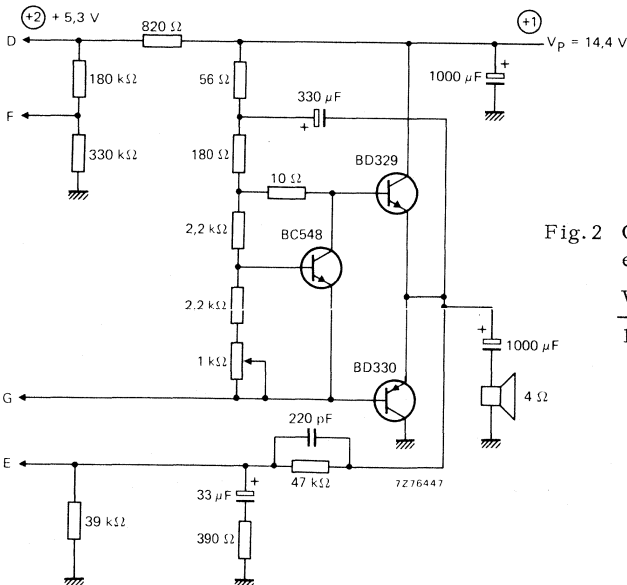


Fig. 2 Output stage for $V_P = 14,4\text{ V}$; especially used in car radios.

V_P	R_L	P_O at $d_{tot} = 10\%$
14,4 V	4 Ω	5,5 W

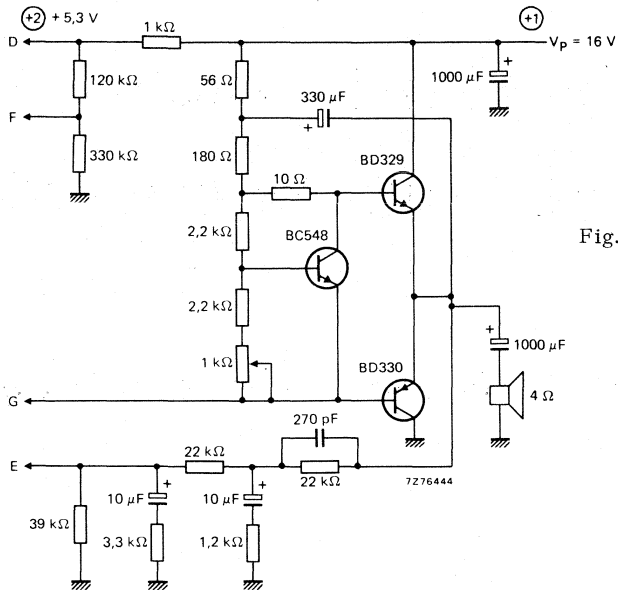


Fig. 3 Output stage for $V_p = 16 V$.

V_p	R_L	P_o at $d_{tot} = 10\%$
16 V	4 Ω	6, 8 W

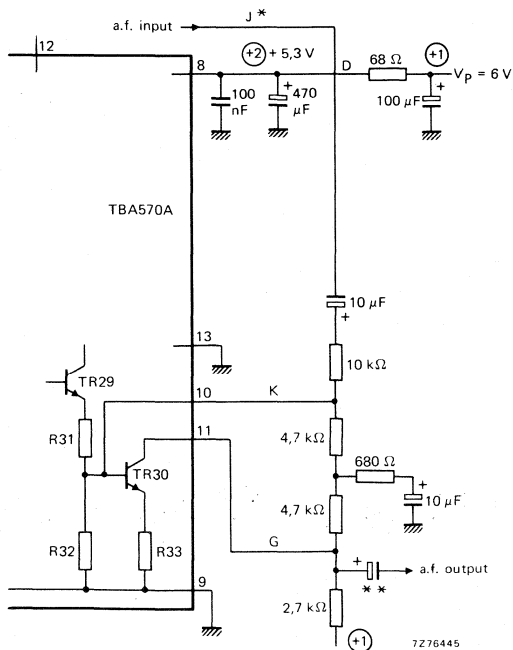


Fig. 4 Post amplifier for $V_o = 500 mV$ and $V_p = 6 V$.

*In circuit on page 5 volume control resistor (100 kΩ) and capacitor (100 nF) on pin 12 should be omitted.

** Capacitor value depends on load.

COIL DATA (in circuit on page 5)

High quality AM/FM receiver (for portable and mains-fed applications)

A.M. -I.F. coils ($f_0 = 455$ kHz)

I. F. bandpass filter :

L9 $N_1 = 284, 5 \mu\text{H}$ **L10** $N_1 = 680 \mu\text{H}$
 $Q_0 = 100$ $Q_0 = 100$
 $N_1/N_2 = 40$ $N_2/N_1 = 74$
 $N_2/N_3 = 1$ $(N_2 + N_1)/N_3 = 10, 7$
 $|Z_T| = 3 \text{ k}\Omega$



F.M. -I.F. coils ($f_0 = 10, 7$ MHz)

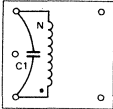
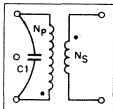
Second i.f. bandpass filter :

Ratio detector :

L7 $N_1 + N_2 = 2, 7 \mu\text{H}$ **L8** $N_1 = 2, 7 \mu\text{H}$ **L11** $N_1 = 2, 7 \mu\text{H}$ **L12** $N_2 + N_3 = 3, 25 \mu\text{H}$
 $Q_0 = 100$ $Q_0 = 90$ $Q_0 = 85$ $Q_0 = 85$
 $kQL_{6-L7} = 1, 2$ $N_1/N_2 = 5, 5$ $kQL_{11-L12} = 0, 7$ $(N_2 + N_3)/N_1 = 6$
 $N_1/N_2 = 1, 75$ $N_1/N_2 = 2, 2$ $N_2 = N_3$

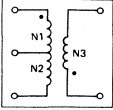
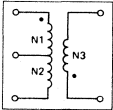
Low-cost 2-band AM portable receiver (see page 9)

L1  $N_1 = 11$ **L2**  $N_1 = 60$
 $N_2 = 2$ $N_2 = 4$ **L1 and L2 on ferrite rod; 10 mmØ;**
wire : 1, 1 Ø **wire : 20 x 0, 03** **length = 10 cm**

L3  $N = 284, 5 \mu\text{H}$ $f_m = 452$ kHz **L4**  $N_p = 284, 5 \mu\text{H}$ $f_m = 452$ kHz
 $C_1 = 430$ pF $Q_0 = 100$ $N_p/N_s = 16, 7$ $Q_0 = 100$
wire : 0, 1 Ø **wire : 0, 1 Ø**

core material : 7 MN(C)

core material : 7 MN(C)

L5  $N_1 + N_2 = 127 \mu\text{H}$ $f_m = 1$ MHz **L6**  $N_1 + N_2 = 13 \mu\text{H}$ $f_m = 7$ MHz
 $(N_1 + N_2)/N_2 = 58$ $Q_0 = 100$ $(N_1 + N_2)/N_2 = 20$ $Q_0 = 90$
 $(N_1 + N_2)/N_3 = 4, 8$ $C_p = 200$ pF $(N_1 + N_2)/N_3 = 4$ $C_p = 40$ pF
wire : 0, 1 Ø **wire : 0, 1 Ø**

core material : 7 BR

core material : 119 AM(C)

Note

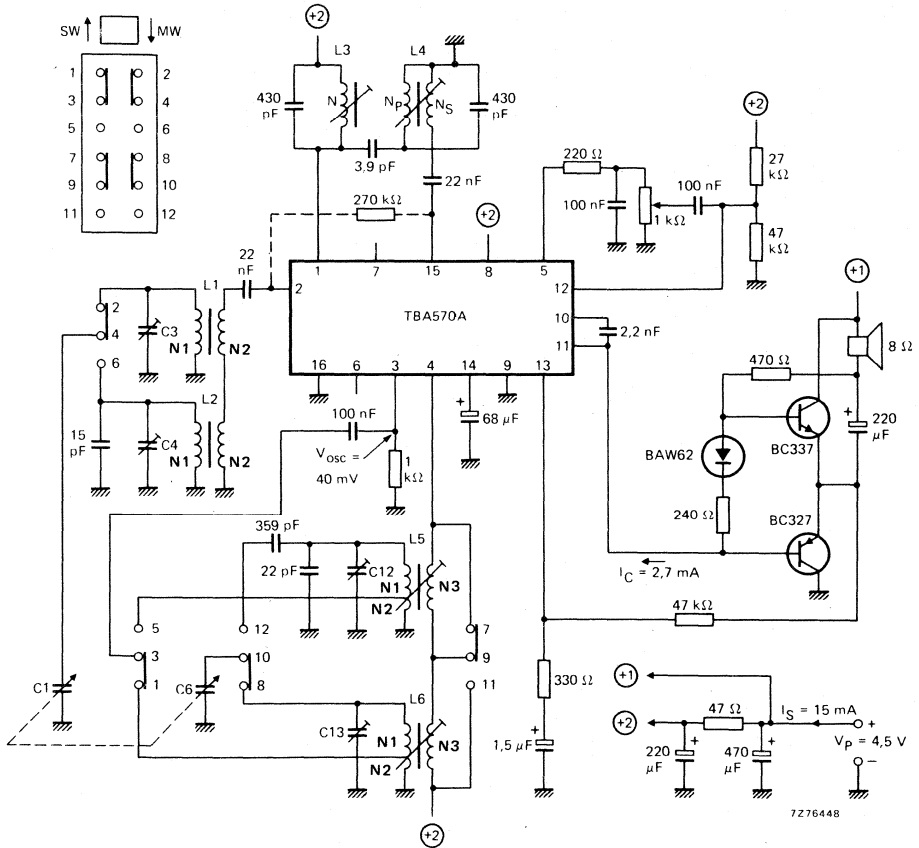
In the circuit on page 9 for L3 and L4 a similar coil to L9 in the circuit on page 5 can be used with the following exceptions :

L3 : secondary windings N2 and N3 are not used.

L4 : secondary windings N2 and N3 are connected in series.

When using a resistor between pins 2 and 15 (see dashed resistor in circuit on page 9), signal handling is improved.

Low-cost 2-band (SW-MW) AM portable receiver ($P_O = 250 \text{ mW}$)



Note: C1 and C6 max. 385 pF.

APPLICATION INFORMATION at $T_{amb} = 25\text{ }^{\circ}\text{C}$

A.M. performance	V_{8-16}	5, 3 V 1)	4, 2 V 2)
R. F. input voltage: $S/N = 26\text{ dB}$ (notes 3 and 4) for $P_o = 50\text{ mW}$ (adjustable); notes 3, 4 and 5	V_i	typ. 18	10 μV
	V_i	typ. 2	2 μV
R. F. input voltage for 10 mV (a. f.) across volume control (notes 3 and 4)	V_i	typ. 2, 7	4, 5 μV
A. F. voltage across volume control at 100 μV (r. f.) input voltage (notes 3 and 4)	V_o	typ. 70	70 mV
Signal-to-noise ratio at 1 mV (r. f.) input voltage (notes 3 and 4)	S/N	typ. 46	47 dB
A. G. C. range (change in r. f. input voltage for 10 dB expansion in audio range); notes 3 and 4		typ. 60	60 dB
R. F. signal handling capability at 80% modulation; $d_{tot} < 10\%$ (note 3)	V_i	typ. 150	7 mV
Harmonic distortion of h. f. part over most of a. g. c. range; $m = 0, 3$; $f_m = 1\text{ kHz}$ (note 6)	d_{tot}	typ. 1	1 %
I. F. selectivity	S_9	typ. 33	16 dB
I. F. bandwidth (3 dB)	B	typ. 5	5, 5 kHz

Notes

- See circuits on pages 5, 6 and 7 (high quality AM/FM receiver).
- See circuit on page 9 (low-cost 2-band AM portable receiver).
- A. F. signal: measured across volume control.
 - R. F. signal: measured at pin 2 with the aerial circuit connected (source resistance about 1 $\text{k}\Omega$).
 - $f_o = 1\text{ MHz}$; $f_m = 1\text{ kHz}$.
- $m = 0, 3$.
- A. M. sensitivity for $P_o = 50\text{ mW}$ can be adjusted by means of the a. c. feedback network in the audio part e. g. : $V_i = 1, 5\text{ }\mu\text{V}$ for $P_o = 50\text{ mW}$ ($S/N \approx 4\text{ dB}$).
- Distortion can be decreased to 0, 7% by connecting a resistor of 270 $\text{k}\Omega$ between pins 2 and 15.

APPLICATION INFORMATION (continued) at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{8-16} = 5,3\text{ V}$

Measured in the circuit on page 5

F.M. performance

Sensitivity for an f. m. signal 3 dB before limiting

at $75\text{ }\Omega$ aerial input of f. m. front-end (note 1)

at pin 2; first i. f. (notes 2 and 6)

 V_i typ. 3,5 μV V_i typ. 50 μV

Sensitivity for 26 dB S/N ratio

at $75\text{ }\Omega$ aerial input of f. m. front-end (note 1) V_i typ. 2,5 μV

A.F. output voltage across volume control

at an i. f. signal beyond limiting (note 2)

 V_o typ. 120 mV

Signal-to-noise ratio

over most of signal range (note 2)

S/N typ. 65 dB

A.M. suppression over most of signal range (note 3)

typ. 60 dB

I.F. selectivity (note 4)

 S_{300} typ. 43 dB

I.F. bandwidth (3 dB; note 4)

B typ. 150 kHz

A.F. signal distortion

3 dB before i. f. limiting (note 5)

 d_{tot} typ. 0,8 %

Notes

1. Aerial e. m. f. (V_i) at $f_o = 98\text{ MHz}$; $R_S = 50\text{ }\Omega$; $\Delta f = \pm 22,5\text{ kHz}$; $f_m = 1\text{ kHz}$.
2. $f_o = 10,7\text{ MHz}$; $\Delta f = \pm 22,5\text{ kHz}$; $f_m = 1\text{ kHz}$.
3. A.M. signal: $m = 0,3$; $f_m = 1000\text{ Hz}$.
F.M. signal: $f_o = 10,7\text{ MHz}$; $\Delta f = \pm 75\text{ kHz}$; $f_m = 400\text{ Hz}$.
Carrier simultaneously modulated with a. m. and f. m.
4. Including ratio detector.
5. $f_o = 98\text{ MHz}$; $\Delta f = \pm 40\text{ kHz}$; $f_m = 1\text{ kHz}$.
6. Pin 3 by-passed to ground with a capacitor of 220 nF.

AUDIO PERFORMANCE

Distortion before clipping (note 1)	d_{tot}	typ.	0,5	%
Input impedance (note 2)	$ Z_i $	typ.	90	k Ω
Noise output power; volume control at min. (note 3)	P_n	typ.	10	nW
Overall fidelity; flat within 3 dB (obtainable values)			35 Hz to 15	kHz
Open loop voltage gain	G_v	typ.	62	dB

V_P	V	4,5	6	9	14,4	16
R_L	Ω	8	4	4	4	4
P_O at $d_{tot} = 10\%$	W	0,22	0,6	1,8	5,5	6,8
P_O at onset of clipping; $d_{tot} = 1\%$	W	0,15	0,4	1,2	4	4,8
V_i for $d_{tot} = 10\%$ (pin 12)	mV	14	16	25	50	45
V_i for $P_O = 50$ mW (pin 12)	mV	5,5	4,5	4	3,5	3,5
Output transistors		BC327 BC337	BC368 BC369	BC368 BC369	BD329 BD330	BD329 BD330
Circuit diagrams on page 6, 7 or 9		page 9	Fig. 1	Fig. 1	Fig. 2	Fig. 3

Post-amplifier (see Fig. 4 on page 7)

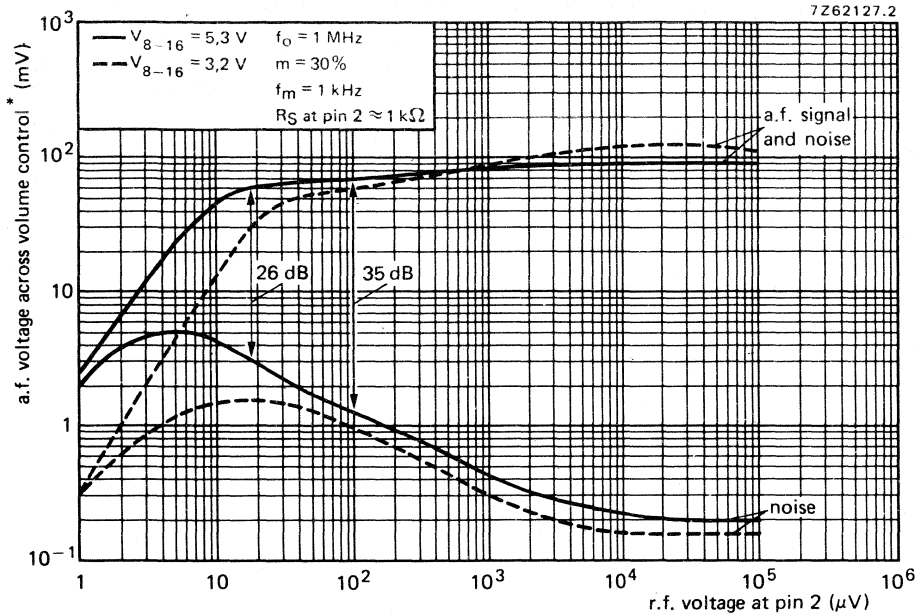
Output voltage	: 500 mV
Audio gain (adjustable):	5
Distortion	: 0,2%

Notes

1. Measured at 1 kHz and a negative feedback of 16 dB.
2. At the maximum tolerated value of resistance-tap/bleeder at pin 12.
3. Measured at a bandwidth of 60 Hz to 15 kHz, pin 12 being connected via a capacitor of 32 μ F to pin 9; $R_L = 4 \Omega$.

APPLICATION INFORMATION (continued)

Typical a.g.c. curves for AM reception (circuit diagram on page 5)

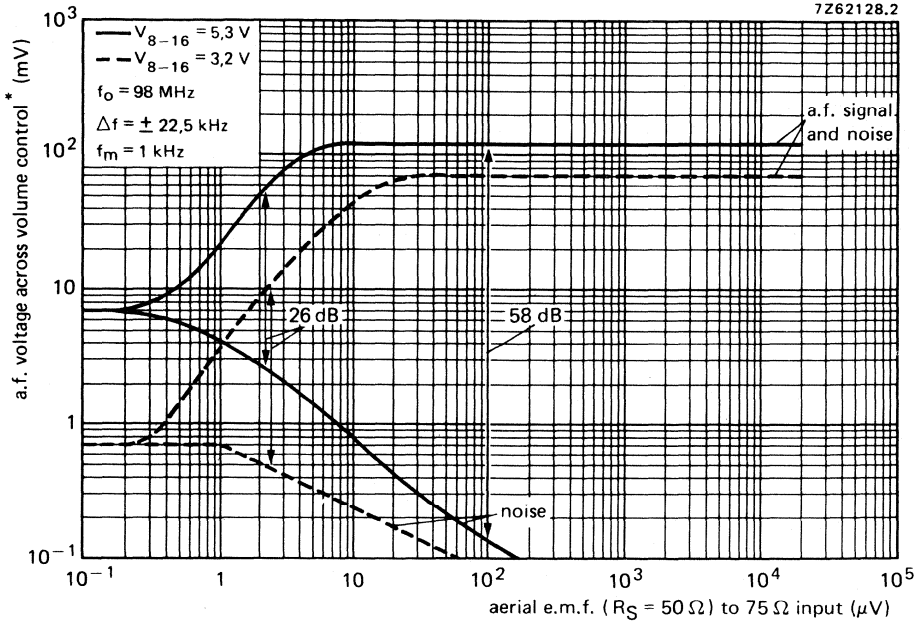


A.F. voltage across volume control as a function of r.f. voltage at pin 2.

*) Slider at lower end.

APPLICATION INFORMATION (continued)

Typical S/N curves for FM reception (circuit diagram on page 5)



A. F. voltage across volume control as a function of aerial e. m. f. from a source with $R_S = 50 \Omega$ to the 75Ω input of the f. m. front-end.

*) Slider at lower end.

INTEGRATED A.M./F.M. RADIO RECEIVER CIRCUIT

The TBA700 is a monolithic integrated circuit for use in a.m. (including the short-wave band), a.m./f.m. receivers.

It incorporates the class-B audio output stage (1 W), stabilization circuit for quiescent current, driver, pre-amplifier, 2-stage i.f. amplifier, a.g.c. and stabilized bias circuit.

The discrete input stage (for a.m.: mixer-oscillator; for f.m.: 1st i.f.) enables a high flexibility in circuit lay-out with conventional or lumped selectivity.

The internal stabilization ensures negligible loss of sensitivity and cross-over distortion over a wide supply voltage range from 2,7 V to 12 V.

QUICK REFERENCE DATA

Applicable supply voltage range of receiver	V_{10-8}	2,7 to 12	V ¹⁾
Ambient temperature	T_{amb}	25	°C
Supply voltage	V_P	nom. 9	V

Total quiescent current (inclusive discrete input transistor, exclusive f.m. front end)	I_{tot}	typ. 24,5	mA
A.F. output power at $d_{tot} = 10\%$, $R_L = 8\ \Omega$	P_O	typ. 1000	mW
<u>A.M. performance</u>			
R.F. input voltage (S/N = 26 dB) (at base of external mixer-oscillator)	V_i	typ. 15	μ V
A.G.C. range (change of r.f. input voltage for 10 dB expansion in audio range)		typ. 72	dB
<u>F.M. performance</u>			
R.F. input voltage (at base of external i.f. stage) 3 dB before limiting	V_i	typ. 150	μ V

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic with internal copper slug.

¹⁾ The data given in this sheet are based on a receiver with $V_P = 9$ V; $P_O = 1000$ mW.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Pin No. 10 voltage	V_{10-8}	max.	12	V
Pins No. 15, 9, 2 voltages	$V_{15-8}, V_{9-8}, V_{2-8}$	max.	11,4	V
Pin No. 16 voltage	V_{16-8}	max.	0	V 1)
Pin No. 7 voltage	$\pm V_{7-8}$	max.	5	V
Pins No. 4, 3, 1 voltages	$-V_{4-16}, -V_{3-16}, -V_{1-16}$	max.	5	V
Pin No. 5 voltage	$\pm V_{5-13}$	max.	5	V
Pin No. 10 voltage	V_{10-9}	max.	11,4	V

Currents

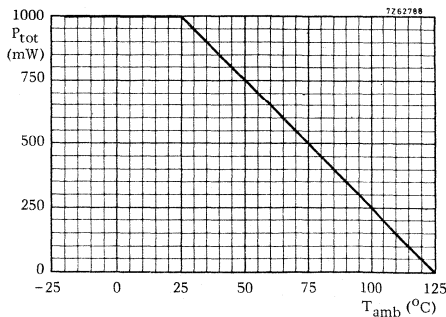
Pins No. 14, 12, 11, 6 currents	$I_{14}, I_{12}, I_{11}, I_6$	max.	5	mA
Pins No. 13, 5, 4, 3, 1 currents	$I_{13}, I_5, I_4, I_3, I_1$	max.	0,5	mA
Pins No. 15, 2 currents	I_{15}, I_2	max.	10	mA
Pin No. 8 current	$-I_{8RM}$	max.	0,8	A 2)
Pin No. 9 current	$\pm I_{9RM}$	max.	0,8	A 2)
Pin No. 10 current	I_{10RM}	max.	0,8	A 2)

Dissipation

Total power dissipation				
at $T_{amb} = 45\text{ }^{\circ}\text{C}$	P_{tot}	max.	800	mW
at $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1000	mW

Temperatures

Storage temperature	T_{stg}	-55 to +125	$^{\circ}\text{C}$
Operating ambient temperature	T_{amb}	-20 to +125	$^{\circ}\text{C}$



- 1) Substrate connected to pin 16.
- 2) Repetitive peak value; internally limited.

CHARACTERISTICS

D.C. characteristics at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_p = 9\text{ V}$

I. F. amplifier

Collector current of i. f. transistor TR2
(a. g. c. transistor "off")

I_C typ. 1 mA
0,55 to 1,6 mA

Collector current of i. f. transistor TR3
(a. g. c. transistor "off")

I_C typ. 2,5 mA
1,4 to 4,2 mA

Saturation voltage of i. f. transistor TR2
at $I_C \leq 2\text{ mA}$

V_{CEsat} < 150 mV

Saturation voltage of i. f. transistor TR3
at $I_C \leq 5\text{ mA}$

V_{CEsat} < 200 mV

Bias voltage for mixer and tuner

V_{14-16} $\left\{ \begin{array}{l} \text{typ. } 1,4\text{ V} \\ 1,25\text{ to }1,55\text{ V} \end{array} \right.$

Temperature dependency of
bias voltage V_{14-16}

T_c typ. $-3,6\text{ mV}/^{\circ}\text{C}$

Bias current (available)

$-I_{14}$ < 100 μA

A. F. amplifier

Input common mode voltage range

V_{5-8}, V_{13-8} 1,0 to 8,5 V ¹⁾

Input base bias current

I_5, I_{13} < 25 μA

Complete circuit

Total quiescent current with 3,3 k Ω

between pins 7 and 8 (inclusive discrete

input transistor, exclusive f. m. front end)

I_{tot} typ. 24,5 mA ²⁾
< 30,5 mA ²⁾

1) Maximum input common mode voltage; $V_{5-8}, V_{13-8} < (V_p - 0,5)\text{ V}$.

2) In those cases where a lower supply current is required the resistor between pins 7 and 8 (3,3 k Ω) can be avoided, resulting in a total current of 17 mA. In this case however some devices may show a marginal increase of the distortion level.

CHARACTERISTICS (continued)

A.C. characteristics of i.f. part

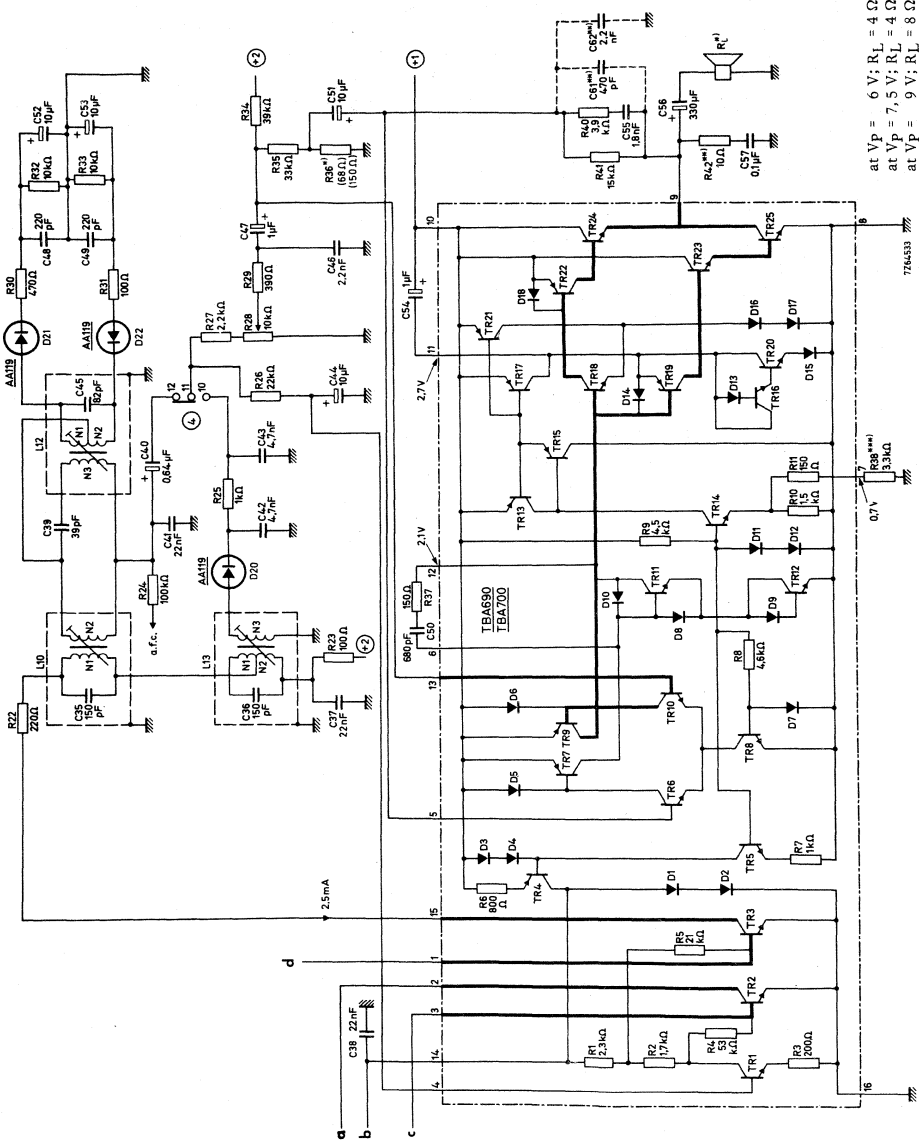
y parameters at $f = 450 \text{ kHz}$ ¹⁾

	i. f. transistors: TR2		TR3	
Input conductance	g_{ie}	typ. 0,45	1,15	mA/V
Input capacitance	C_{ie}	typ. 23	36	pF
Output conductance	g_{oe}	typ. 6,0	13,5	$\mu\text{A/V}$
Output capacitance	C_{oe}	typ. 4,0	4,25	pF
Transfer admittance	$ y_{fe} $	typ. 37	82	mA/V
Phase angle of transfer admittance	φ_{fe}	typ. 1°	2°	
Feedback admittance	$ y_{re} $	typ. 2,5	1,8	$\mu\text{A/V}$
Phase angle of feedback admittance	φ_{re}	typ. 90°	90°	

y parameters at $f = 10,7 \text{ MHz}$ ¹⁾

	i. f. transistors: TR2		TR3	
Input conductance	g_{ie}	typ. 0,6	1,5	mA/V
Input capacitance	C_{ie}	typ. 22	35	pF
Output conductance	g_{oe}	typ. 24	30	$\mu\text{A/V}$
Output capacitance	C_{oe}	typ. 4,3	4,7	pF
Transfer admittance	$ y_{fe} $	typ. 35	73	mA/V
Phase angle of transfer admittance	φ_{fe}	typ. 22°	35°	
Feedback admittance	$ y_{re} $	typ. 64	43	$\mu\text{A/V}$
Phase angle of feedback admittance	φ_{re}	typ. 90°	90°	

1) At typical values for h_{fe} and I_c .



at $V_p = 6\text{ V}$; $R_L = 4\ \Omega$
 at $V_p = 7.5\text{ V}$; $R_L = 4\ \Omega$
 at $V_p = 9\text{ V}$; $R_L = 8\ \Omega$

Reference numbers L9 and L11 are not used in this circuit.

APPLICATION INFORMATION (continued) at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_P = 9\text{ V}$

See also circuit diagram on pages 6 and 7.

A. M. performance

R. F. input voltage for signal to noise ratio of 26 dB	V_i	typ.	15	μV	¹⁾²⁾
R. F. input voltage for 10 mV (a. f.) across volume control	V_i	typ.	3	μV	¹⁾²⁾
A. F. voltage across volume control at 100 μV (r. f.) input voltage	V_o	typ.	100	mV	¹⁾²⁾
Signal to noise ratio at 1 mV (r. f.) input voltage	S/N	typ.	53, 4	dB	¹⁾²⁾
A. G. C. range (change in r. f. input voltage for 10 dB expansion in audio range)					
without a. g. c. diode		typ.	42	dB	¹⁾²⁾³⁾
with a. g. c. diode		typ.	72	dB	¹⁾²⁾
R. F. signal handling capability on base of TR26 80% modulation ($d_{tot} \leq 10\%$)					
without a. g. c. diode	V_i	typ.	6	mV	³⁾
with a. g. c. diode	V_i	typ.	80	mV	
Harmonic distortion of h. f. part (over most of a. g. c. range)	d_{tot}	typ.	1	%	¹⁾²⁾
I. F. selectivity	S_9	typ.	30	dB	
I. F. bandwidth	B_{3dB}	typ.	4, 5	kHz	

1) a. Negligible influence of supply voltage variations in a range of 2,7 V to 12 V

b. A. F. signal: measured across volume control.

c. R. F. signal: measured at base of external mixer-oscillator with the antenna-circuit connected (source resistance R_S of about 1 k Ω).

d. $f_o = 1\text{ MHz}$, $f_m = 1\text{ kHz}$

2) $m = 0.3$

3) Dashed parts of circuit diagram on pages 6 and 7 are omitted.

APPLICATION INFORMATION (continued) See also circuit on pages 6 and 7.

F.M. performanceSensitivity for an f.m. signal 3 dB
before limiting

at 75 Ω aerial input of f.m. front end	V_i	typ.	12	μV	1)
at base of external (first i.f.) stage	V_i	typ.	150	μV	2)
at pin 3	V_i	typ.	2,2	mV	2)

Sensitivity for 26 dB S/N ratio

at 75 Ω aerial input of f.m. front end	V_i	typ.	4	μV	1)
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A.F. output voltage across volume
control at an i.f. signal beyond limiting

	V_o	typ.	140	mV	2)
--	-------	------	-----	----	----

S/N ratio over most of signal range

	S/N	typ.	55	dB	2)
--	-----	------	----	----	----

A.M. suppression over most of signal range

	>	40	dB	2)3)
--	---	----	----	------

I.F. selectivity

	S_{300}	typ.	40	dB	4)
--	-----------	------	----	----	----

I.F. bandwidth

	$B_{3\text{dB}}$	typ.	180	kHz	4)
--	------------------	------	-----	-----	----

A.F. signal distortion, 3 dB before i.f. limiting

	d_{tot}	<	2	%	5)
--	------------------	---	---	---	----

Audio performanceA.F. output power at $d_{\text{tot}} = 10\%$
at onset of clipping

	P_o	typ.	1	W	6)
	P_o	typ.	0,7	W	6)

Distortion before clipping

	d_{tot}	typ.	1	%	6)
--	------------------	------	---	---	----

A.F. input signal (at pin 13)

at $P_o = 50$ mWat $P_o = 700$ mW

	V_i	typ.	6	mV	6)
	V_i	typ.	17	mV	6)

Noise output power (volume control at minimum)

	P_N	typ.	20	nW	7)
--	-------	------	----	----	----

Typical overall fidelity (flat within 3 dB)

	200 Hz to 6	kHz	8)
--	-------------	-----	----

Open loop voltage gain

	G_v	typ.	60	dB
--	-------	------	----	----

1) Aerial e. m. f. (V_i) at $f_o = 100$ MHz; $R_S = 50$ Ω (source resistance; see page 12)
 $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz.2) $f_o = 10,7$ MHz; $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz.3) A.M. signal: $m = 0,3$; $f_m = 400$ Hz (carrier simultaneously modulated with a.m. and f.m.).

4) Including ratio detector.

5) $f_o = 100$ MHz; $\Delta f = \pm 40$ kHz; $f_m = 1$ kHz.6) Measured at 1 kHz, a negative feedback of 15 dB and a loudspeaker of 8 Ω ; $V_P = 9$ V.7) Measured at a bandwidth of 200 Hz to 6 kHz, pin 13 being connected via a capacitor of 32 μF to pin 16; loudspeaker impedance 8 Ω .

8) Depending on values of capacitors C51 and C55, 50 Hz to 15 kHz is possible.

COIL DATA See also circuit on pages 6 and 7.

1. A.M.-I.F. coils ($f_o = 452$ kHz)

First i. f. bandpass filter

Primary : L14 = 38 μ H
 $C_p = 3300$ pF
 $Q_0 = 90$

Secondary : L15 (N_1) = 125 μ H
 $C_p = 1000$ pF
 $Q_0 = 80$
 $N_1/N_2 = 18$
 $k_{QL14-L15} = 1$

Single tuned coil

L17 (N_1) = 125 μ H
 $C_p = 1000$ pF
 $Q_0 = 80$
 $N_1/N_2 = 30$

Detector coil

L13 (N_1+N_2) = 0,84 mH
 $C_p = 150$ pF
 $Q_0 = 130$
 $N_1/N_2 = 3,1$
 $(N_1+N_2)/N_3 = 4$

2. F.M.-I.F. coils ($f_o = 10,7$ MHz)

First i. f. bandpass filter

Primary : L4 (N_1) = 2,6 μ H
 $C_p = 82$ pF
 $Q_0 = 90$
 $N_1/N_2 = 10$

First single tuned filter

L8 (N_1) = 1,44 μ H
 $C_p = 150$ pF
 $Q_0 = 45$
 $N_1/N_2 = 5,7$

Second single tuned filter

L16 (N_1) = 1,44 μ H
 $C_p = 150$ pF
 $Q_0 = 45$
 $N_1/N_2 = 5,7$

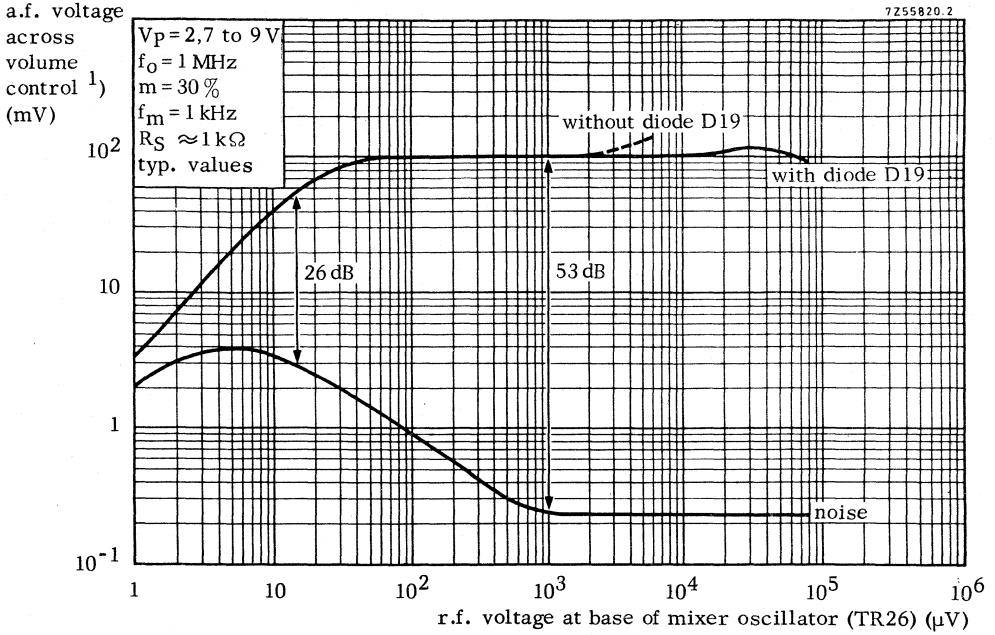
Secondary : L5 (N_1) = 1,44 μ H
 $C_p = 150$ pF
 $Q_0 = 55$
 $N_1/N_2 = 5,7$
 $k_{QL4-L5} = 1,2$

Ratio detector

Primary : L10 (N_1) = 1,44 μ H
 $C_p = 150$ pF
 $Q_0 = 95$
 $N_1/N_2 = 2$

Secondary : L12 (N_1+N_2) = 2,6 μ H
 $C_p = 82$ pF
 $Q_0 = 110$
 $N_1/N_2 = 1$
 $(N_1+N_2)/N_3 = 5,4$
 $k_{QL10-L12} = 0,7$

APPLICATION INFORMATION (continued)

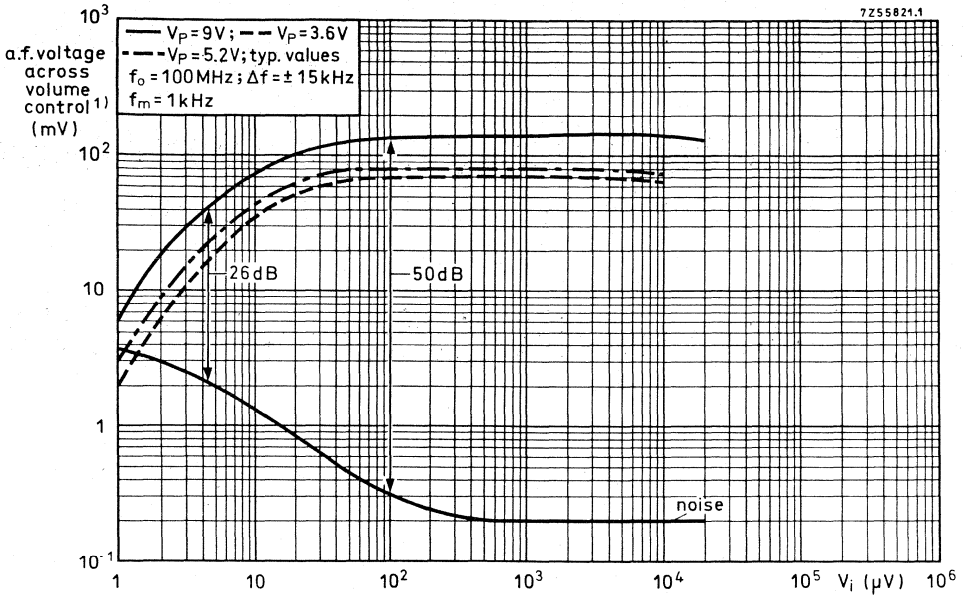


Typical a.g.c. curves at a.m. reception

A. F. voltages across volume control versus r. f. voltage at base of mixer-oscillator.

1) Slider at lower end.

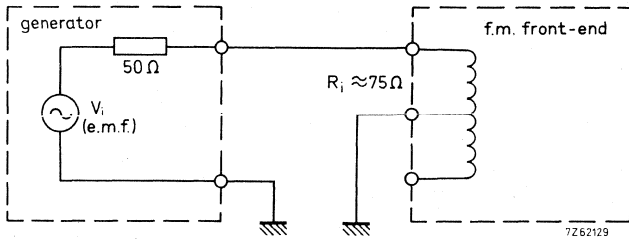
APPLICATION INFORMATION (continued)



Typical S/N curves at f.m. reception

A.F. voltage across volume control versus aerial e.m.f. represented by the generator voltage V_i (e.m.f.) connected to the 75Ω input of the f.m. front-end.

Test circuit



¹⁾ Slider at lower end.

F.M. STEREO DECODER

The TCA290A is a high quality monolithic integrated f. m. stereo decoder based on matrix decoding (frequency multiplexing).

The circuit provides automatic mono/stereo switching depending on both the pilot signal and the field strength and directly energizes a stereo indicator lamp. An external connection for mono/stereo switching is also available.

QUICK REFERENCE DATA

Supply voltage (pin 7)	V_p	nom.	15 V
Ambient temperature	T_{amb}		25 °C

Distortion	d_{tot}	typ.	0, 2 %
Cross-talk at $f = 1$ kHz	α	>	40 dB
19 kHz suppression	α_{19}	> typ.	30 dB 35 dB
38 kHz suppression	α_{38}	> typ.	36 dB 40 dB

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages

Supply voltage	V ₇₋₁₆	max. 18 V
Indicator lamp voltage	V ₁₁₋₁₆	max. 28 V ¹⁾
Switching voltage mono/stereo	V ₁₃₋₁₆	max. 3 V

Currents

Indicator lamp current (d. c.)	I ₁₁	max. 100 mA
Indicator lamp turn-on current (peak value)	I _{11M}	max. 200 mA

Dissipation

Total power dissipation	P _{tot}	max. 500 mW
-------------------------	------------------	-------------

Temperatures

Storage temperature	T _{stg}	-55 to +125 °C
Operating ambient temperature	T _{amb}	-30 to +80 °C

CHARACTERISTICS at T_{amb} = 25 °C; V₇₋₁₆ = 15 V.

<u>Input MPX voltage</u> (peak-to-peak value)	V _{14-16(p-p)}	typ. 1 V
<u>Input resistance</u> (pin 14)	R _i	> 50 kΩ
<u>Output resistance</u> (pins 9 and 10)	R _o	typ. 5.6 kΩ
<u>Distortion</u> at f = 1 kHz; V _{9-16(rms)} = 1 V; V _{10-16(rms)} = 1 V	d _{tot}	typ. 0.2 %
<u>Voltage gain</u> defined as: $\frac{V_{9-16}}{V_{14-16}}$; $\frac{V_{10-16}}{V_{14-16}}$ at V _{14-16(p-p)} = 1 V	G _v	typ. 3 2,5 to 4
<u>Pilot-tone threshold switching voltage</u> (r. m. s. value) at stereo "ON"	V _{14-16(rms)}	typ. 18 mV 14 to 22 mV

Switching voltage

to mono	V ₁₃₋₁₆	> 1,3 V
to stereo	V ₁₃₋₁₆	< 0,8 V
hysteresis		> 0,2 V

Total current (excluding indicator lamp)

I _{tot}	typ. 20 mA
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Cross-talk at f = 1 kHz

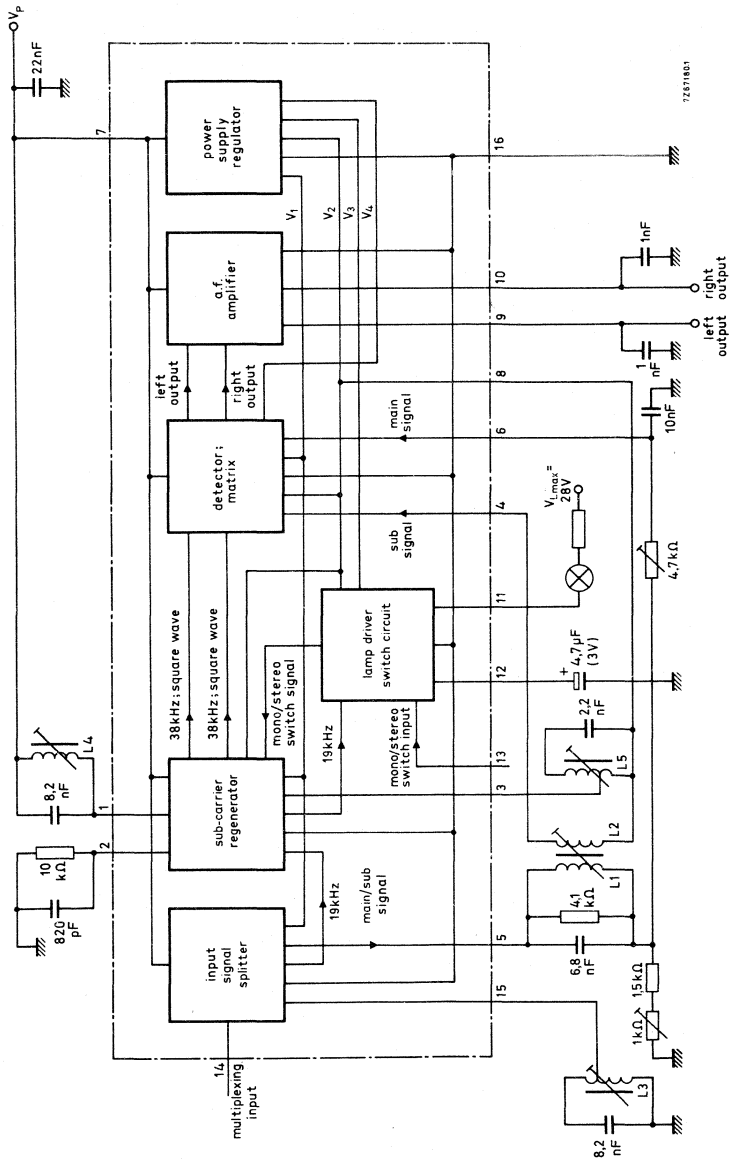
α	> 40 dB
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Ultra-sonic frequency rejection

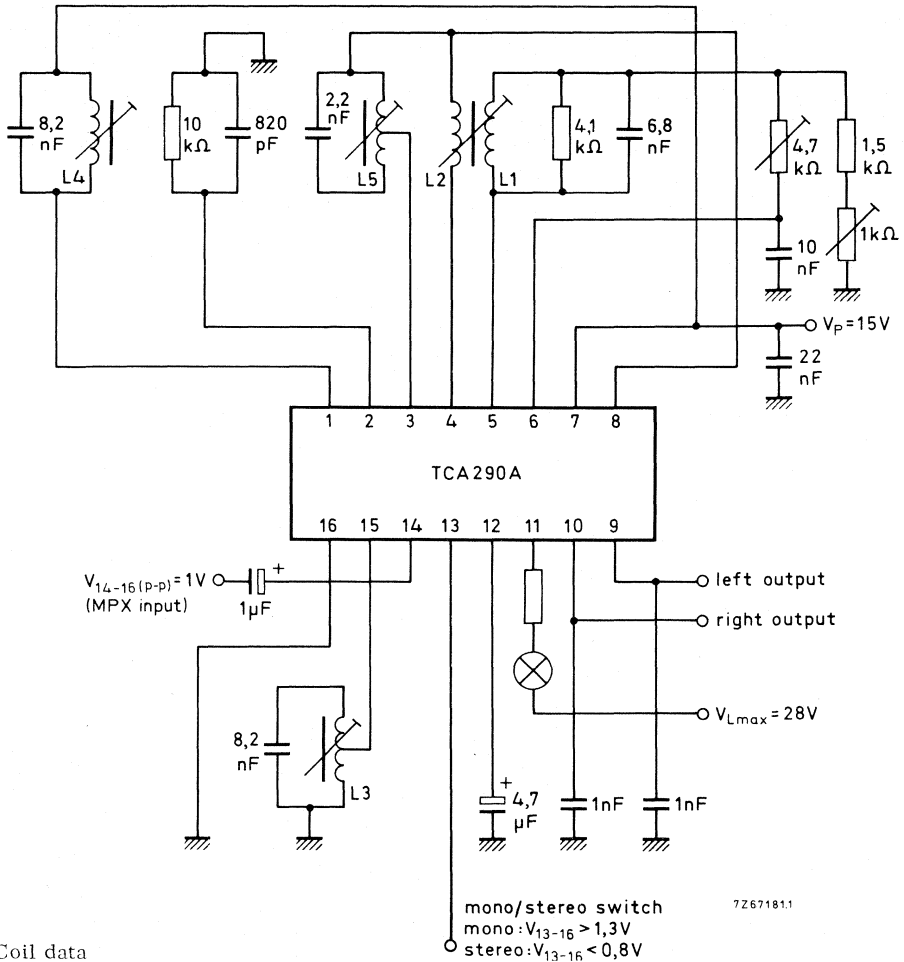
at 19 kHz	α ₁₉	> 30 dB typ. 35 dB
at 38 kHz	α ₃₈	> 36 dB typ. 40 dB
at 57 kHz	α ₅₇	> 45 dB

¹⁾ Measured in test circuit on page 3.

CIRCUIT DIAGRAM



APPLICATION INFORMATION

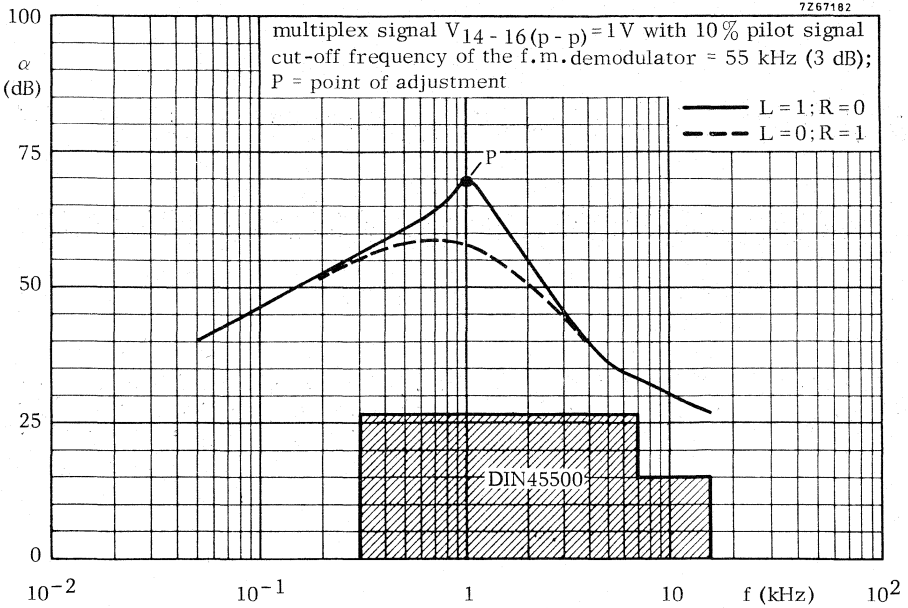


Coil data

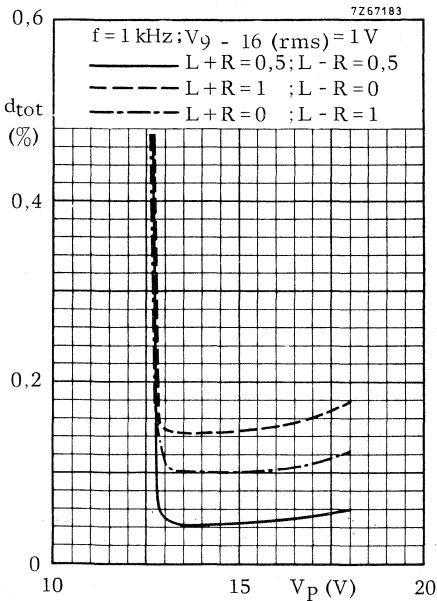
- L1: 290 turns 0,1 mm e. c. wire
- L2: 220 turns 0,1 mm e. c. wire (wound around L1) } Bandwidth: 6, 36 kHz
- L3: 520 turns 0,1 mm e. c. wire (tapped at 130 turns from ground); $Q_0 \approx 50$
- L4: 520 turns 0,1 mm e. c. wire; $Q_0 \approx 50$
- L5: 520 turns 0,1 mm e. c. wire (tapped at 60 turns from pin 8); $Q_0 \approx 80$

All coils wound on:

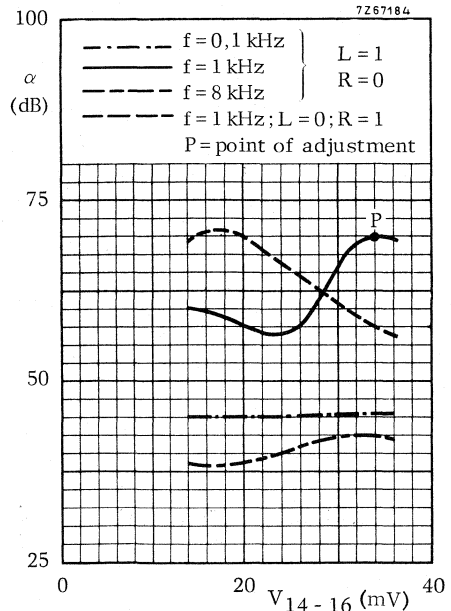
- coil former : 4312 021 29650
- window 3D3 : 4322 020 37030
- screw core 3D3 : 4312 020 32150



Damping of cross-talk versus audio frequency.



Total harmonic distortion versus supply voltage.



Damping of cross-talk versus the 19 kHz input signal.

I.F. AMPLIFIER

The TCA420A is a monolithic integrated i.f. amplifier for hi-fi f.m. receivers combining the following functions:

- f.m. -i.f. amplifier
- symmetrical f.m. detector
- a.f.c. voltage
- mono/stereo switching voltage
- field-strength depending indicator current
- automatic (adjustable) side response suppression

QUICK REFERENCE DATA

Supply voltage	V_P	typ.	15	V
Ambient temperature	T_{amb}	typ.	25	$^{\circ}C$
Frequency	f_0		10,7	MHz

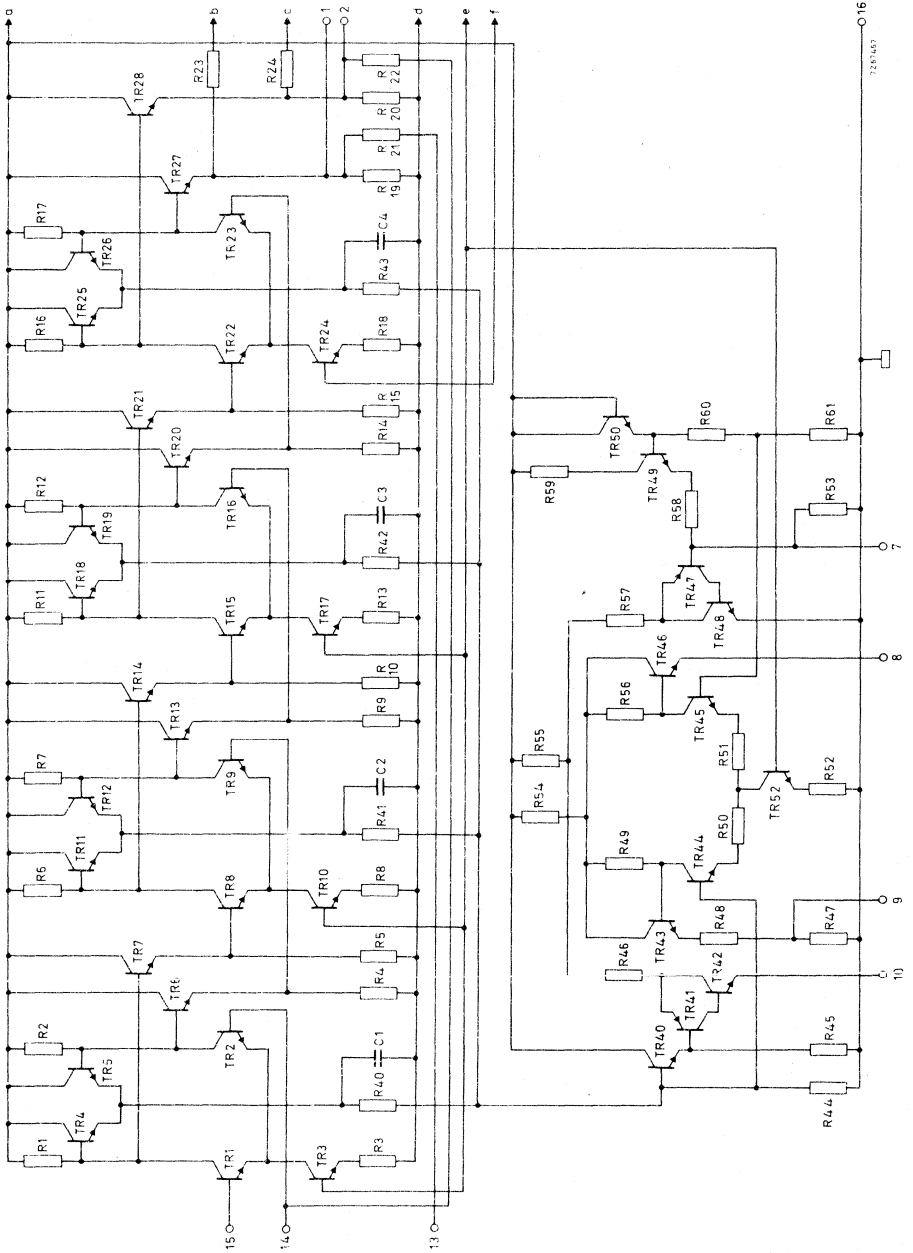
Input limiting voltage (-3 dB)	V_{ilim}	typ.	35	μV
A.F. output voltage at $\Delta f = \pm 15$ kHz	V_{6-16}	typ.	115	mV
A. M. rejection at $\Delta f = \pm 15$ kHz; $m = 0,3$; $f_m = 1$ kHz; $V_i = 10$ mV	α	typ.	50	dB
Centre shift of f.m. detector curve at input voltage variation of 1 mV to 30 μV	$ f_{01} - f_{02} $	typ.	7	kHz
I.F. voltage gain	G_V	typ.	65	dB

PACKAGE OUTLINE (see general section)

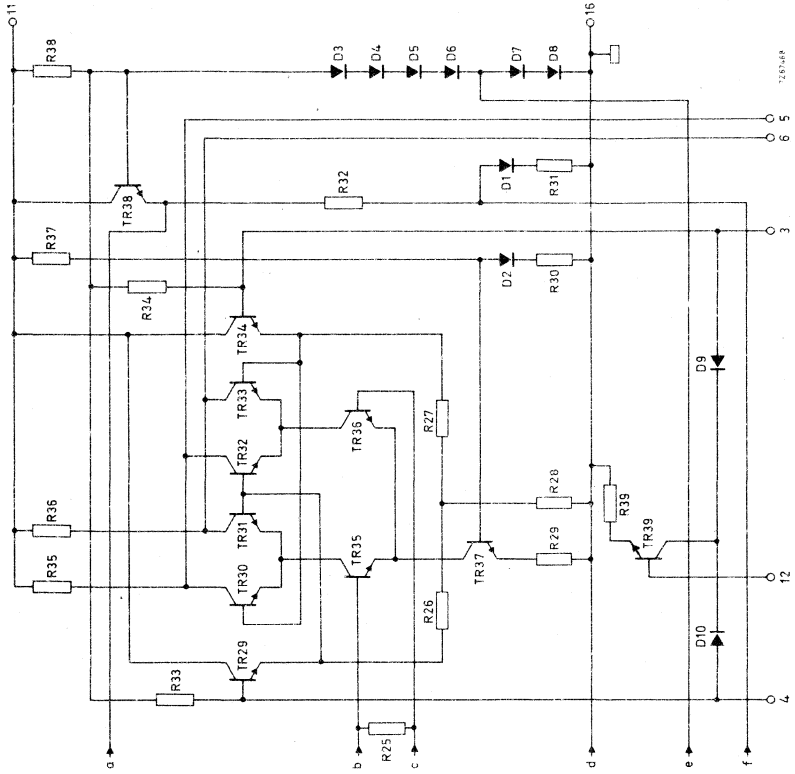
16-lead DIL; plastic.

TCA420A

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage (pin 11) $V_P = V_{11-16}$ max. 18 V

Current

Total current I_{11} max. 40 mA

Power dissipation

Total power dissipation P_{tot} max. 720 mW

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} -25 to +80 °C

CHARACTERISTICS at $V_P = 15$ V; $T_{amb} = 25$ °C; see circuit on page 7.

Output voltages (d.c. value) (pins 5 and 6) V_{5-16} } typ. 9,5 V
 V_{6-16} } 8,3 to 11 V

Voltage difference (d.c. value) (pins 5 and 6)

at $V_i = 1$ mV ΔV_{5-6} < 350 mV

Current

I_{11} typ. 26 mA
 < 35 mA

Input limiting voltage (-3 dB; $R_1 = 5$ k Ω ; pin 5)

V_i lim typ. 35 μ V
 < 50 μ V

APPLICATION INFORMATION measured in the circuit on page 7 at following conditions:

$f_o = 10,7$ MHz; $V_P = 15$ V; $T_{amb} = 25$ °C; measured after adjustment to minimum distortion at: $V_i = 1$ mV, $\Delta f = \pm 75$ kHz, $f_m = 1$ kHz, $R_1 = 5$ k Ω and $C_{5-6} = 220$ pF; a.c. values are measured on recommended printed circuit board on page 6.

A.F. output voltage

$\Delta f = \pm 15$ kHz V_{6-16} > 95 mV
 typ. 115 mV

Total distortion at $f_m = 1$ kHz

$\Delta f = \pm 75$ kHz d_{tot} typ. 0,8 %
 < 1,2 %

$\Delta f = \pm 40$ kHz d_{tot} typ. 0,3 %
 $\Delta f = \pm 15$ kHz d_{tot} typ. 0,2 %

APPLICATION INFORMATION (continued)

A. M. rejection ¹⁾

f. m. signal: $\Delta f = \pm 15$ kHz; $f_m = 70$ Hz

a. m. signal: $m = 30\%$; $f_m = 1$ kHz; $V_i = V_{5-16}$

at $V_i = 0, 3$ mV	α	>	40	dB
at $V_i = 1, 0$ mV	α	>	40	dB
at $V_i = 10$ mV	α	} typ.	45	dB
at $V_i = 100$ mV	α		50	dB
		>	40	dB

Signal to noise ratio

reference signal: $f_o = 10, 7$ MHz; $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz

noise signal : $f_o = 10, 7$ MHz; without modulation

filter : $B(3 \text{ dB}) = 250$ Hz to 16 kHz

at $V_i = 100$ mV	S/N	>	60	dB
at $V_i = 20$ μ V	S/N	typ.	26	dB

Centre shift of f. m. detector curve ²⁾

f. m. signal: $\Delta f = \pm 50$ kHz; $f_m = 70$ Hz

a. m. signal: $m = 85\%$; $f_m = 1$ kHz

$ f_{o1} - f_{o2} $	typ.	7	kHz
	<	15	kHz

I. F. voltage gain

G_V	typ.	65	dB
-------	------	----	----

I. F. limited output voltages (peak-to-peak value) ³⁾

$V_i = 5$ mV; $f = 1$ MHz	$V_{1-16(p-p)} = V_{2-16(p-p)}$	>	250	mV
		typ.	350	mV

Input voltage levels for obtaining the required output voltages for switching a stereo decoder from mono to stereo vice-versa. These values are adjustable and the published levels are optimized for the TCA290A, where:

- switching voltage to mono > 1, 3 V
- switching voltage to stereo < 0, 8 V

Input voltage for $V_{10-16} = 0, 8$ V

after adjusting R1, so $V_{R1} = 1, 3$ V at $V_i = 0$	V_i	typ.	1, 3	mV
			0, 5 to 1, 75	mV

Input voltage for $V_{10-16} = 1, 3$ V

after adjusting R1, so $V_{R1} = 0, 8$ V at $V_i = 3$ mV	V_i	typ.	80	μ V
		<	200	μ V

1) The interfering signal is measured with filter ($B(3 \text{ dB}) = 700$ Hz to 5 kHz).

2) Defined as difference between frequency f_{o1} at $V_i = 1$ mV and frequency f_{o2} at $V_i = 30$ μ V. The frequencies f_{o1} and f_{o2} at equal voltages V_{5-6} .

3) Detector circuit not connected. Loads between pins 1-16 and 2-16 are equal: 10 M Ω in parallel with 8 pF.

APPLICATION INFORMATION (continued)

Field-strength indicator current

adjust R2 so $I_9 = 0$ at $V_i = 0$; R3 = 0;
 measured at $V_i = 120$ mV; $R_{\text{indicator}} = 2$ k Ω

I_9	>	140	μA
	typ.	200	μA

Input voltage for 10 dB side response suppression

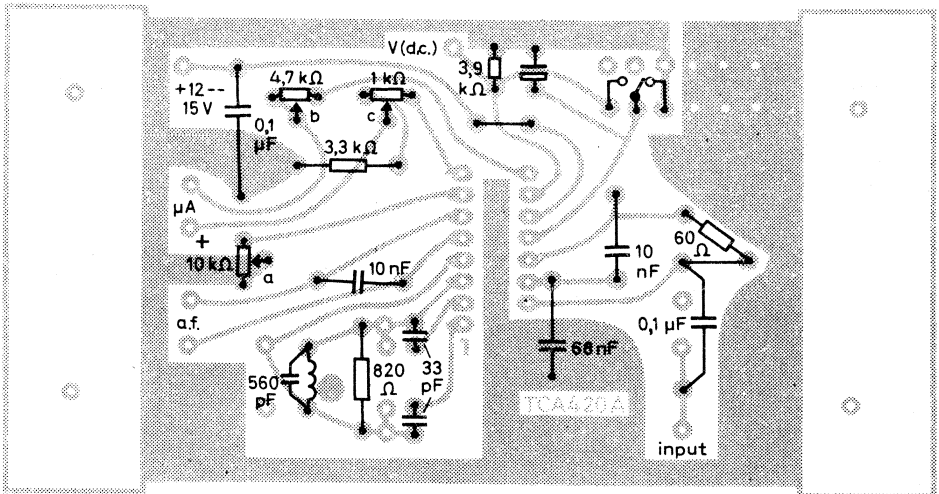
at S1 = "on"
 adjust R1, so $V_{10-16} = 1,3$ V at $V_i = 0$, S1 = "off"

V_i	typ.	40	μV
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Output signal muting at S2 = "on"

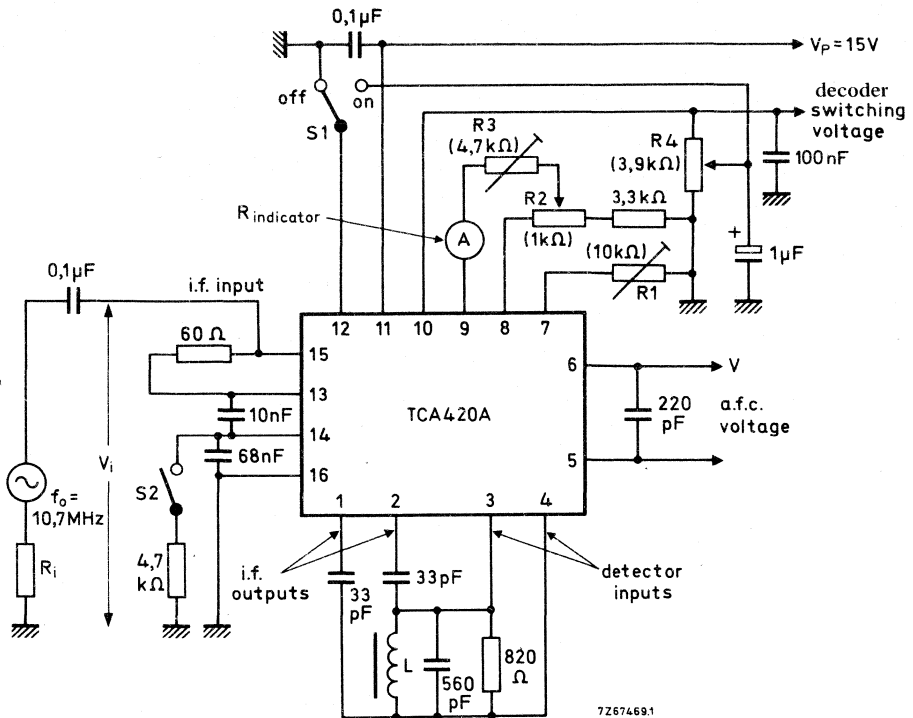
reference signal at S2 = "off": $V_i = 1$ mV, $f_m = 1$ kHz
 $\Delta f = \pm 75$ kHz

ΔV_o	>	60	dB
--------------	---	----	----



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TEST CIRCUIT



Notes

- V₁₁₋₁₆ : supply voltage
- V₁₀₋₁₆ : switching voltage for stereo decoder (field strength dependent)
- R₁ : pre-set potentiometer for adjusting necessary output voltage V₁₀₋₁₆
- R₂ : pre-set potentiometer for adjusting the zero level of the field strength indicator current
- R₃ : pre-set potentiometer for adjusting the maximum level of the field strength indicator current
- R₄ : pre-set potentiometer for adjusting the side response suppression
- S₁ : side response suppression switch
- S₂ : output signal muting switch.

MAGNETIC FIELD DETECTOR USING HALL EFFECT

The TCA450A is a monolithic integrated circuit for magnetic field detection. It incorporates a Hall element and a differential amplifier the output stages of which form a long-tailed pair.

The differential voltage generated by the Hall element depends on the density and the polarity of the magnetic flux to be detected.

The minimum available output current of the differential amplifier is 50 mA at saturation.

The circuit can be used for commutation in brushless motors, tachogenerators, measuring probes (field strength; current), speed and position detectors.

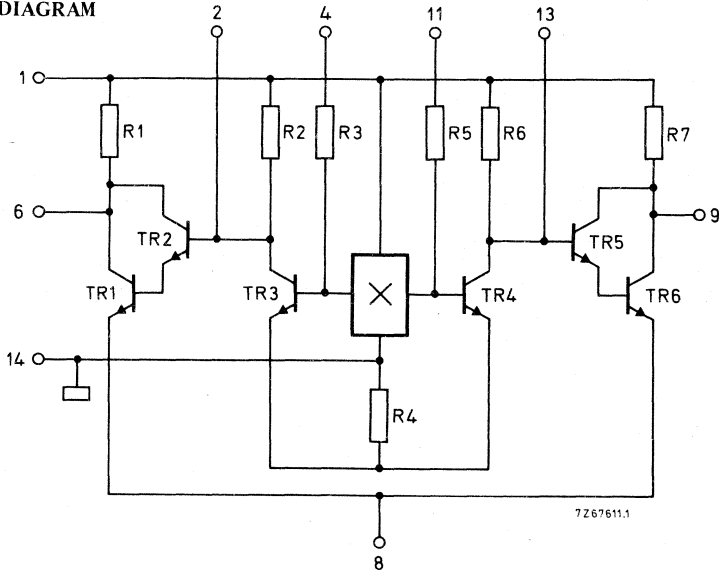
QUICK REFERENCE DATA

Supply voltage	V_P	4 to 16	V
Operating ambient temperature	T_{amb}	-55 to +125	°C
Output current at pins 6 or 9 $V_P = 8\text{ V}; -I_E = 2\text{ mA}$	$I_6; I_9$	max. 50	mA
Magnetic sensitivity of Hall element		typ. 0, 4	V/T *)
Offset flux density	$\pm B_{offset}$	typ. 7, 5 < 20	mT *) mT
Voltage gain of the amplifier	$\frac{V_{2-13}}{V_{4-11}}$	typ. 15	
Mutual conductance of the amplifier	$\frac{I_6 - I_9}{V_{4-11}}$	$ g_m $ typ. 240	mA/V
*) 1 T (Tesla) = 1 Wb/m ² = 10 ⁴ Gs			

PACKAGE OUTLINE (see general section)

14-lead; plastic (SOT-43).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to pins 14 and 8

V_P max. 18 V

Output current at pins 6 or 9

$I_6; I_9$ max. 50 mA

Power dissipation

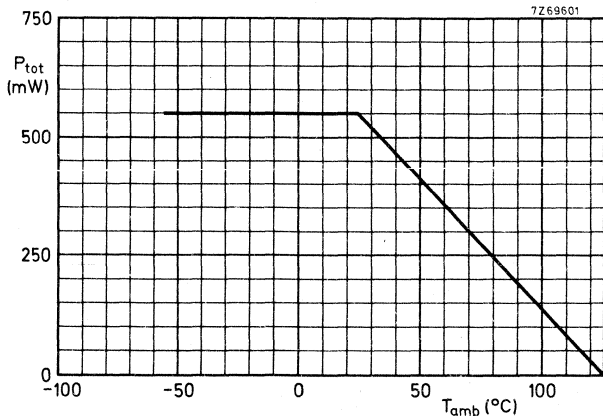
See derating curve below

Storage temperature

T_{stg} - 55 to +125 °C

Operating ambient temperature

T_{amb} - 55 to +125 °C



Note: IC mounted on printed-circuit board.

CHARACTERISTICS All voltages with respect to pin 14; all currents positive into IC.

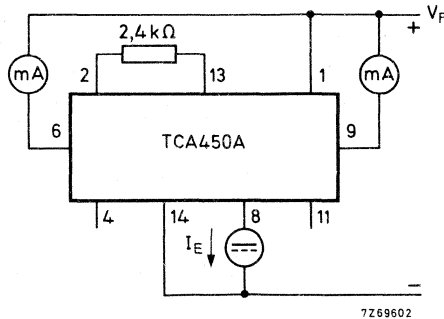
Supply voltage	V_{1-14}	typ.	8 V	4 to 16 V
Output current at pins 6 and 9	$I_6 + I_9$	<	50 mA	
The following characteristics are measured in test circuit below. $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{1-14} = 8\text{ V}$; $I_E = -2\text{ mA}$; unless otherwise specified.				
Offset flux density of the Hall element	$\pm B_{offset}$	typ.	7,5 mT	20 mT ¹⁾
Magnetic sensitivity of the Hall element		typ.	0,4 V/T	¹⁾
Voltage gain of the amplifier	$\frac{V_{2-13}}{V_{4-11}}$	typ.	15	
Mutual conductance of the amplifier	$I_6 - I_9 / V_{4-11}$	$ g_m $	typ.	240 mA/V ²⁾
Offset flux density in balanced condition	$I_6 = I_9$	$\pm B_{offset}$	<	20 mT ¹⁾
Required flux density for 1 : 10 current ratio	I_6 / I_9 or I_9 / I_6	$\pm B$	<	25 mT ¹⁾
Collector resistors of the output stage	R_{6-1} ; R_{9-1}	typ.	1000 Ω	800 to 1200 Ω

Note

Output 6 is conducting when the reference side of the integrated circuit is directed towards the north pole of the magnetic field.
 Output 9 is conducting when the reference side is directed to the south pole of the magnetic field.
 All specified magnetic fields are homogeneous and applied perpendicular to the contact plane.

TEST CIRCUIT

pins 3, 5, 10 and 12 are not connected;
 pin 7 is internally connected

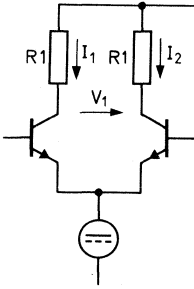


1) 1 T (Tesla) = 1 Wb/m² = 10⁴ Gs.

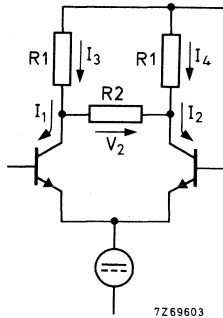
2) Without 2,4 k Ω resistor in application circuit, the expected value will be 5 times better.

APPLICATION INFORMATION

In the circuit diagram below, a resistor of 2,4 kΩ and an extra RC-filter are connected between pins 2 and 13, which reduce the gain of the voltage amplifier (see formulas).



$$V_1 = (I_2 - I_1)R_1$$



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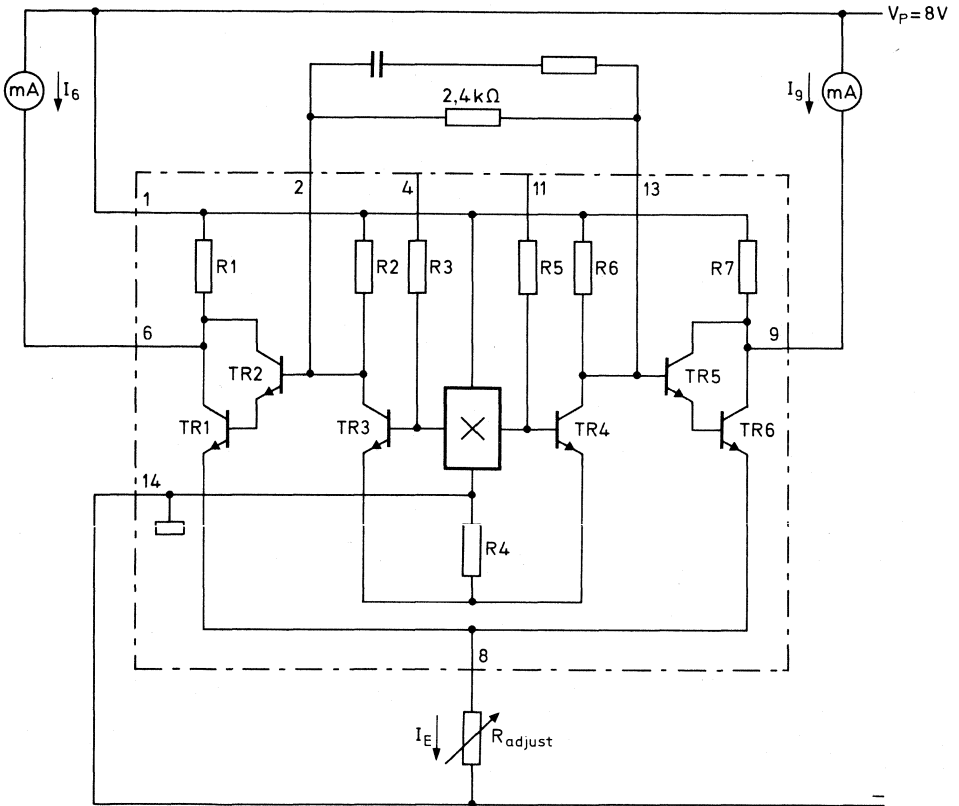
$$I_3R_1 + V_2 - I_4R_1 = 0$$

$$I_3 = I_1 + \frac{V_2}{R_2} \text{ and } I_4 = I_2 - \frac{V_2}{R_2}$$

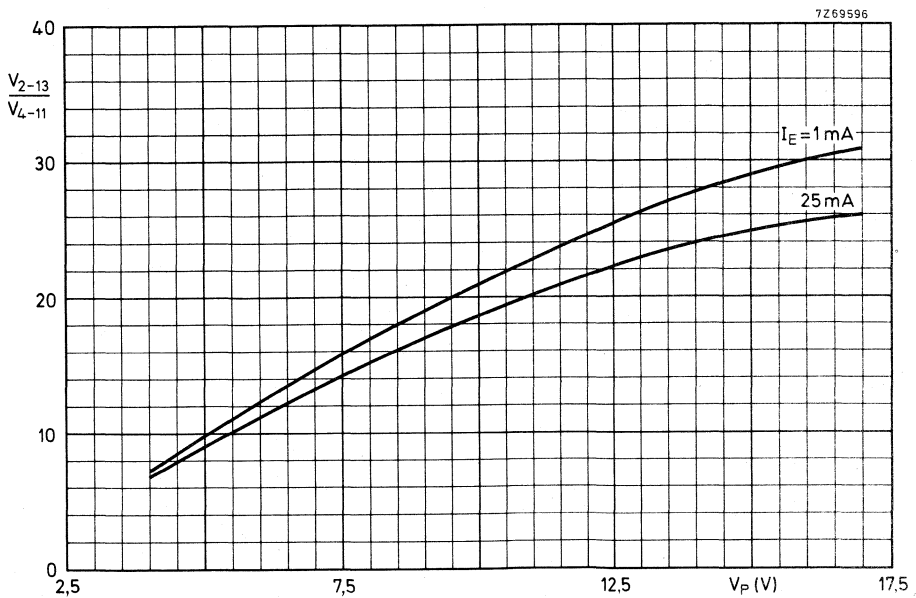
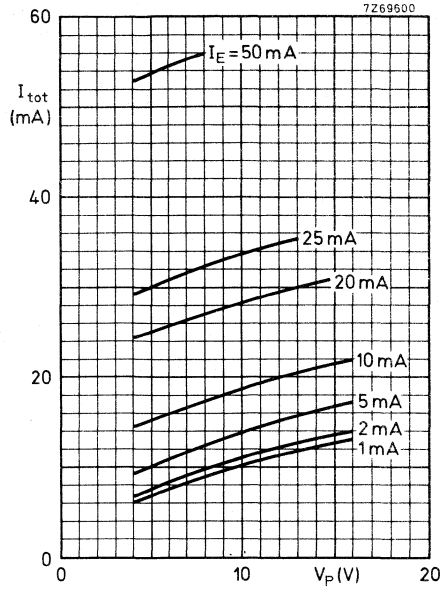
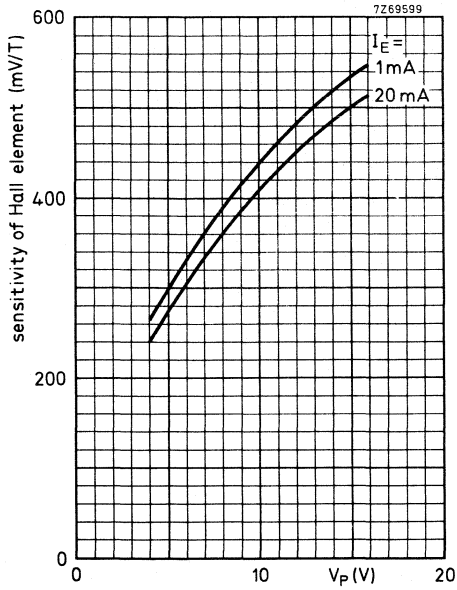
$$I_1R_1 + \frac{R_1}{R_2}V_2 + V_2 - I_2R_1 + \frac{R_1}{R_2}V_2 = 0$$

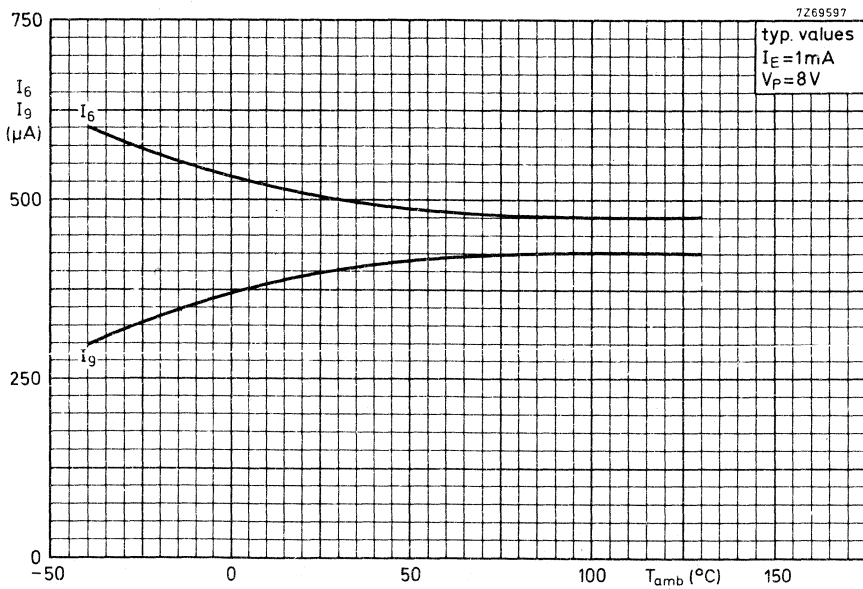
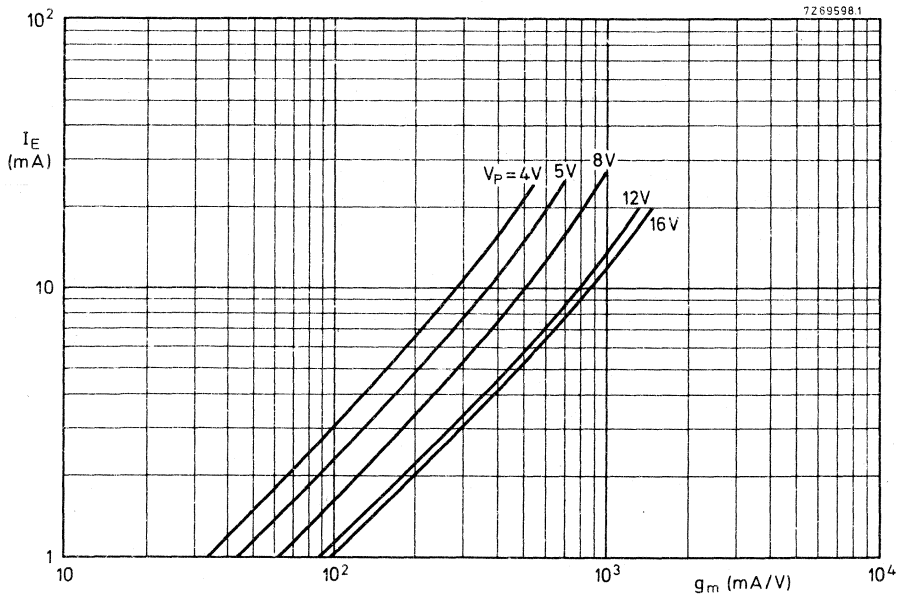
$$V_1 + (1 + 2\frac{R_1}{R_2})V_2 = 0$$

$$\frac{V_1}{V_2} = 1 + 2\frac{R_1}{R_2}$$



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INTEGRATED VOLTAGE STABILIZER

The TCA530 is an adjustable 30 V integrated circuit voltage stabilizer for use with variable capacitance diodes.

The circuit features: continuous short-circuit protected output, a. f. c. control voltage input, internal switch-on delay (can be adjusted externally), pre-stabilization and crystal temperature control (temperature sensor and heater).

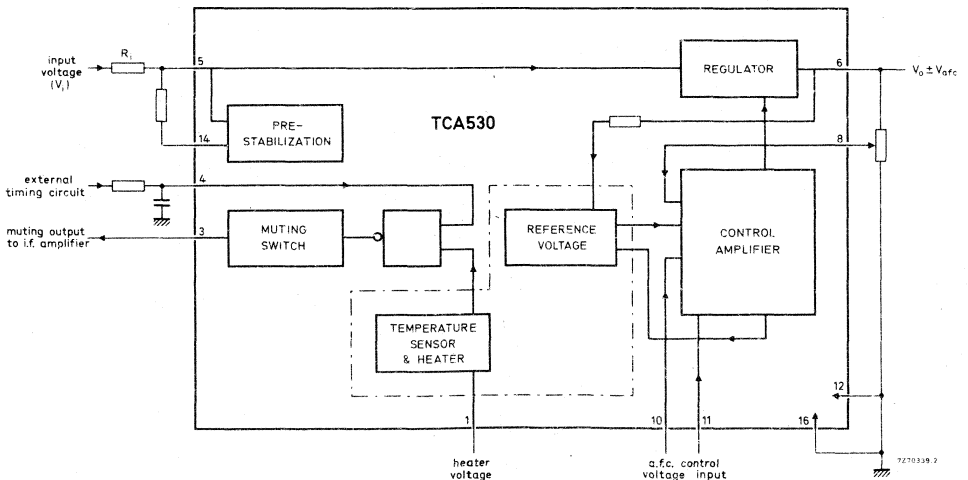
QUICK REFERENCE DATA

Input voltage range	V_i	50 to 68 V
Output voltage	V_{6-16} typ.	30 V
Amplitude range of output voltage for a. f. c.	ΔV_{6-16} typ.	$\pm 0,75$ V
Variation of output voltage as a function of:		
input voltage	typ.	0,2 mV/V
temperature	typ.	0,1 mV/°C
output current	typ.	0,5 mV/mA
heater voltage	typ.	0,2 mV/V
Operating ambient temperature range	T_{amb}	-20 to +80 °C

PACKAGE OUTLINE (see general section)

Plastic 16-lead dual in-line.

BLOCK DIAGRAM



TCA530

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Supply voltage: pin 1	V_{1-16}	max.	20 V
pin 3 (muting switch supply)	V_{3-16}	max.	15 V ¹⁾
A.F.C. input control voltages: pin 10 and 11	$V_{10-16} = V_{11-16}$	max.	15 V
pin 10	V_{10-11}	max.	6 V

Currents

Input currents: pin 5	I_5	max.	25 mA
pin 8	I_8	max.	500 μ A
pin 14	I_{14}	max.	15 mA
pin 4	I_4	max.	500 μ A
pin 3	I_3	max.	5 mA
pin 1	I_1	max.	300 mA

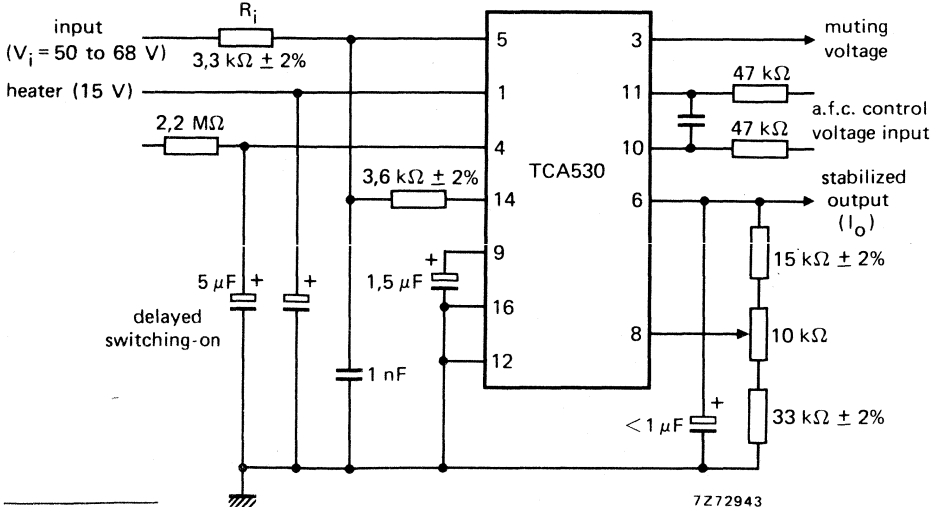
Power dissipation

Total power dissipation (excluding heater power) at $T_{amb} = 60^\circ\text{C}$	P_{tot}	max.	500 mW
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Temperatures

Storage temperature	T_{stg}	-25 to +125 $^\circ\text{C}$
Operating ambient temperature	T_{amb}	-20 to +80 $^\circ\text{C}$

CHARACTERISTICS at $V_{6-16} = 30\text{ V}$; $V_{10-16} = V_{11-16} = 10\text{ V}$; $V_{1-16} = 15\text{ V}$;
 $T_{amb} = 25^\circ\text{C}$



¹⁾ $V_{3-16} < 20\text{ V}$ if the application circuit corresponds to the circuit above.

CHARACTERISTICS (continued)

Input voltage range at $R_i = 3, 3 \text{ k}\Omega$	V_i	50 to 68	V
Minimum input voltage at pin 5	V_{5-16}	>	32,5 V
Maximum input voltage	V_i	depends on value of R_i	
Heater voltage range	V_{1-16}	8 to 20	V
Heater current at $V_{1-16} = 15 \text{ V}$	I_1	typ.	40 mA
Heater peak current when switched on	I_{1M}	typ.	230 mA
		<	300 mA
Stabilization time up to $\pm 150 \text{ mV}$ of final value at $V_{1-16} = 15 \text{ V}$	t_s	<	2 s
Switch-on delay on pin 3 without external capacitor	t_d	<	3 s ¹⁾
Output current (start of current limiting)	I_6	<	8 mA
Amplitude range of output voltage for a. f. c.	$\pm \Delta V_{6-16}$	<	1 V
Ratio of regulated output voltage to input control voltage	$\Delta V_{6-16} / \Delta V_{10-11}$	typ.	1, 2:1
		muting	on off
Switching voltage	V_{4-16}	<	8 8 to 11 V
Switching current	I_4	typ.	1 > 0,1 μA
Saturation voltage on pin 3 at $I_3 = 500 \mu\text{A}$	$V_{3-16\text{sat}}$	<	0,5 V
Reference voltage	V_{8-16}	typ.	20 V
		18, 2 to 21, 8	V
Common mode input voltage range of the control amplifier	$V_{10-16} = V_{11-16}$	6 to 18	V
Control input current	$I_{10}; I_{11}$	typ.	0,1 μA
Control input resistance	R_{10-11}	>	1 $\text{M}\Omega$
Common mode rejection ratio	CMRR	typ.	60 dB

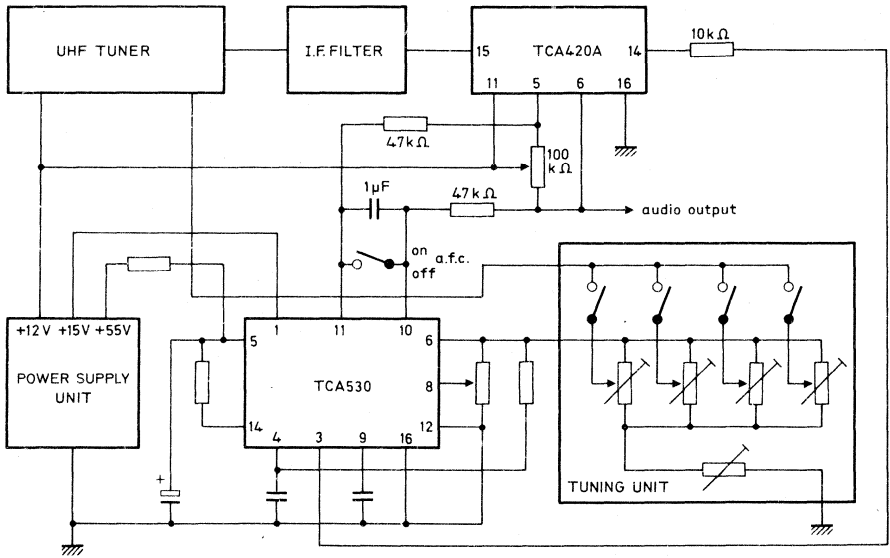
¹⁾ Can be increased by RC circuit.

CHARACTERISTICS (continued)

Hum suppression at $f > 30$ Hz	typ.	60 dB
Output noise voltage at $f = 10$ to $15\,000$ Hz (r. m. s. value)	<	50 μ V
Variation of output voltage as function of input voltage	$\Delta V_{6-16}/\Delta V_{5-16}$	typ. 0,2 mV/V
temperature	$\Delta V_{6-16}/\Delta T_{amb}$	typ. 0,1 mV/ $^{\circ}$ C
output current	$\Delta V_{6-16}/\Delta I_6$	typ. 0,5 mV/mA
heater voltage	$\Delta V_{6-16}/\Delta V_{1-16}$	typ. 0,2 mV/V

APPLICATION INFORMATION

F. M. receiver with TCA530 and TCA420A



D.C. VOLUME AND BALANCE CONTROL CIRCUIT

The TCA730 is a monolithic integrated circuit for controlling volume and balance in stereo amplifiers by means of a d.c. voltage.

It also incorporates an externally switchable physiological volume control.

Performance exceeds the DIN45 500 specifications.

QUICK REFERENCE DATA

Supply voltage	V_{8-15}	typ.	15 V
Ambient temperature	T_{amb}	typ.	25 °C

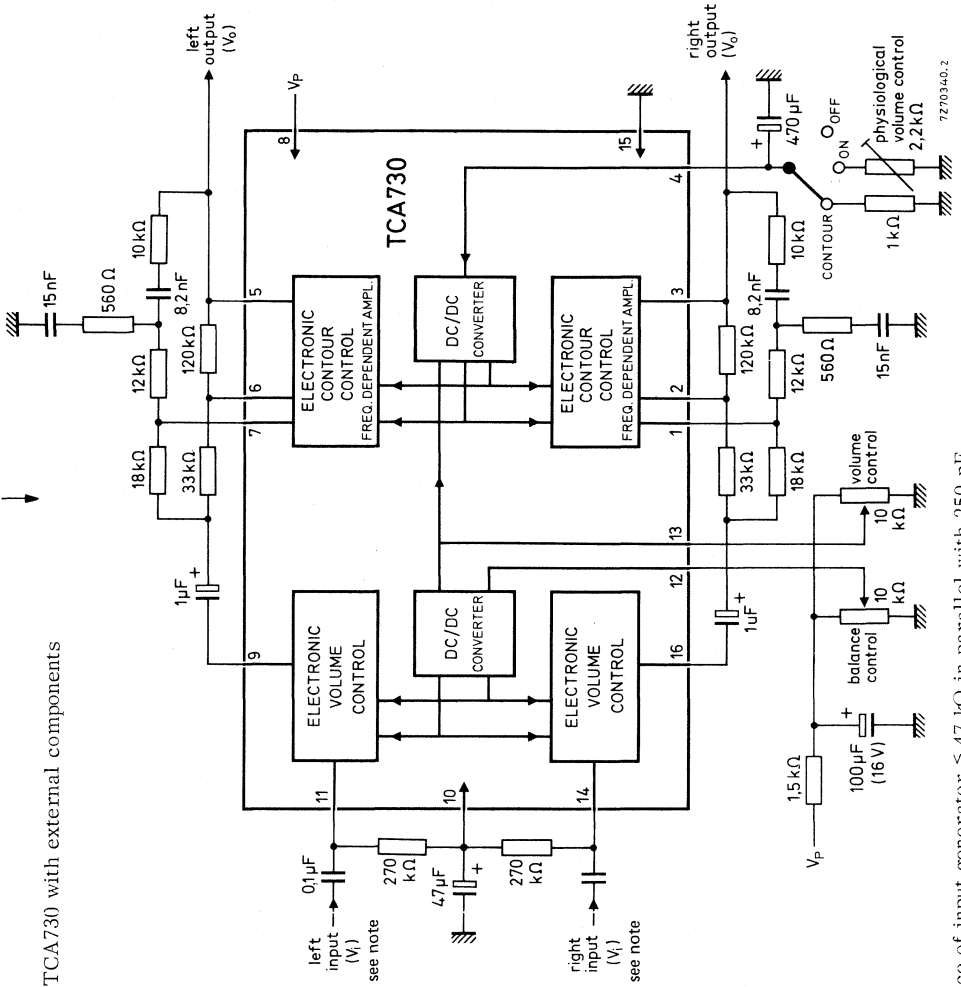
Volume control range at $V_i = 100$ mV			+20 to -70 dB
Distortion at $V_{o(rms)} = 1$ V	d_{tot}	typ.	0,1 %
Balance control range			±10 dB
Input voltage	V_i	<	1 V
Input impedance with external resistor of 270 kΩ	$ Z_{i1} $	typ.	250 kΩ
Load resistance	R_L	>	4,7 kΩ
Output voltage	V_o	<	1 V
Channel separation		typ.	60 dB
Signal-to-noise ratio	S/N	typ.	57 dB
Frequency response (±1 dB)			20 Hz to 20 kHz
Channel balance		typ.	2 dB

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

TCA730

BLOCK DIAGRAM of TCA730 with external components



Note: series impedance of input generator ≤ 47 kΩ in parallel with 250 pF.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages

Pin No. 8 voltage	V_{8-15}	max.	18 V
Pin No. 12 voltage	V_{12-15}	max.	12 V
Pin No. 13 voltage	V_{13-15}	max.	12 V
Pin No. 4 voltage	V_{4-15}	max.	3 V

Total power dissipation

P_{tot}	max.	860 mW
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Temperatures

Storage temperature	T_{stg}	-20 to +125 °C
Operating ambient temperature	T_{amb}	-20 to +60 °C

CHARACTERISTICS at $V_{8-15} = 15 V$; $T_{amb} = 25 °C$; $f = 1 kHz$ (unless otherwise specified)

Measured in circuit on page 2.

Supply voltage range

V_{8-15}	13, 5 to 16, 5 V
------------	------------------

Supply current

I_8	typ.	30 mA
	<	40 mA

Voltage gain

V_o/V_i	0 to +20 dB
-----------	-------------

Voltage attenuation

V_o/V_i	0 to -70 dB
-----------	-------------

Input resistance

$R_{11-15} = R_{14-15}$	>	3 MΩ
-------------------------	---	------

Input impedance with external

resistor of 270 kΩ between pins 11-10, 14-10

$ Z_i $	typ.	250 kΩ
---------	------	--------

D.C. input current

$I_{11} = I_{14}$	<	2 μA
-------------------	---	------

Output voltage

$V_i = 100 mV$ to 1 V

V_o	typ.	1 V
-------	------	-----

Frequency response (-1 dB)

without physiological volume control

20 Hz to 20 kHz

CHARACTERISTICS (continued)

Distortion

$V_o/V_i = +20$ to $+10$ dB; $V_{o(rms)} = 1$ V

d_{tot} typ. 0,1 %
 < 0,2 %

$V_o/V_i = +10$ to 0 dB; $V_{o(rms)} = 1$ V

d_{tot} typ. 0,3 %
 < 0,5 %

$V_o/V_i = 0$ to -50 dB; $V_{i(rms)} = 1$ V

d_{tot} typ. 0,3 %
 < 0,5 %

$V_o/V_i = -50$ to -70 dB; $V_{i(rms)} = 1$ V

d_{tot} typ. 0,5 %
 < 1,0 %

Channel separation at $V_{o(rms)} = 1$ V

$f = 250$ Hz to $12,5$ kHz

> 56 dB
 typ. 60 dB

$f = 20$ Hz to 20 kHz

> 46 dB
 typ. 50 dB

Channel balance (without physiology)

$V_o/V_i = 0$ to -50 dB

typ. 1 dB
 < 2 dB

$V_o/V_i = -50$ to -70 dB

typ. 2 dB
 < 4 dB

Balance control range

$V_o/V_i = 0$ to -50 dB

± 10 dB

Signal/noise ratio at $f = 20$ Hz to 20 kHz

$V_{i(rms)} = 100$ mV; $V_{o(rms)} = 50$ mV

S/N > 52,5 dB
 typ. 57 dB

Control voltage range

volume control

V_{13-15} 1 to 9 V

balance control

V_{12-15} 1 to 9 V

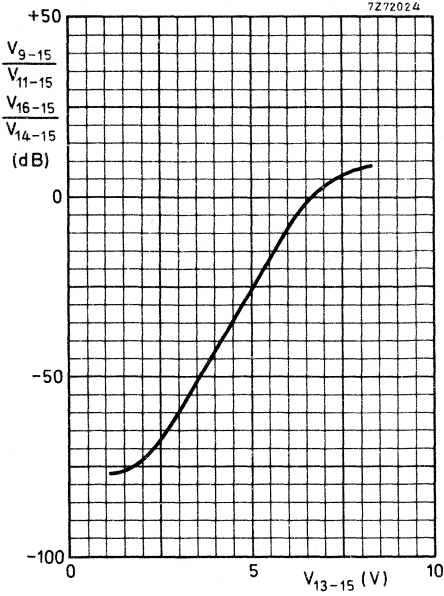
Control current

at $V_{13-15} = 8$ V

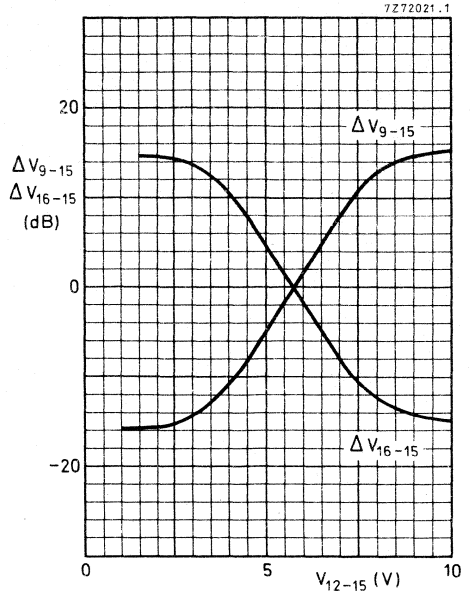
I_{13} < 50 μ A

at $V_{12-15} = 8$ V

I_{12} < 25 μ A

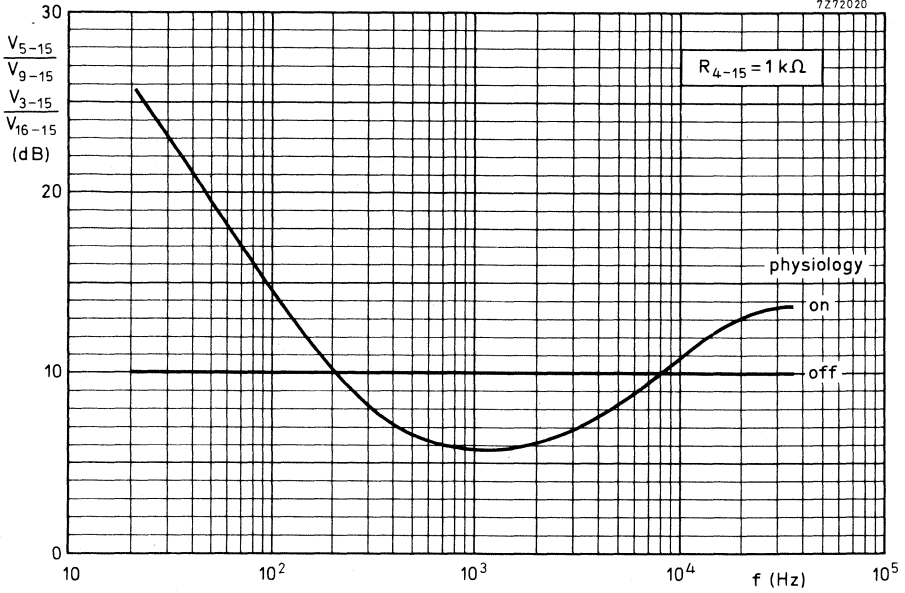


Volume control curve without physiology at $f = 1$ kHz



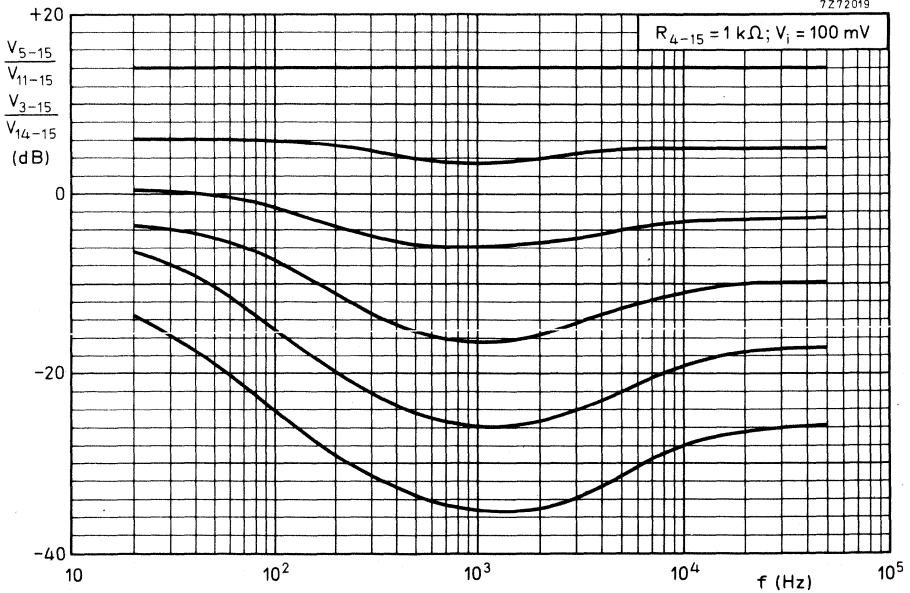
Balance control curve at $f = 1$ kHz

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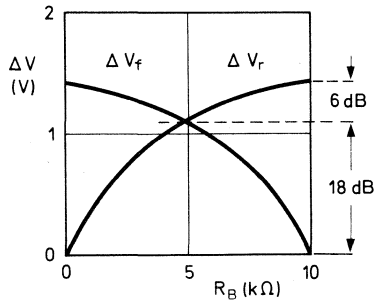
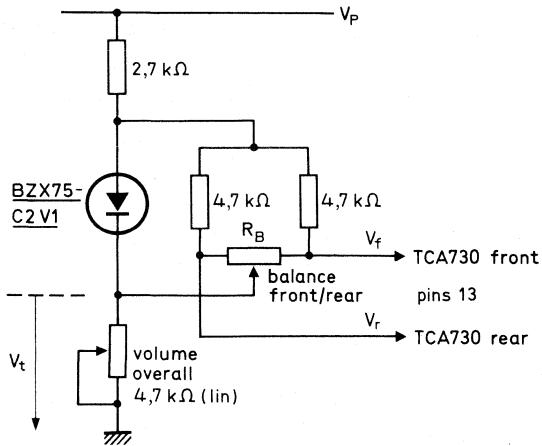
Physiological voltage gain versus frequency (measured in the circuit on page 2)

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Physiological volume control (measured in the circuit on page 2)

Balance control (front/rear) at quadrophonic amplification



$$V_f = V_t + \Delta V_f$$

$$V_r = V_t + \Delta V_r$$

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D.C. TONE CONTROL CIRCUIT

The TCA740 is a monolithic integrated circuit for controlling bass and treble in stereo amplifiers by means of a d.c. voltage.

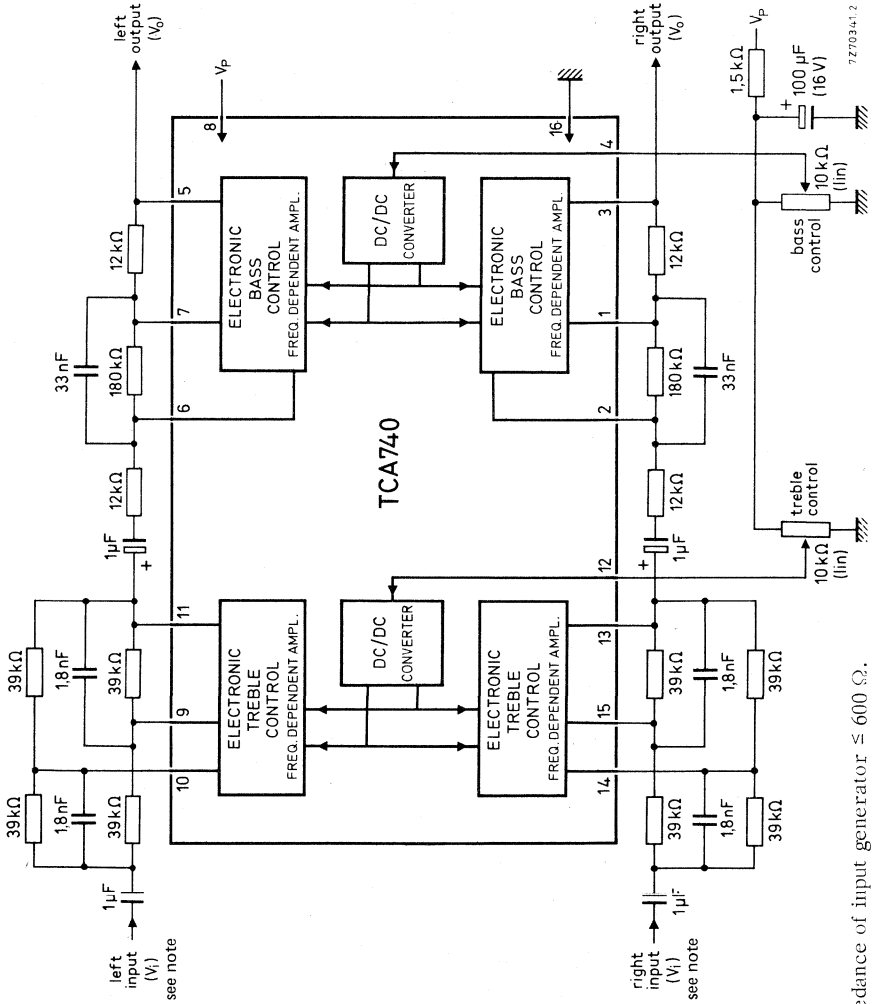
QUICK REFERENCE DATA			
Supply voltage	V_{8-16}	typ.	15 V
Ambient temperature	T_{amb}	typ.	25 °C

Bass boost		>	14 dB ←
Bass cut		>	14 dB ←
Treble boost		>	14 dB ←
Treble cut		>	14 dB ←
Distortion at $V_{o(rms)} = 1\text{ V}$	d_{tot}	typ.	0.1 %
Signal-to-noise ratio	S/N	typ.	60 dB
Channel separation		typ.	60 dB

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

BLOCK DIAGRAM of TCA740 with external components



Note: series impedance of input generator $\leq 600 \Omega$.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages

Pin 8 voltage	V_{8-16}	max.	18	V
Pin 4 voltage	V_{4-16}	max.	12	V
Pin 12 voltage	V_{12-16}	max.	12	V
<u>Total power dissipation</u>	P_{tot}	max.	860	mW

Temperatures

Storage temperature	T_{stg}	-20 to +125	°C
Operating ambient temperature	T_{amb}	-20 to +60	°C

CHARACTERISTICS at $V_{8-16} = 15$ V; $T_{amb} = 25$ °C (unless otherwise specified)

Measured in circuit diagram on page 2

<u>Supply voltage range</u>	V_{8-16}	13,5 to 16,5	V
-----------------------------	------------	--------------	---

<u>Supply current</u>	I_8	typ.	30	mA
		<	40	mA

<u>Voltage gain at linear frequency response</u>	V_o/V_i	typ.	0	dB
--	-----------	------	---	----

Voltage gain at $f = 1$ kHz

at maximum bass/treble boost	V_o/V_i	typ.	+1,5	dB
at maximum bass/treble cut	V_o/V_i	typ.	-1,5	dB

Bass boost at $V_{4-16} = 10$ V

$f = 40$ Hz (ref. 1 kHz)	>	14	dB	←
--------------------------	---	----	----	---

Treble boost at $V_{12-16} = 10$ V

$f = 15$ kHz (ref. 1 kHz)	>	14	dB	←
---------------------------	---	----	----	---

Bass cut at $V_{4-16} = 1$ V

$f = 40$ Hz (ref. 1 kHz)	>	14	dB	←
--------------------------	---	----	----	---

Treble cut at $V_{12-16} = 1$ V

$f = 15$ kHz (ref. 1 kHz)	>	14	dB	←
---------------------------	---	----	----	---

Signal-to-noise ratio

$f = 20$ Hz to 20 kHz; $V_o(rms) = 50$ mV	S/N	>	56,5	dB
		typ.	60	dB

Distortion at linear frequency response

$f = 1$ kHz; $V_o(rms) = 1$ V	d	typ.	0,1	%
		<	0,2	%

CHARACTERISTICS (continued)

Channel separation at $V_o(\text{rms}) = 1 \text{ V}$

$f = 250 \text{ Hz to } 12,5 \text{ kHz}$		>	56	dB
		typ.	60	dB
$f = 20 \text{ Hz to } 20 \text{ kHz}$		>	46	dB
		typ.	50	dB

Input impedance without external components

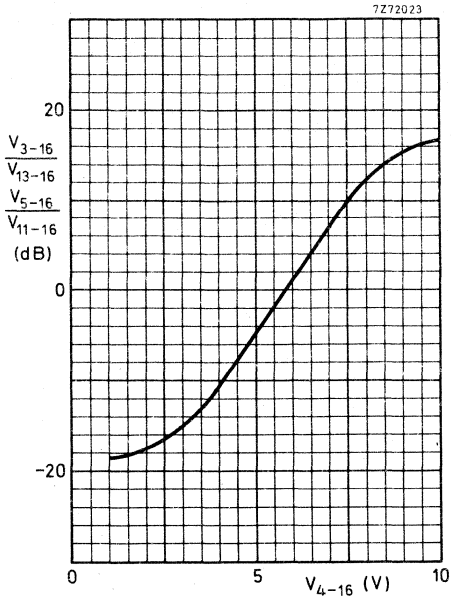
at pins 1, 2, 6, 7, 9, 10, 14 and 15	$ Z_i $	>	1	$\text{M}\Omega$
--------------------------------------	---------	---	---	------------------

D.C. input current

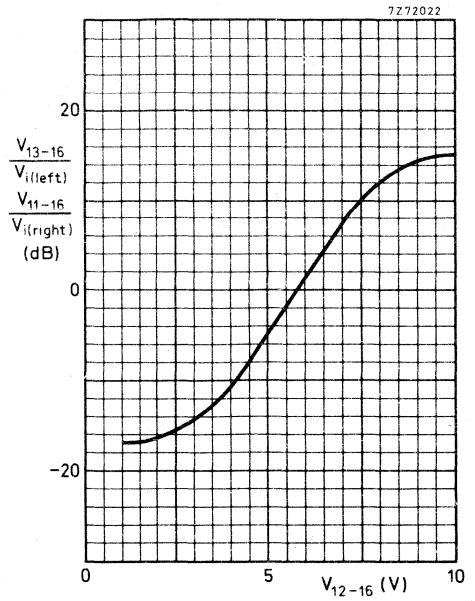
at pins 1, 2, 6, 7, 9, 10, 14 and 15	I_i	<	2	μA
--------------------------------------	-------	---	---	---------------

Control current

at $V_{12-16} = 8 \text{ V}$	I_{12}	<	25	μA
at $V_{4-16} = 8 \text{ V}$	I_4	<	25	μA



Bass control curve at $f = 40$ Hz



Treble control curve at $f = 15$ kHz

MULTI-STABILIZER FOR ELECTRONIC TUNING

The TCA750 is basically a stabilizer for use in electronic tuning systems.

The circuit is combined with an external reference diode which **entirely** determines the thermal stability of the system and can be adapted to the stability requirements of AM, FM or TV receivers.

The reference diode BZV38 used in conjunction with the TCA750 form an ideal pair for FM tuners in radio or TV receivers.

Additional to a stabilized voltage (V_{O1}) for the electronic tuning system, the TCA750 incorporates two other output voltages (V_{O2} and V_{O3}) for stabilized supply of the entire receiver combination as well as the following attractive features :

- The output current of any of the three stabilizers can be increased by a discrete power transistor without affecting circuit stability.
- For mute control at switching on, V_{O2} can be delayed by external components.
- An a. f. c. coupling circuit provides a constant correction factor by superimposing an a. f. c. voltage on V_{O1} .
- Adjustable a. f. c. amplification factor (< 5).
- Pulse or touch contact operation switches off the a. f. c. whilst changing stations.
- Delayed switching on of the a. f. c. , externally adjustable ($t_d < 2$ s).
- Search tuning becomes very simple when using the a. f. c. current source (pin 10).
- All three stabilized outputs are protected against short circuit and are **individually** adjustable.

QUICK REFERENCE DATA see page 2

PACKAGE OUTLINE (see general section)

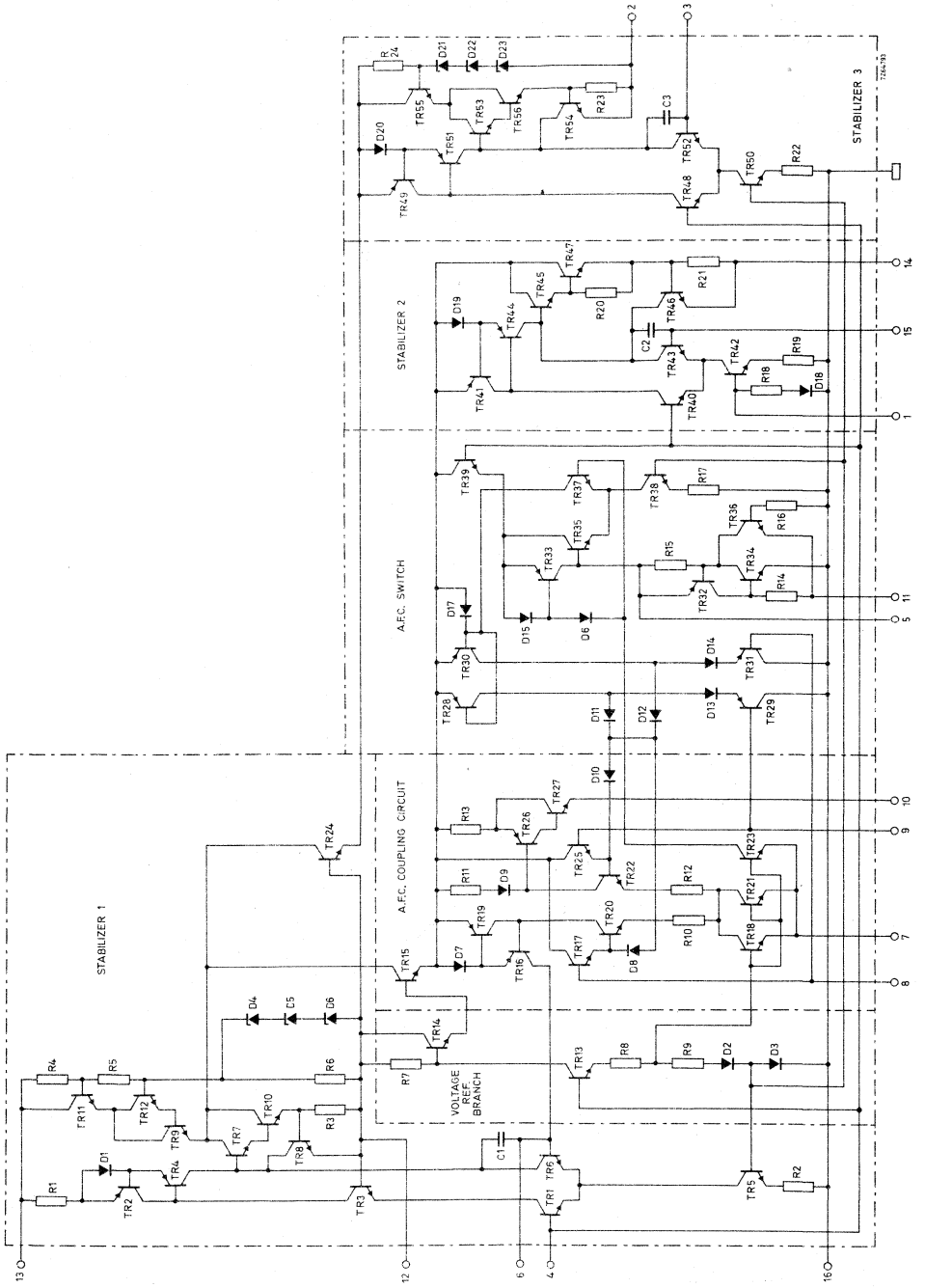
16-lead DIL; plastic.

QUICK REFERENCE DATA

Input voltage range	V_{13-16}	26, 5 to 54	V
Ambient temperature	T_{amb}	typ. 25	°C
Input voltage	V_{13-16}	typ. 45	V
Tuning voltage (V_{O1})*	V_{12-16}	21 to 31	V
Output current (I_{1})*	I_{12}	< 14, 5	mA
Stabilizing time	t_{stab}	typ. 0, 8	s
Temperature coefficient (V_{O1})	TCA750 BZV38	$\Delta V_{O1}/\Delta T$	typ. 1 ppm/°C typ. 30 ppm/°C
Line regulation		$\Delta V_{O1}/\Delta V_{in}$	typ. 10 ppm/V
Output voltage (V_{O2})*	V_{14-16}	8 to 18	V
Output current (I_{2})*	I_{14}	< 6	mA
Output voltage (V_{O3})*	V_{2-16}	8 to 26	V
Output current (I_{3})*	I_2	< 6	mA

* Symbols used in test circuit on page 5.

CIRCUIT DIAGRAM



TCA750

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Input voltage (supply)	V_{13-16}	max.	54 V
A. F. C. input voltages (pins 8 and 9)	V_{8-16}, V_{9-16}	max.	17 V
	$\pm V_{8-9}$	max.	6 V

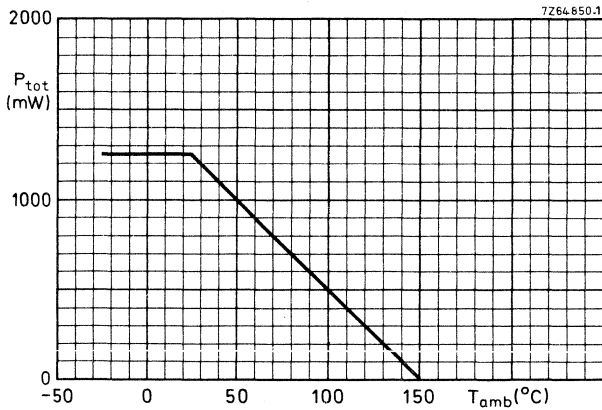
Currents

Output current: pin 12	I_{12}	max.	55 mA
pin 14	I_{14}	max.	20 mA
pin 2	I_2	max.	25 mA
Input current (pin 11)	$\pm I_{11}$	max.	6 mA

Temperatures

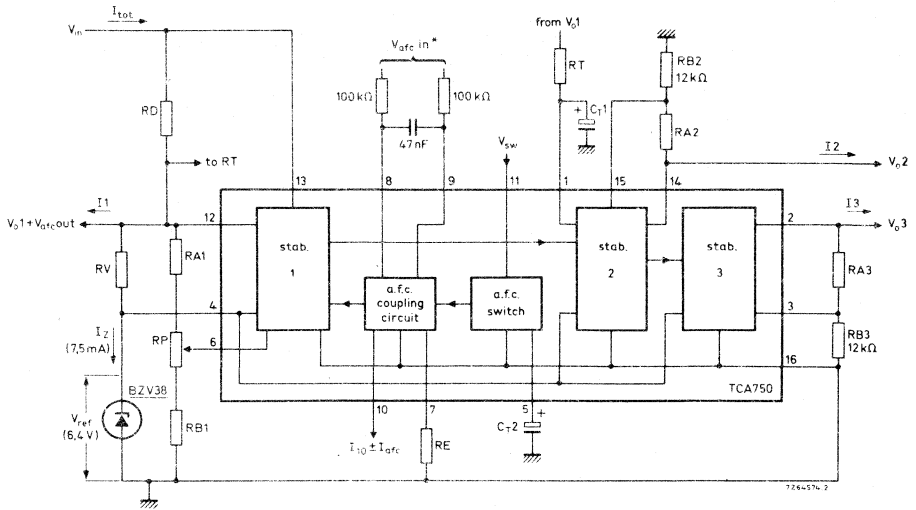
Storage temperature	T_{stg}	-55 to +150 °C
Operating ambient temperature	T_{amb}	-25 to +150 °C ¹⁾

Power dissipation



¹⁾ See power derating curve.

TEST CIRCUIT



*) $V_{afc\ in}$ is superimposed on a common-mode voltage (V_{com}) of 5 V to 17 V.

Multi-stabilizer peripheral components

Note to power reduction resistor RD

For worst case conditions (max. output currents of the three stabilizers and a high supply voltage V_{in}) the power dissipation (P_{tot}) must be reduced by the use of the external resistor RD.

$$\text{Power reduction} = \frac{(V_{in} - V_{o1})^2}{RD}$$

The minimum permissible value of RD is derived by the formula

$$RD_{min} = \frac{V_{in\ max} - V_{o1} - V_{afc\ out}}{I_{12} - I_{13\ min}}$$

where,

$$I_{13\ min} = 4,5\ \text{mA (stand-by current } I_S)$$

$$I_{12} = I_Z + I_{RA1} + I_{11\ min}$$

CHARACTERISTICS and APPLICATION INFORMATION (see test circuit on page 5) at $T_{amb} = 25\text{ }^{\circ}\text{C}$

Supplies		Note	Min.	Typ.	Max.	Unit
Input voltage	V_{in}	1	26, 5	-	54	V
Input current	I_{tot}	2	-	-	31	mA
Output characteristics						
D.C. output resistance (all stabilizers)	R_{out}	-	-	1	-	Ω
Permissible output short-circuit duration	t_{short}	-	-	-	-	-
stabilizer 1		-	continuous	-	-	-
stabilizers 2 or 3		-	-	-	10	s
Stabilizer 1						
Output voltage range (adjustable)	V_{O1}	3	21	-	31	V
Output current	I_1	4, 5	0	-	5	mA
Stabilizing time	t_{stab}	6	-	-	1	s
Output voltage temp. coefficient	$\Delta V_{O1}/\Delta T$	7, 8	-	40	-	ppm/ $^{\circ}\text{C}$
Line regulation	$\Delta V_{O1}/\Delta V_{in}$	8	-	10	-	ppm/V
A.F.C. coupling circuit						
A.F.C. input voltage ($\frac{1}{2} V_{afc}$ swing)	V_{afc} in	-	-	-	5	V
A.F.C. output voltage ($\frac{1}{2} V_{afc}$ lim swing)	V_{afc} lim	15, 16	-	0, 9	-	V
A.F.C. output current threshold	I_{10}	15, 16	-	-	1, 5	mA
A.F.C. output current swing	I_{afc} lim	15, 16	-	-	3, 0	mA
A.F.C. off delay	t_d	-	-	2	-	s
Amplification factor	μ	-	-	-	5	-
A.F.C. slope ($\Delta I_{afc}/\Delta V_{afc}$ in)	S	14	-	2, 5	-	mA/V
Common-mode voltage	V_{com}	9	5	-	17	V
V_{O1} change due to a.f.c. switching	$\Delta V_{O1}/afc$	-	-	-	25	mV
Asymmetry of a.f.c. input (a.f.c. off)	$\pm(I_8 - I_9)$	-	-	-	0, 5	μA
A.F.C. switch operated by manual switch						
Input voltage (a.f.c. on)	V_{sw}	-	-0, 5	-	+0, 5	V
Positive input voltage (a.f.c. off)	$+V_{sw}$	-	0, 8	-	6	V
Negative input voltage (a.f.c. off)	$-V_{sw}$	-	0, 8	-	-	V
Positive input current (a.f.c. off)	$+I_{11}$	-	0, 004	-	3	mA
Negative input current (a.f.c. off)	$-I_{11}$	-	0, 8	-	2	mA
A.F.C. switch operated by pulse						
Positive trigger pulse peak current	$+I_{11}$ pulse	13	-	-	-	-
pulse width = 10 μs		-	800	-	3000	μA
100 μs		-	80	-	3000	μA
1 ms		-	8	-	3000	μA
10 ms		-	4	-	3000	μA
Negative trigger pulse peak current	$-I_{11}$ pulse	-	0, 8	-	2	mA
Negative trigger pulse width		-	10	-	-	μs

CHARACTERISTICS and APPLICATION INFORMATION (continued)

Stabilizer 2

		Note	Min.	Typ.	Max.	Unit
Output voltage range (adjustable)	V_{O2}	10	8	-	18	V
Output current	12	5	0	-	5,5	mA
Output voltage temp. coefficient	$\Delta V_{O2}/\Delta T$	7, 8	-	45	-	ppm/°C
Switch-on delay time	t_{don}	11	0	-	6	s
Switching voltage	V_{1-16}	-	0, 8	-	1	V

Stabilizer 3

Output voltage range (adjustable)	V_{O3}	12	8	-	26	V
Output current	13	5	0	-	5,5	mA
Output voltage temp. coefficient	$\Delta V_{O3}/\Delta T$	7, 8	-	45	-	ppm/°C

Notes (also from page 6)

1. The V_{in} range depends on the value of V_{O1} (see Fig. 1).
2. At $I_1 = 5$ mA, $I_2 = I_3 = 5,5$ mA, $I_{10} = 0$.
3. Adjustable by means of RA1, RB1 and RP.
4. If a higher level is required from the output of stabilizer 1, the reference diode supply may be obtained from the emitter of a power transistor connected to the output from stabilizer 3 (see Fig. 5). In this case, the current available from stabilizer 1 is increased to 12,5 mA (bleeder current $I_{RA1} = 2$ mA).
5. At $T_{amb} = 60$ °C max. with all stabilizers at rated currents.
6. With V_{O1} within 0,05% of its steady value.
7. Temperature coefficient at T_{amb} from 10 °C to 60 °C with V_{in} constant, and using metal film bleed resistors having a temperature coefficient of ≤ 50 ppm/°C.
8. With all stabilizer output currents constant and within the specified limits.
9. Common-mode voltage = voltage between pins 8 and 16, and 9 and 16 of the IC.
10. V_{O2} depends on the value of V_{O1} (see Fig. 3); adjustable with RA2.
11. Adjustable by means of RT and CT1. The delay time is limited by the leakage current of CT1.
12. V_{O3} depends on the value of V_{O1} (see Fig. 4); adjustable with RA3.
13. The delay time after triggering depends on the value of CT2.
14. With RE = 10 k Ω and $T_{amb} = 25$ °C.
15. V_{afc} out at V_{afc} in after limiting.
16. With RE = 10 k Ω ; RA1 = 12 k Ω .

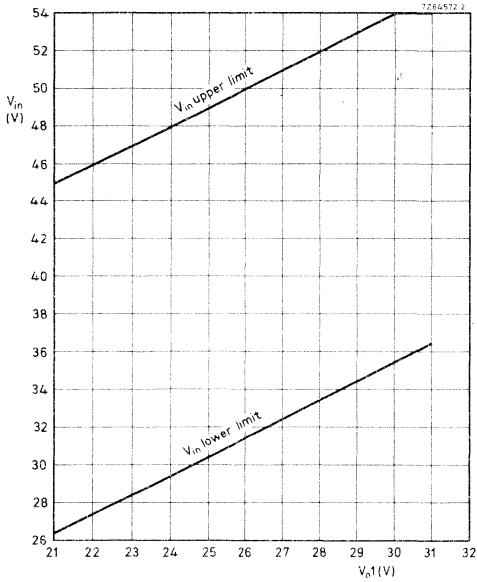


Fig. 1. Range of values for V_{01}

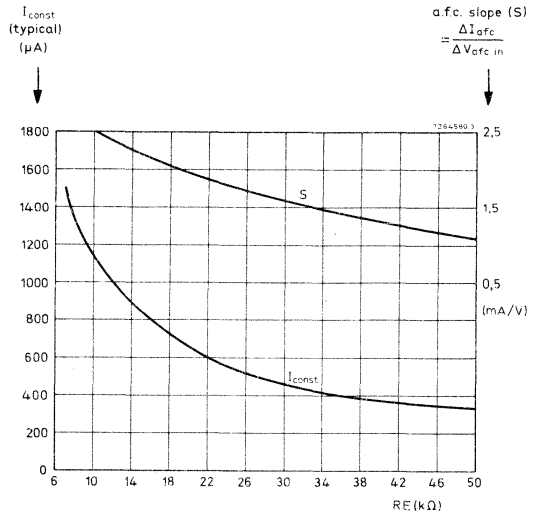


Fig. 2. Determination of I_{10} and S-factor from RE

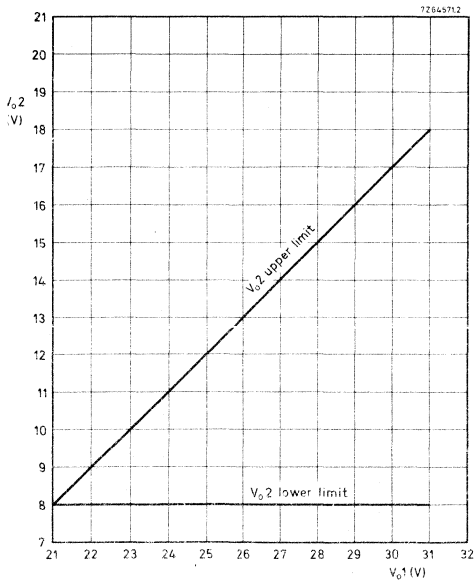


Fig. 3. Range of values for V_{02}

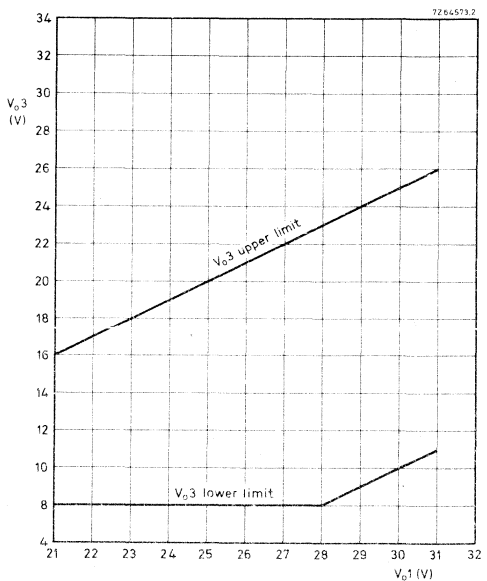


Fig. 4. Range of values for V_{03}

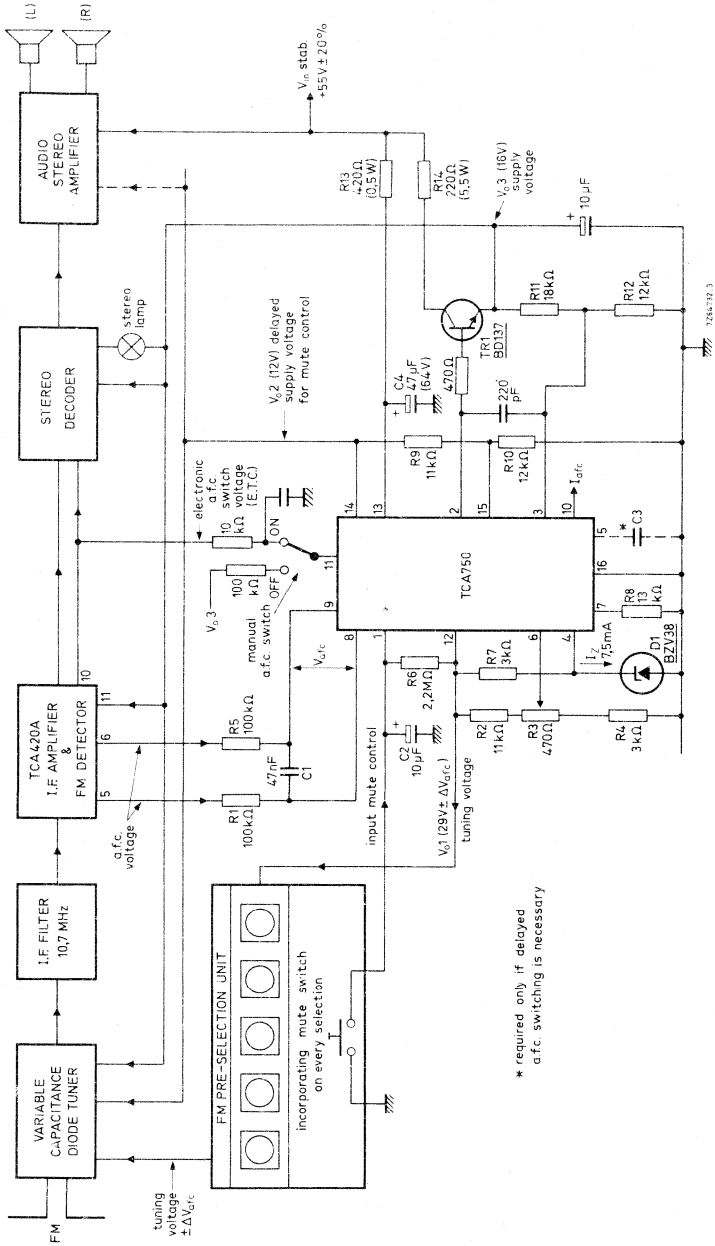


Fig. 5. Hi-fi radio receiver with electronic tuning using TCA750.

INTEGRATED AUDIO AMPLIFIER

The TCA760B is a monolithic integrated audio amplifier incorporating high flexibility for applications in battery and mains-fed equipment.

Due to special internal circuitry (stabilization, temperature correction, high a. c. feedback of 20 dB) the cross-over distortion is negligible over the entire supply voltage range (5 to 14 V). Presetting is not required for the quiescent current (5 to 15,7 mA), it is internally adjusted.

Additional features are :

- low noise output voltage;
- high peak current (1 A);
- high unloaded supply voltage (15 V);
- high gain (closed loop 15 dB at a feedback of 20 dB);
- safe operation regarding second breakdown;
- high ripple rejection.

The device will withstand repetitive short circuits across the speaker load if the absolute maximum junction temperature is not exceeded.

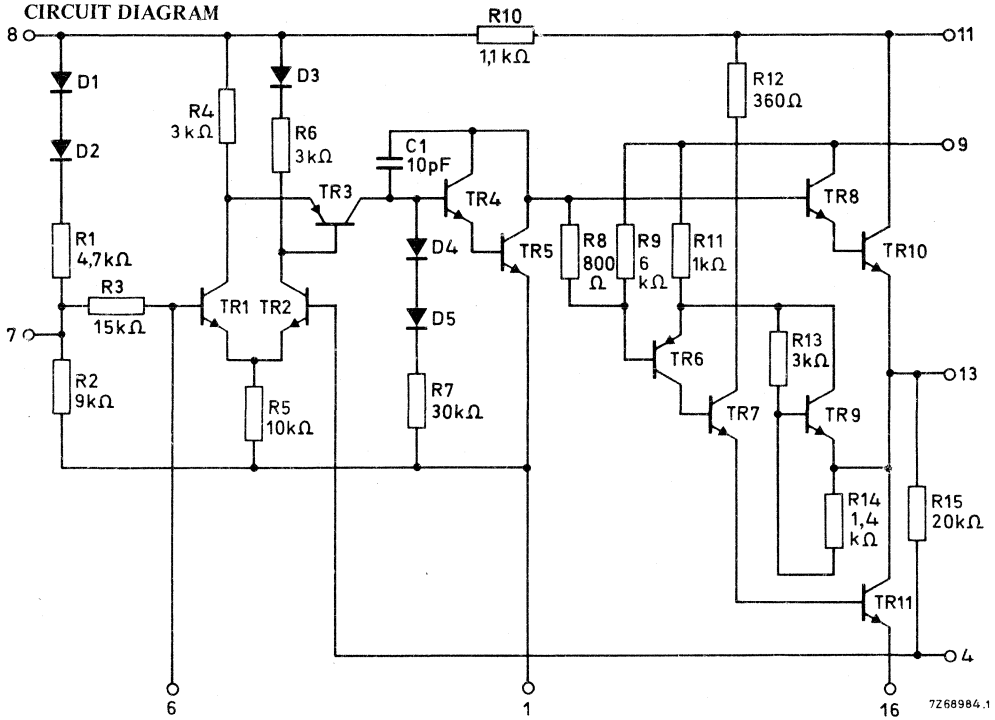
QUICK REFERENCE DATA

Supply voltage range	V_P	5 to 14	V
Total quiescent current	I_{tot}	5 to 15,7	mA
Supply voltage (peak value)	V_{PM}	max. 15	V
Output power at $d_{tot} = 10\%$			
at $V_P = 9\text{ V}; R_L = 8\ \Omega$	P_o	typ. 1,1	W
at $V_P = 12\text{ V}; R_L = 8\ \Omega$	P_o	typ. 2,1	W
Total distortion before clipping	d_{tot}	typ. 0,7	%
Input impedance	$ Z_i $	typ. 15	k Ω
Sensitivity for P_o at $d_{tot} = 10\%$	V_i	typ. 10	mV

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

TCA760B



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (pin 11)	V_{11-16}	max.	14	V
Unloaded supply voltage (pin 11; peak value) (no-signal condition)	V_{11-16M}	max.	15	V

Currents

Output current (pin 13, 11, 4)	I_O	max.	1	A
Non-repetitive peak output current (pin 13, 11, 4)	I_{OSM}	max.	2	A

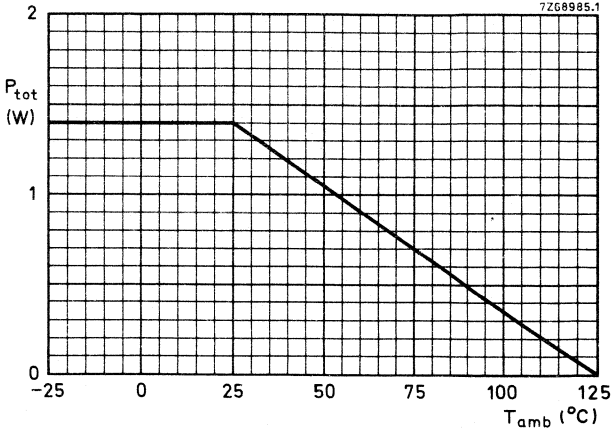
Power dissipation ¹⁾

Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	P_{tot}	max.	1,4	W
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Temperatures

Storage temperature	T_{stg}	-55 to +125	$^\circ\text{C}$
Operating ambient temperature	T_{amb}	-25 to +125	$^\circ\text{C}$

¹⁾ See derating curve on page 3.



Design data

Pin 6 to 4 voltage	$\pm V_{6-4}$	max.	6	V
Pin 13 to 16 voltage	V_{13-16}	max.	14	V
Pin 11 to 13 voltage	V_{11-13}	max.	14	V

CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_P = 9\text{ V}$; $R_L = 8\text{ }\Omega$ unless otherwise specified

D.C. characteristics

Supply voltage range	V_{11-16}	5 to 14 V
Total quiescent current	$I_{11\text{ tot}}$	{ typ. 10 mA 5 to 15,7 mA } ¹⁾
Saturation voltages of output stages at $I_O = 0,5\text{ A}$	V_{CEsat}	< 0,9 V

A.C. characteristics

A.F. output power at onset of clipping at $d_{tot} = 10\%$	P_O	typ.	0,8 W	3)
	P_O	typ.	1,1 W	
Open loop voltage gain	G_V	typ.	70 dB	
Total harmonic distortion at $P_O = 0,7\text{ W}$	d_{tot}	{ typ.	0,7 %	
		<	3 %	
Noise output power at $R_S = 0$	P_n	typ.	2 nW	¹⁾²⁾
Input sensitivity at $P_O = 0,7\text{ W}$	V_i		4 to 8,5 mV	
Input impedance	$ Z_i $	typ.	15 k Ω	
Equivalent input noise voltage at $R_S = 7\text{ k}\Omega$	V_n	{ typ.	1,5 μV	¹⁾²⁾
		<	3,0 μV	

1) Measured without signal.

2) Measured at a frequency ranging from 30 Hz to 15 kHz.

3) Measured across R_L .

APPLICATION INFORMATION

Supply voltage V_{11-16}	6	6	7,5	7,5	9	9	10	12	V
Load resistance R_L	4	8	4	8	4	8	8	8	Ω
A. F. output power at onset of clipping	0,45 0,42	0,35 0,33	0,8 0,7	0,6 0,57	1,1 1,0	0,9 0,8	1,2 1,1	1,4 1,3	W 1) W 2)
A. F. output power at $d_{tot} = 10\%$	0,66 0,62	0,48 0,46	1,1 1,0	0,8 0,78	1,5 1,4	1,2 1,1	1,5 1,45	2,1 2,0	W 1) W 2)
Sensitivity for $P_0 = 50$ mW V_i	1,4	2,0	1,4	2,0	1,4	2,0	2,0	2,0	mV
for $d_{tot} = 10\%$ V_i	4,8	7,0	8,0	9,0	10	10	11,0	12,0	mV
T_{amb} (maximum)	93	107	78	99	45	87	81	45	$^{\circ}C$
Supply current for full output power	185	125	225	165	300	190	215	250	mA
Quiescent current I_{tot}	10,0	10,0	10,0	10,0	10,0	10,0	10,0	10,0	mA
Value of R1	47	47	47	47	47	47	47	47	Ω
R2	100	100	100	100	100	100	100	100	Ω
R3	1	1	1	1	1	1	1	1	Ω
C1	1,6	1,6	1,6	1,6	1,6	1,6	1,6	1,6	μF
C2	47	47	47	47	47	47	47	47	μF
C3	125	125	125	125	125	125	125	125	μF
C4	470	220	470	220	470	220	220	220	μF
C5	1000	470	1000	470	1000	470	470	470	μF
C6	150	150	150	150	150	150	150	150	nF
C7	47	47	47	47	47	47	47	47	μF
Input impedance $ Z_i $	15	15	15	15	15	15	15	15	k Ω
Closed loop voltage gain G_V	50	50	50	50	50	50	50	50	dB 3)
Open loop voltage gain G_V	66	68	70	71	70	74	76	78	dB
Frequency response	← see pages 9 and 10 →								
Noise output power P_n			4			2			nW 4)
Noise output power P_n			50			25			nW 5)

1) Measured before output capacitor (C5).

2) Measured across R_L .

3) At $R_1 = 47 \Omega$. The gain can be increased by decreasing the value of R_1 ; at decreasing the gain level however the maximum tolerated value of R_1 amounts to 100Ω ; at further decrease of the gain an attenuator at the input is preferred.

4) $R_S = 0 \Omega$; frequency range 30 Hz to 15 kHz.

5) $R_S = 7 k\Omega$; frequency range 30 Hz to 15 kHz.

APPLICATION INFORMATION (continued)

General notes

1. Prescription for print lay-out:

Pin 1 must be used as a ground connection for the input circuit.

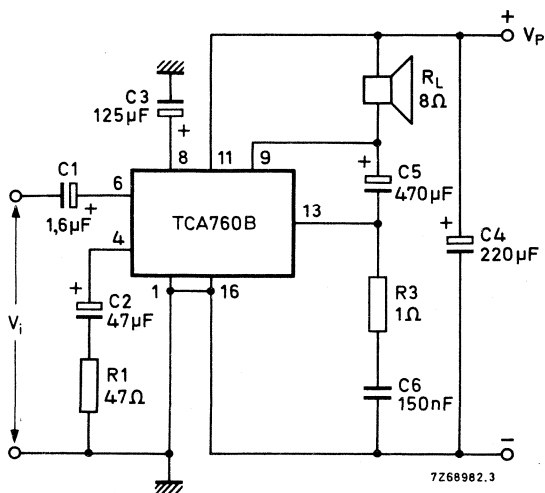
Pin 16 must be used for the output circuit and for connection of the negative supply voltage.

The pins 16 and 1 have to be interconnected as close to the package as possible to prevent a common impedance in the ground line.

2. The smoothing capacitor across the supply must be connected close to the pins.

3. To prevent radio signals in the low frequency amplifier a small capacitor of about 560 pF between pins 6 and 1 is preferred.

Basic power amplifier

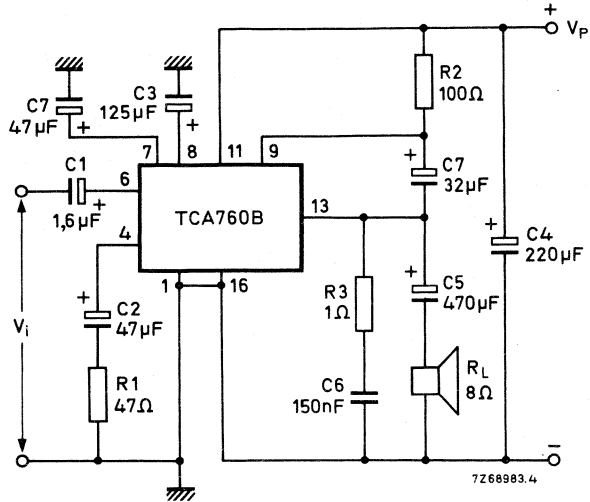


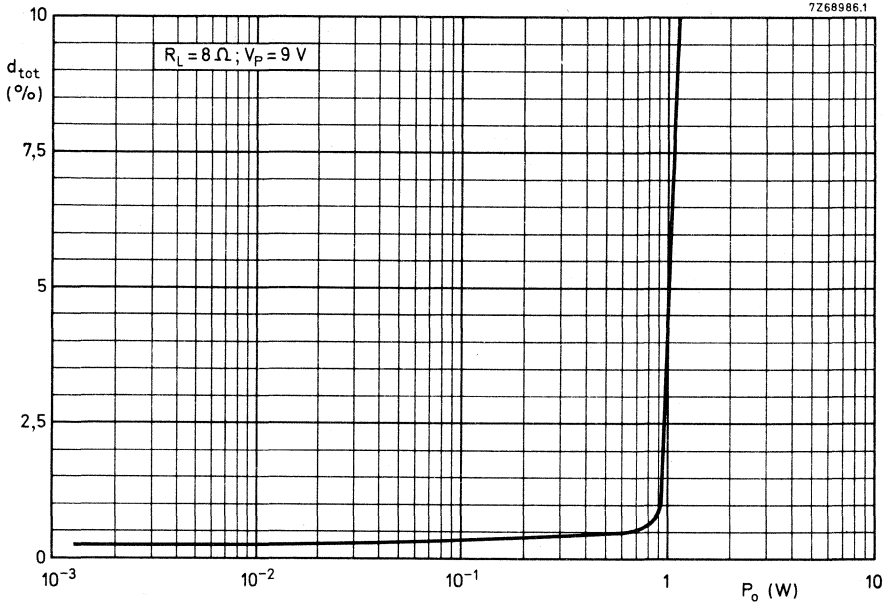
APPLICATION INFORMATION (continued)

Power amplifier for mains-fed supply

When using a mains-fed power supply with high ripple it is advantageous to connect the speaker to ground by bootstrapping pin 9.

Pin 7 is available for extra hum suppression (see graphs on page 9).

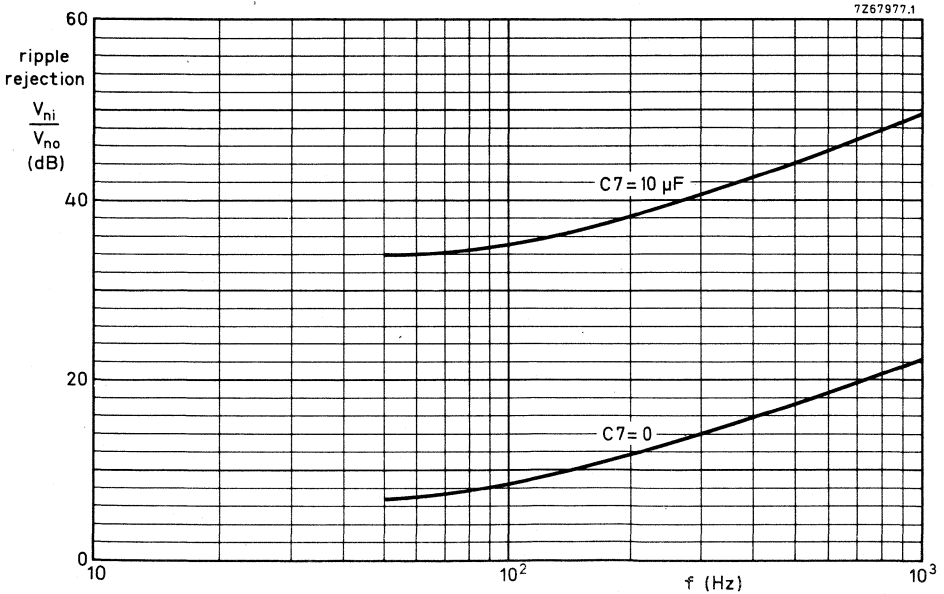
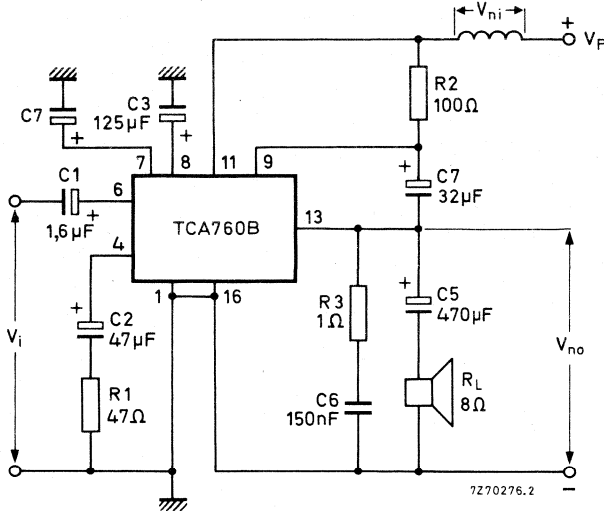




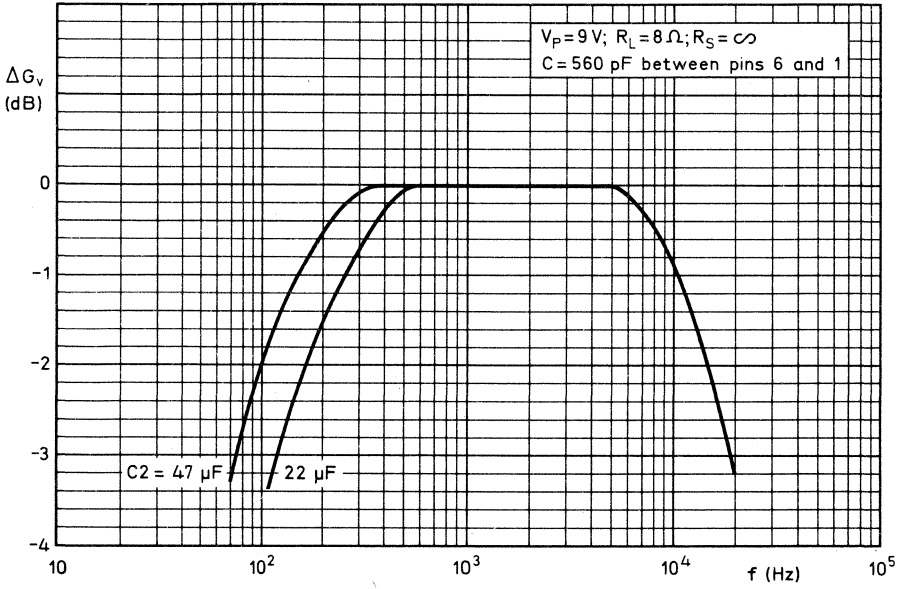
APPLICATION INFORMATION (continued)

The influence on the hum suppression when a capacitor of $10\ \mu\text{F}$ is connected between pins 7 and 1 is shown in the graph below.

An increase of the capacitor value gives no further improvement in hum suppression.



7267976



RECORDING PREAMPLIFIER CIRCUIT

The TDA1002 incorporates all amplifier circuits necessary for the record/playback functions, with the exception of the audio power output amplifier.

It comprises:

- a preamplifier for microphone or playback
- a recording amplifier with automatic level control and a dynamic limiter with a short limiting time.

For radio recorders, the TDA1002 is adapted to existing radio ICs (TBA570A, TBA700), in which the detector output is accessible for recording and the audio input for playback.

For cassette recorders, it is adapted to the existing audio power ICs such as TCA760B.

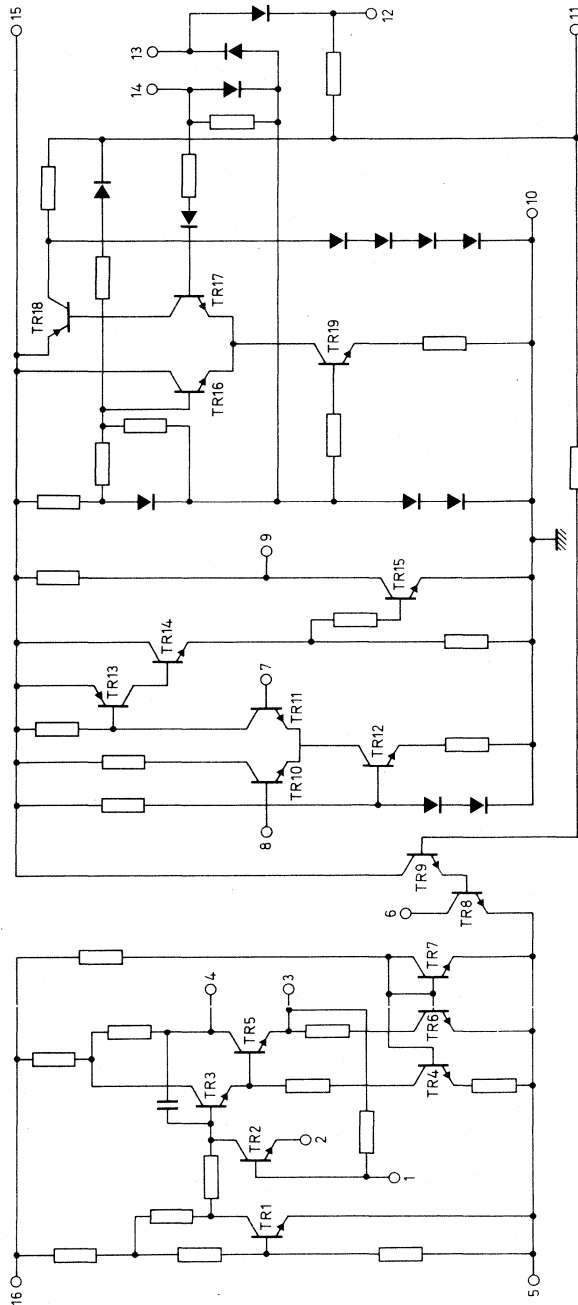
QUICK REFERENCE DATA

Supply voltage range	V_P	nom.	9 V 4 to 12 V
Ambient temperature	T_{amb}	typ.	25 °C

Total quiescent current	I_{tot}	typ.	14 mA
<u>Preamplifier</u>			
		Record (mic.)	Playback
Voltage gain	G_V	typ.	28 50 dB
Distortion before clipping	d_{tot}	typ.	0, 1 0, 3 %
Input impedance	$ Z_i $	typ.	17 17 kΩ
<u>Recording amplifier</u>			
Voltage gain (at f = 1 kHz)	G_V	typ.	54 dB
Distortion at $V_o = 1 V$	d_{tot}	typ.	0, 4 %
Impedance level at P (see page 9)	$ Z_i $	typ.	40 kΩ
<u>Automatic level control</u>			
		input	output
		10	400 mV
		1000	900 mV
Limiting time ($\Delta V_i = 20$ dB)		typ.	4 ms
Recovery time ($\Delta V_i = -20$ dB)		typ.	20 s

PACKAGE OUTLINE 16-lead DIL; plastic (see general section).

CIRCUIT DIAGRAM



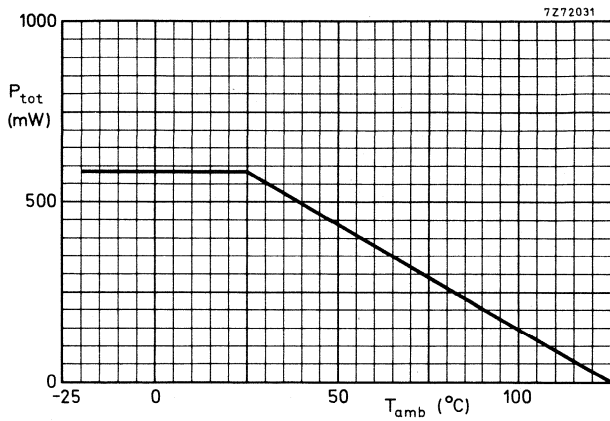
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage : pin 15	V_{15-10}	max.	12 V
pin 16	V_{16-5}	max.	12 V

Dissipation

Total power dissipation see derating curve below



Temperatures

Storage temperature	T_{stg}	-65 to +125 °C
Operating ambient temperature (see also derating curve above)	T_{amb}	-20 to +125 °C

D.C. CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$

<u>Supply voltages</u>	V_{15-10}		4 to 12	V
	V_{16-5}		4 to 13	V
<u>Quiescent currents</u>	I_{15}	typ.	9	mA
	I_{16}	typ.	4,5	mA
<u>Output voltages</u>				
Preamplifier	V_{4-5}	typ.	3,3	V
Recording amplifier	V_{9-10}	typ.	4	V

A.C. CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_p = 9\text{ V}$

<u>Preamplifier</u>			Record 1) (mic.)	Playback 2)
Open loop voltage gain	G_V	typ.	80	80 dB
Voltage gain at $f = 1\text{ kHz}$	G_V	typ.	28	50 dB
Output voltage before clipping	V_O	>	2,2	- V
Equivalent noise input voltage	V_n	typ.	0,5	0,5 μV 3)
Input impedance	$ Z_i $	typ.	17	17 $\text{k}\Omega$
Distortion at $V_O = 500\text{ mV}$	d_{tot}	typ.	0,1 4)	0,3 5) %
Amplitude response				see note 6
<u>Recording amplifier (with automatic level control) 7)</u>				
Open loop voltage gain	G_V	typ.	80	dB 8)9)
Voltage gain at $f = 1\text{ kHz}$	G_V	typ.	54	dB 8)9)
Amplitude response				see Fig. 8 on page 10
Impedance level at P (see page 9)	$ Z_i $	typ.	40	$\text{k}\Omega$ 10)
Distortion at $V_O = 1\text{ V}$ (see Fig. 9 on page 10) without automatic level control)	d_{tot}	<	0,4	%

1) Measured in Fig. 1 on page 6.

2) Measured in Fig. 3 on page 7.

3) $R_S = 0,5\text{ k}\Omega$; $B = 300\text{ Hz}$ to 15 kHz .

4) See Fig. 2 on page 6.

5) See Fig. 4 on page 7.

6) See Fig. 5 on page 8.

7) Measured in Fig. 7 on page 9.

8) Referring to V_O and V_i .

9) The automatic level control being disconnected.

10) Depends on impedance level at pin 6.

A.C. CHARACTERISTICS (continued)Automatic level control¹⁾

Output voltage at $V_S = 1$ mV	V_{9-10}	typ.	70	mV
at $V_S = 10$ mV	V_{9-10}	typ.	400	mV
at $V_S = 100$ mV	V_{9-10}	typ.	600	mV
at $V_S = 1000$ mV	V_{9-10}	typ.	900	mV
			700 to 1200	mV
Limiting time (clipping at $\Delta V_i = +20$ dB)	t_l	<	6	ms ²⁾
Level setting time to reach final level within ± 1 dB after $\Delta V_i = +20$ dB	t_s	<	4	s ²⁾
Recovery time after $\Delta V_i = -20$ dB	t_r	typ.	20	s ³⁾

¹⁾ The input signal V_S of 1 kHz is applied via 33 k Ω to pins 6 and 8 (see Fig. 6 on page 8).

²⁾ See Fig. 10 on page 11.

³⁾ See Fig. 11 on page 11; 2 dB value depends on R_R/C_R (see page 9).

Preamplifier used as microphone amplifier

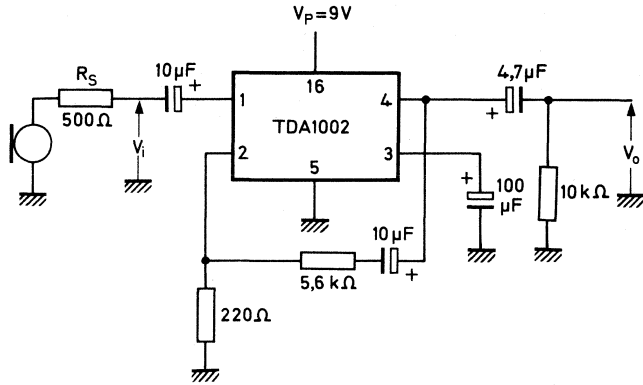


Fig. 1

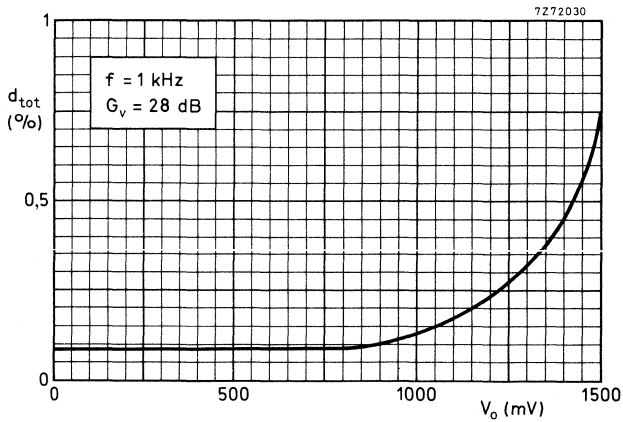


Fig. 2. (typical values)

Preamplifier used for playback

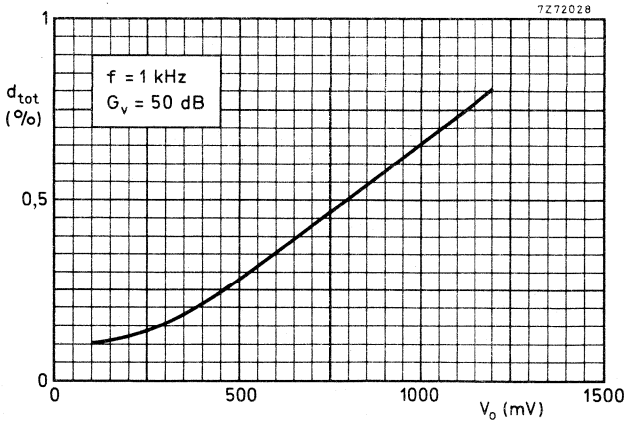
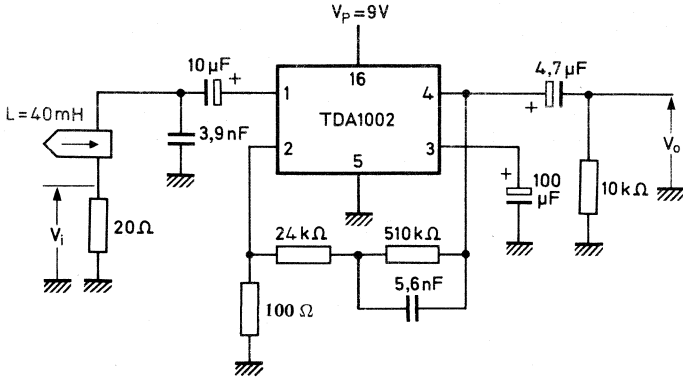


Fig. 4. (typical values)

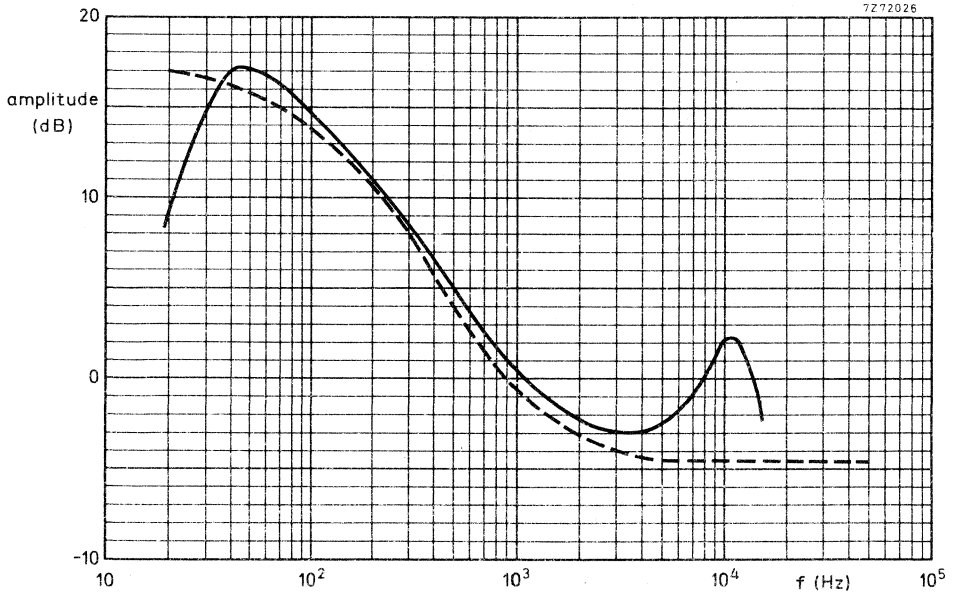


Fig. 5. (typical values)

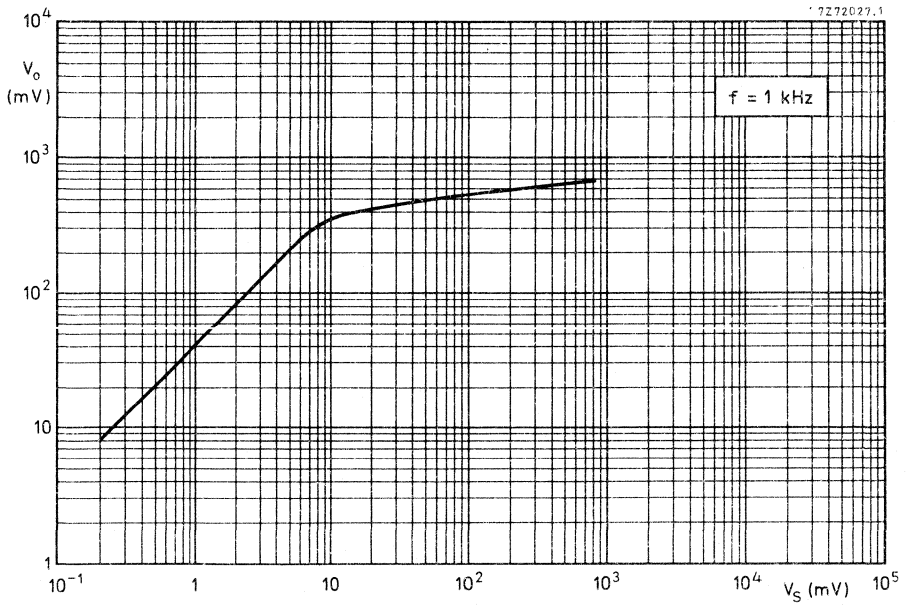
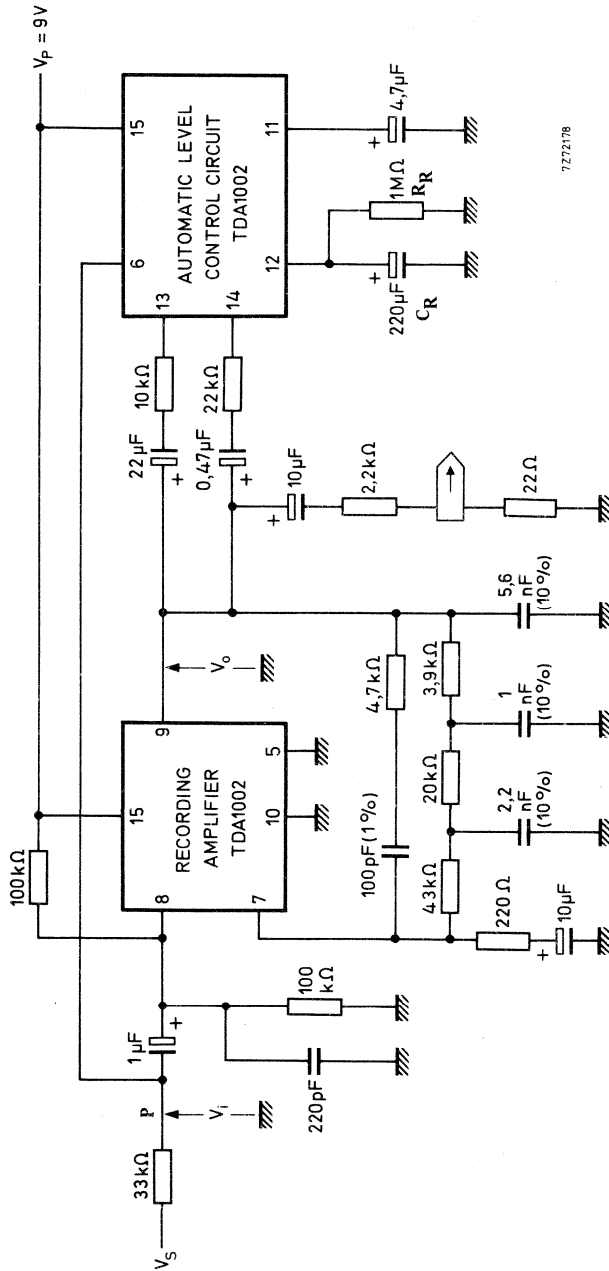


Fig. 6. (typical values)

Recording amplifier with automatic level control



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Fig. 7.



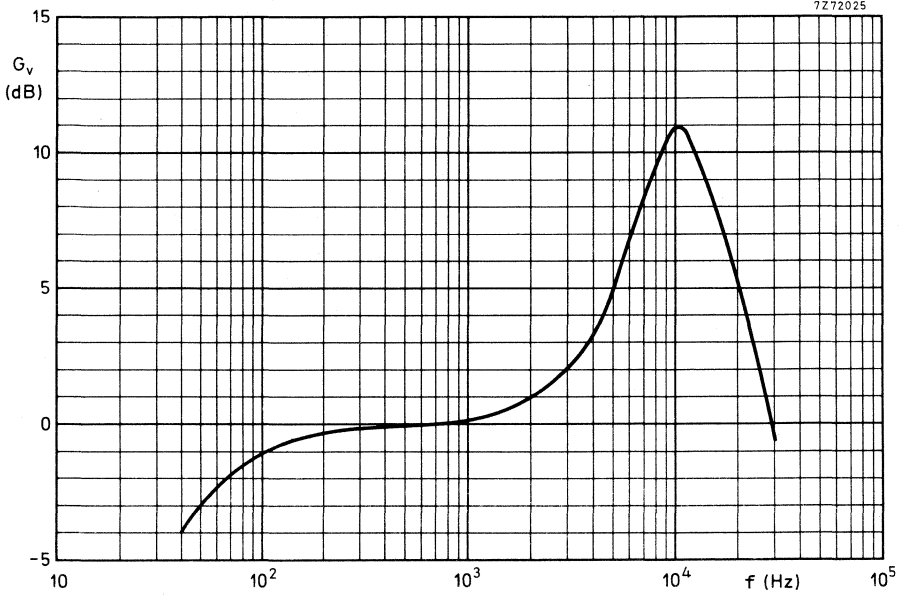


Fig. 8. Amplitude response of recording amplifier (level control not connected) (typical values)

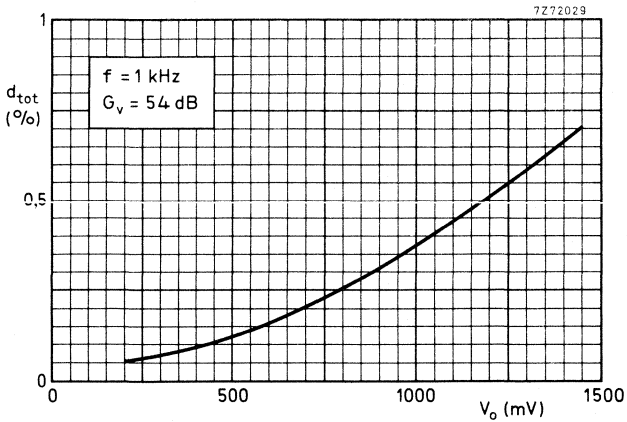
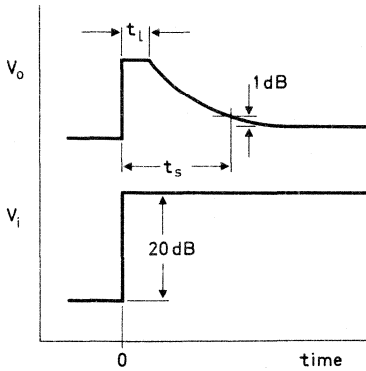


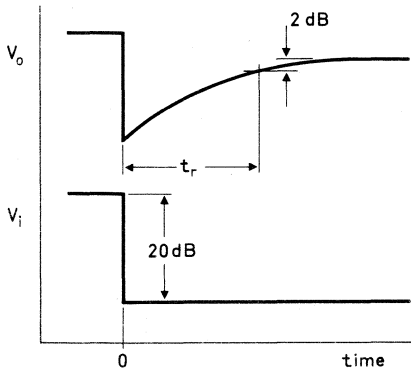
Fig. 9. (typical values)

TIMING DIAGRAMS



t_l = limiting time
 t_s = level setting time

Fig. 10



t_r = recovery time

Fig. 11



MOTOR REGULATOR AND BIAS/ERASE OSCILLATOR CIRCUIT

The TDA1003A is pin for pin compatible with the TDA1003 with an extension of features. The TDA1003A is for use in recording/playback systems. It incorporates capstan motor speed control, an automatic stop circuit, and a bias/erase oscillator.

The motor circuit controls the back e. m. f. and delivers a stabilized voltage to the capstan motor. The motor voltage is corrected for line voltage and torque variations, and temperature variations of the magnetic material and windings. The motor speed control is operative as long as a pulse train, derived from the tape wind spool mechanism via an interrupter, is applied to the automatic stop circuit. The TDA1003A can also be used without stop circuit by connecting pin 16 to ground. An output is available for a "stop" indicator lamp.

The oscillator section contains a temperature-independent voltage reference source and an a. g. c. circuit controlling the transconductance of a balanced oscillator circuit incorporating the erase head. Any Q variations of the erase head winding are fed back to maintain the oscillator output as a constant undistorted sine-wave so that harmonic products do not cause interference during radio recording.

QUICK REFERENCE DATA

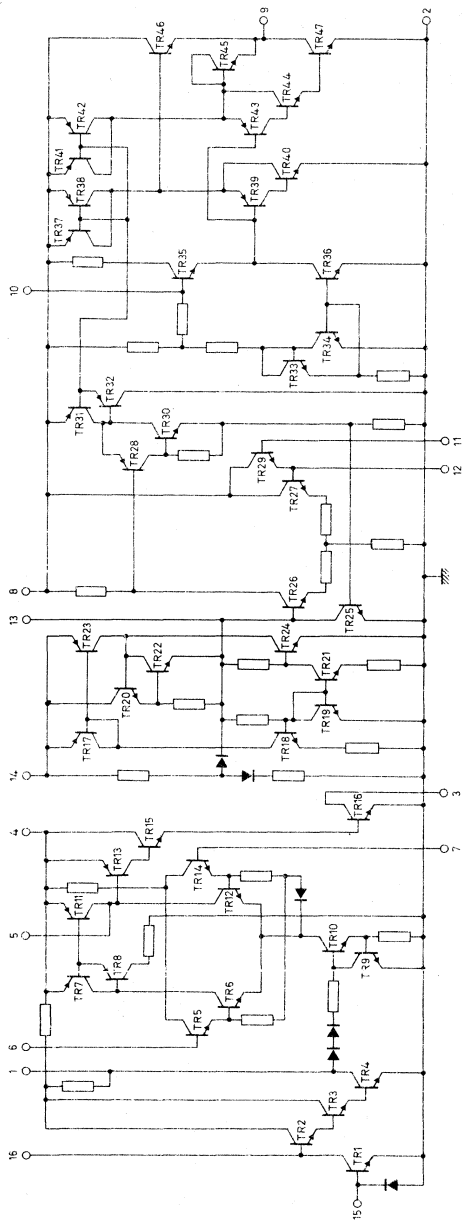
Supply voltage range	V_p		3, 5 to 18	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage	V_p	typ.	9	V

Motor regulator				
Current consumption	I_4	typ.	1, 8	mA
Motor starting current	I_3	<	1000	mA
Operating motor current	I_3	<	250	mA
Minimum operating voltage at $I_3 = 600$ mA	V_{3-2min}	typ.	0, 9	V
Supply voltage rejection	$\Delta V_{3-2}/\Delta V_{4-2}$	typ.	1	mV/V
Stop circuit				
Output current for "stop" indicator lamp	I_1	<	100	mA
Knee voltage at $I_1 = 100$ mA	V_{1-2}	typ.	0, 6	V
Input current for $I_1 = 100$ mA	I_{16}	>	4	μ A
Bias and erase oscillator				
Current consumption at Q = 40	I_8	typ.	25	mA
Erase head voltage at Q = 40 (r. m. s. value)	$V_{erase(rms)}$	typ.	16	V

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic power.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage on : pin 4	V_{4-2}	max.	18	V
pin 8	V_{8-2}	max.	18	V
pin 14	V_{14-2}	max.	18	V

Currents

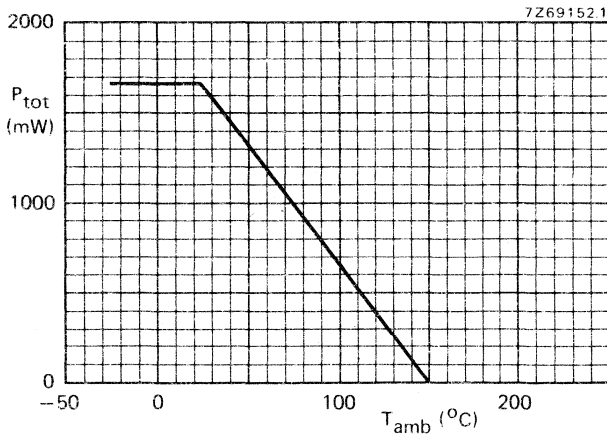
Motor current (pin 3; peak-value)	I_{3M}	max.	1000	mA
"Stop" indicator lamp current (d. c. : pin 1)	I_1	max.	100	mA
Maximum input current (pin 15)	$\pm I_{15 \max}$	max.	20	mA

Temperatures

Storage temperature	T_{stg}	-65 to +150	°C
Operating ambient temperature see also power derating curve below	T_{amb}	-20 to +150	°C

Power dissipation

Total power dissipation see derating curve below



CHARACTERISTICS at $V_p = 9\text{ V}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ unless otherwise specified; see test circuit on page 6

Supply voltage range (pins 4, 8 and 14)	V_p		3, 5 to 18	V ¹⁾	
Motor regulator					
Current consumption	I_4	typ.	1, 8	mA	
			1 to 3	mA	
Operating motor current	I_3	<	250	mA	
Motor starting current (peak-value)	I_{3M}	<	1000	mA	
Input offset voltage at $I_3 = 3\text{ mA}$	$ V_{7-6} $	typ.	2	mV	
		<	8	mV	
Input offset current at $I_3 = 3\text{ mA}$	$ I_{7-6} $	typ.	0, 2	μA	
Input voltage range (common mode)	V_{6-2}		2, 4 to ($V_p - 0, 25$)	V	
	V_{7-2}		2, 4 to ($V_p - 0, 25$)	V	
Input bias current	$I_{6; 17}$	typ.	0, 1	μA	
		<	1, 0	μA	
Input sensitivity (for $\Delta I_3 = 100\text{ mA}$)	ΔV_{7-6}	typ.	1	mV	
		<	10	mV	
Minimum operating voltage at $I_3 = 600\text{ mA}$	$V_{3-2\text{ min}}$	typ.	0, 9	V ²⁾	
		<	1, 8	V	
Automatic motor "stop" circuit					
"Stop" indicator lamp current	I_1	<	100	mA	
Knee voltage at $I_1 = 100\text{ mA}$	$V_{15-2} = \text{low}$ ("stop" condition)	V_{1-2}	typ.	0, 6	V
			<	1, 0	V
Input current for $I_1 = 100\text{ mA}$	I_{16}	>	4	μA	
Voltage at pin 1 without external load ($V_{16} = \text{low}$)	V_{1-2}	typ.	4, 1	V	
			3 to 5, 0	V	
Maximum input current (pin 15)	$\pm I_{15\text{ max}}$	<	20	mA	

¹⁾ To guarantee proper functioning with $V_p = 3, 5\text{ V}$ to 18 V , the external component values as shown in test circuit on page 6 should be modified.

²⁾ The minimum operating voltage is defined as the voltage (V_{3-2}) at which the motor still operates at correct speed.

CHARACTERISTICS (continued)**Bias and erase oscillator**

Current consumption at $Q = 40$	I_8	typ.	25	mA
at $Q = 20$	I_8	{ typ. <	38 46	mA
Internal current limiting	I_8	<	95	mA ¹⁾
Peak output current	$\pm I_9$	>	100	mA
Output voltage swing (peak-to-peak value)	$V_{9-2(p-p)}$	typ.	V_{P-2}	V
Current consumption of reference source	I_{14}	typ. <	1,8 2,4	mA
Reference voltage (temperature compensated) ²⁾	V_{13-2}	typ.	1,7	V
Erase head voltage; $Q = 40$; $L = 620 \mu\text{H}$ (r. m. s. value)	$V_{\text{erase}(rms)}$	typ.	1,55 to 1,9	V
Change of V_{erase} when Q changes from 20 to 60	ΔV_{erase}	typ. <	1 1,8	V

APPLICATION INFORMATION measured in circuit on page 7**Motor regulator**

Supply voltage rejection	$\frac{\Delta V_{3-2}}{\Delta V_{4-2}}$	typ.	1	mV/V
Motor speed variation over $T_{\text{amb}} = -5$ to $+55$ °C	$\pm \Delta n$	typ.	2	%

Automatic motor "stop" circuit

Input voltage from wind spool supplied via 10 k Ω to pin 15 (peak-to-peak value)	$V_{W(p-p)}$	typ.	1,2	V
Input current (pin 15)	$\pm I_{15}$	<	20	mA

Bias and erase oscillator

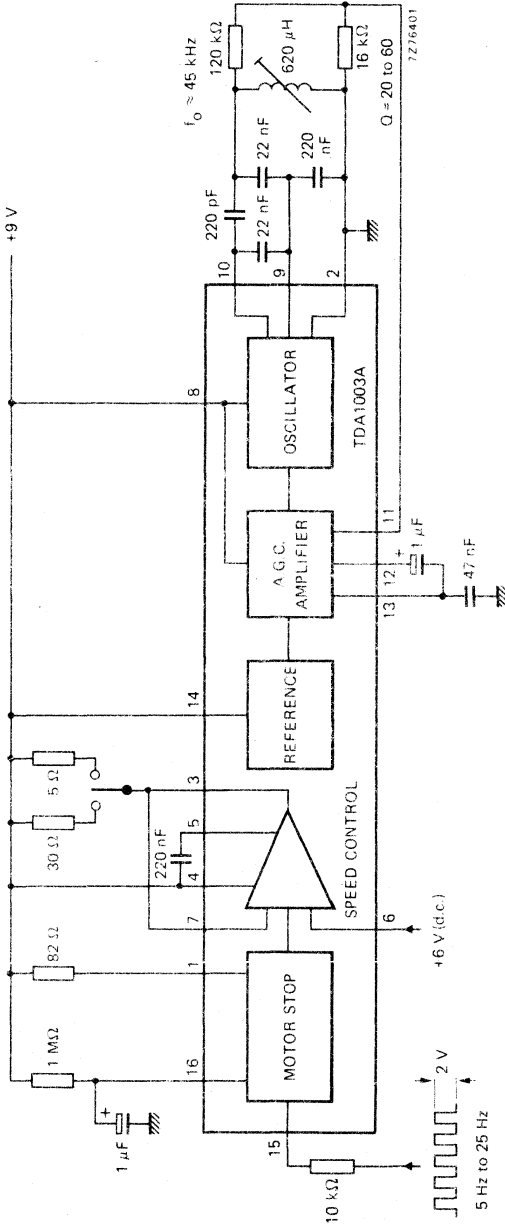
Erase head voltage for $Q = 40$; $L = 620 \mu\text{H}$ (r. m. s. value)	$V_{\text{erase}(rms)}$	typ.	16	V
Change of V_{erase} when Q changes from 20 to 60	ΔV_{erase}	typ.	1	V
Harmonic distortion (unsaturated erase head)	$-\alpha_{2\text{ndharm}}$	typ.	55	dB ³⁾
	$-\alpha_{3\text{rdharm}}$	typ.	40	dB
	$-\alpha_{>6\text{thharm}}$	>	80	dB

¹⁾ If erase head is defective.

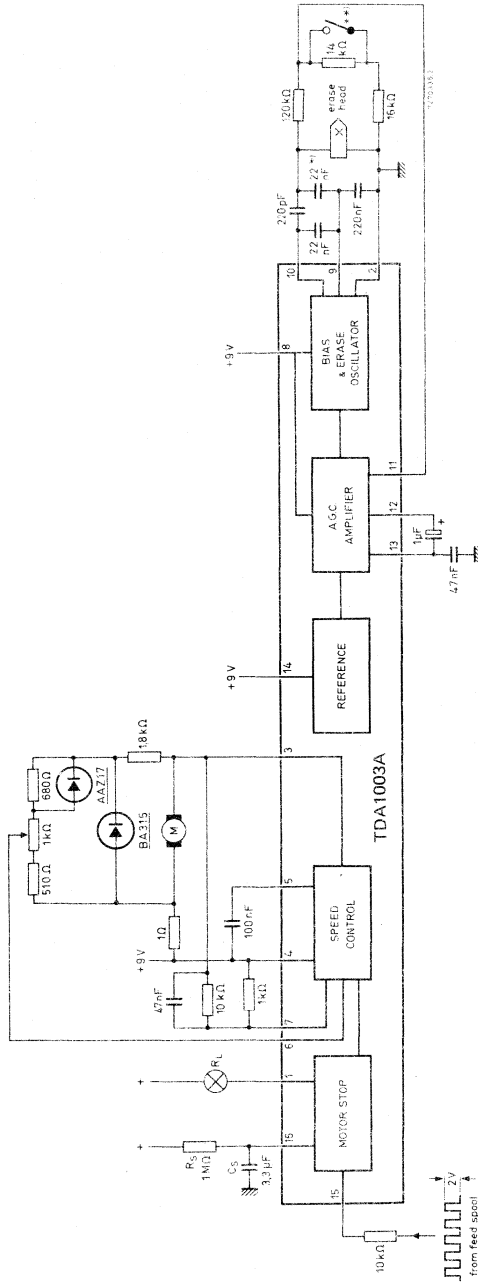
²⁾ Typical value of temperature coefficient 0 mV/°C.

³⁾ At unsaturated erase head, with respect to 45 kHz.

TEST CIRCUIT



APPLICATION INFORMATION (continued)



Motor (M): $R_M = 14 \Omega$
 $E_H = 2.3 \text{ V}$ at 1500 r. p. m.
 Erase head: $L = 620 \mu\text{H}$
 $Q = 40$
 $f_0 = 45 \text{ kHz}$

Indicator lamp: 9 V; 40 mA

*) Capacitor with low losses required; especially for CrO₂ tape and low battery voltage.

***) Switch closed: suitable for CrO₂ tape
 open : suitable for Fe₂O₃ tape.



10 W AUDIO POWER AMPLIFIER

with thermal shut-down

The TDA1004A is a monolithic integrated circuit in a plastic 16-lead power dual in-line package, intended for use as a low-frequency class-B amplifier.

This circuit can also be used in car radios, even when $2\ \Omega$ load is required.

The device provides 10 W output power at $20\ \text{V}/4\ \Omega$; 6 W at $14\ \text{V}/4\ \Omega$ and 7,5 W at $14\ \text{V}/2\ \Omega$. The supply voltage ranges from 9 to 20 V.

The TDA1004A is pin for pin compatible with the TDA1004.

The d. c. and a. c. gain are equal, which means an external feedback network is not necessary.

The circuit comprises two separate amplifiers with the following features:

- low-cost and small number of external components;
- thermal limiting circuit, the gain of the circuit decreases when the crystal temperature exceeds $150\ ^\circ\text{C}$;
- continuous short-circuit protection of the load for supply voltages up to 16 V;
- very good ripple rejection;
- low input impedance;
- low thermal resistance of the package thus requiring relatively small heatsinks;
- filtered but not stabilized supply (pin 6) available for other electronic functions.

QUICK REFERENCE DATA

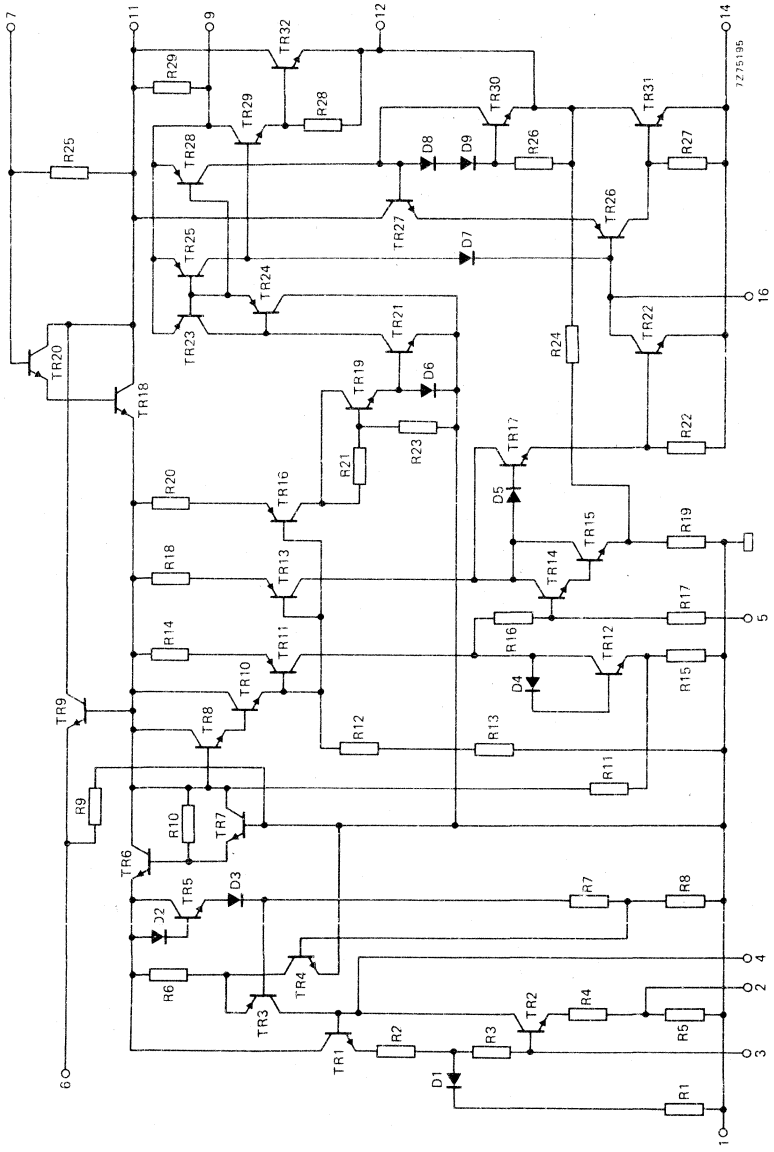
Supply voltage range	V_P	9 to 20	V
D. C. output current (peak value)	I_{OM}	< 2,5	A
Output power at $d_{tot} = 10\%$			
at $V_P = 14\ \text{V}; R_L = 4\ \Omega$	P_O	typ. 6,2	W
at $V_P = 14\ \text{V}; R_L = 2\ \Omega$	P_O	typ. 7,0	W
at $V_P = 20\ \text{V}; R_L = 8\ \Omega$	P_O	typ. 7,0	W
at $V_P = 20\ \text{V}; R_L = 4\ \Omega$	P_O	typ. 11,0	W
Total harmonic distortion at $P_O < 1\ \text{W}; R_L = 4\ \Omega$	d_{tot}	typ. 0,2	%
Input impedance	$ Z_i $	typ. 20	k Ω
Total quiescent current at $V_P = 14\ \text{V}$	I_{tot}	typ. 30	mA
Sensitivity at $P_O = 1\ \text{W}; R_L = 4\ \Omega$	V_i	typ. 6,6	mV
Operating ambient temperature	T_{amb}	-25 to +150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic power (SOT-69B).



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_p max. 24 V

Currents

Repetitive peak output current (pins 11, 12, 14) I_{ORM} max. 2.5 A

Non-repetitive peak output current (pins 11, 12, 14) I_{OSM} max. 5.0 A

Supply current from pin 6 I_6 max. 30 mA

Power dissipation

Total power dissipation see derating curve below

Temperatures

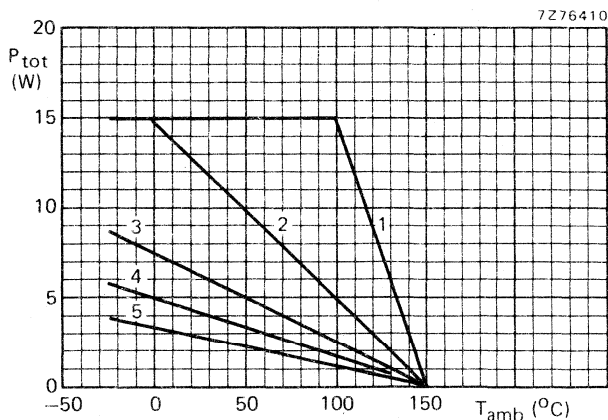
Storage temperature T_{stg} -55 to +150 °C

Operating ambient temperature T_{amb} -25 to +150 °C

Short-circuiting

A.C. short-circuit duration of load impedance during sine-wave signal drive:
without heatsink at $V_p = 14$ V

t_{sc} max. 100 hours



1. Infinite heatsink
2. External heatsink of 100 cm²
3. External heatsink of 30 cm²
4. External heatsink of 12 cm²
5. In free air: without external heatsink

Heatsink: blackened aluminium area.

THERMAL RESISTANCE (The power derating curve on page 3 is based on the following data)

From junction to case	$R_{th\ j-c}$	=	3,3	°C/W
From junction to ambient	$R_{th\ j-a}$	=	45	°C/W

CHARACTERISTICS**D.C. characteristics**

Supply voltage range (pin 11)	V_P		9 to 20	V
Supply voltage (pin 6) at $I_6 = 0$ mA at $I_6 = 20$ mA	V_{6-1}	>	11,0	V
	V_{6-1}	>	10,8	V
Output current (peak value)	I_{OM}	<	2,5	A
Output current at pin 6 (peak value)	I_{6M}	<	30	mA
Total quiescent current at $V_P = 14$ V	I_{tot}	typ.	30	mA
	I_{tot}	<	90	mA

A.C. characteristics at $T_{amb} = 25$ °C; $V_P = 14$ V; $R_L = 4$ Ω; $f = 1$ kHz unless otherwise specified; see also test circuit on page 5.

A. F. output power at $d_{tot} = 10\%$ ¹⁾ at $V_P = 14$ V; $R_L = 4$ Ω; without bootstrap ²⁾ at $V_P = 14$ V; $R_L = 4$ Ω at $V_P = 14$ V; $R_L = 2$ Ω at $V_P = 20$ V; $R_L = 8$ Ω at $V_P = 20$ V; $R_L = 4$ Ω	} with bootstrap ¹⁾	P_o	>	4,8	W
		P_o	>	5,5	W
		P_o	typ.	6,2	W
		P_o	typ.	7,0	W
		P_o	typ.	7,0	W
		P_o	typ.	11,0	W
Voltage gain preamplifier	G_{v1}	typ.	20	dB	
			17 to 23	dB	
power amplifier	G_{v2}	typ.	30	dB	
			27 to 33	dB	
total amplifier	$G_{v\ tot}$	typ.	50	dB	
			47 to 53	dB	
Total harmonic distortion at $P_o = 1$ W	d_{tot}	typ.	0,2	%	
		<	1,0	%	
Frequency response (-3 dB)	B		60 Hz to 17	kHz	
Input impedance: preamplifier	$ Z_i $	>	15	kΩ	
		typ.	20	kΩ	
		typ.	30	kΩ	
power amplifier	$ Z_i $	typ.	30	kΩ	
Output impedance of preamplifier (pin 4)	$ Z_o $	>	10	kΩ ³⁾	

¹⁾ Output power is always measured at the d.c. output of the amplifier, so losses in coupling capacitor are not taken into account.

²⁾ See circuit on page 7. With this circuit 4,8 W is guaranteed.

³⁾ At this impedance value from pin 4 to ground, the maximum output power can be delivered.

CHARACTERISTICS (continued)

Output voltage preamplifier
at $d_{tot} = 5\%$ (r. m. s. value)

$V_{4-1}(\text{rms})$	>	0,6 V	1)
	typ.	1,0 V	

Noise output voltage at $R_S = 0 \Omega$
at $R_S = 2 \text{ k}\Omega$

V_n	typ.	0,3 mV	2)
V_n	<	1,0 mV	

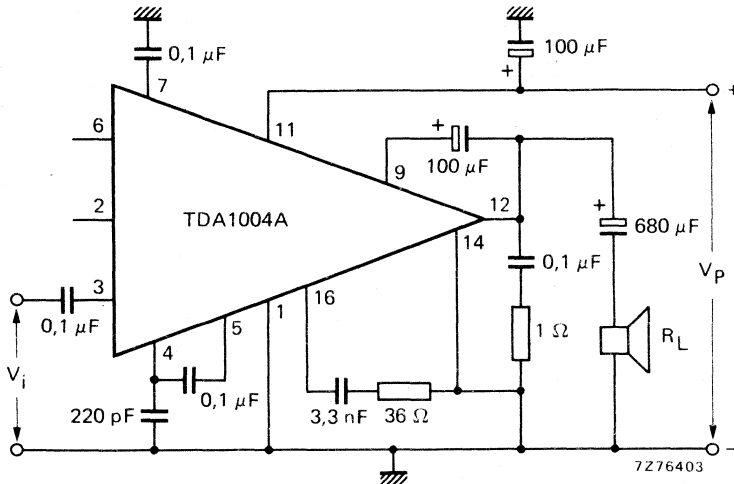
Sensitivity at $P_o = 1 \text{ W}$

V_i	typ.	6,6 mV
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Ripple rejection at $f = 100 \text{ Hz}$
at $f = 1 \text{ kHz}$

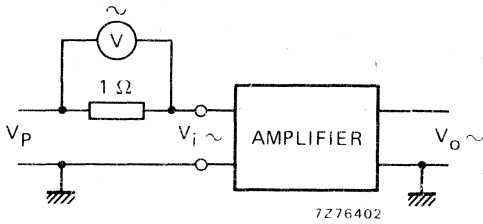
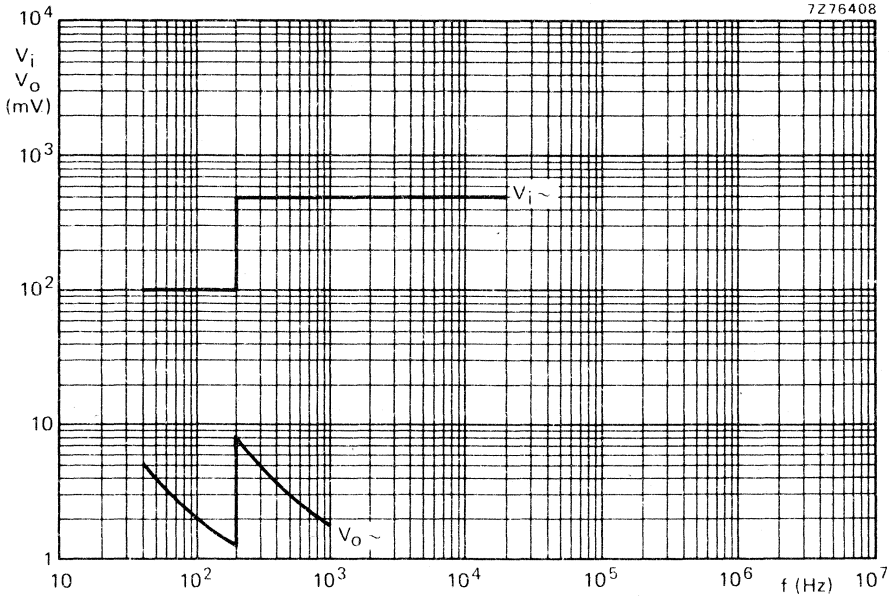
RR	typ.	32,5 dB	3)
RR	typ.	50,0 dB	

Test circuit



1) Measured with a 30 kΩ a.c. load impedance at pin 4 (disconnected from pin 5).
 2) Measured at a bandwidth of 60 Hz to 15 kHz.
 3) See ripple rejection on page 6.

RIPPLE REJECTION

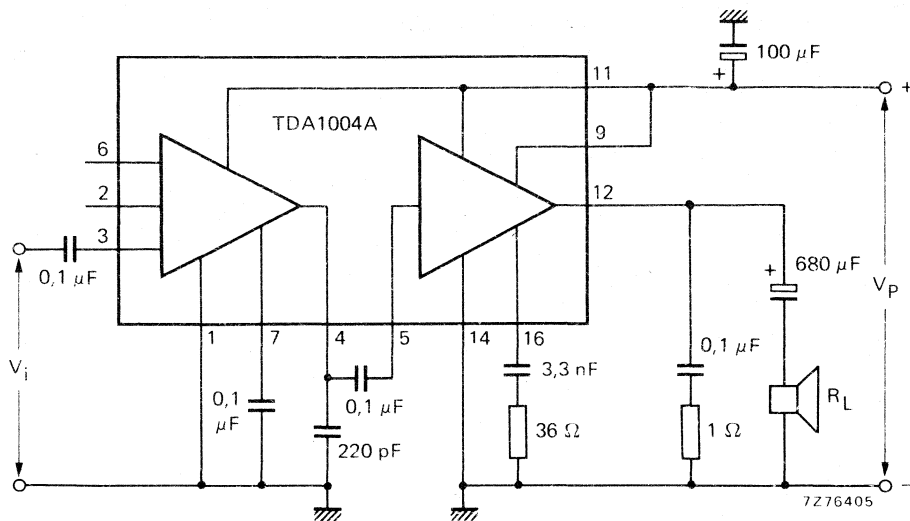


Typical ripple rejection measured with nominal load impedance ($R_L = 4 \Omega$) and input a.c. short-circuited.

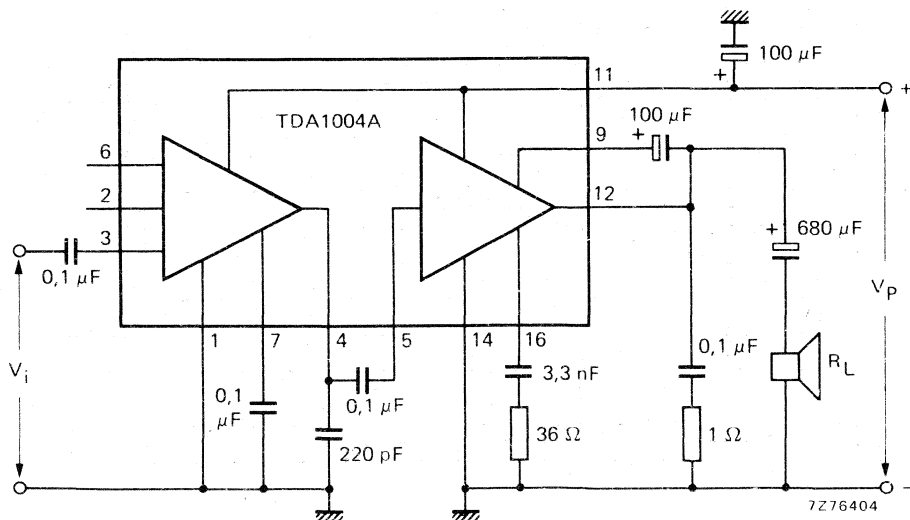
$V_o \text{ max} = 4 \text{ mV}$ at $f = 10^3 \text{ Hz}$.

APPLICATION INFORMATION

Without bootstrap

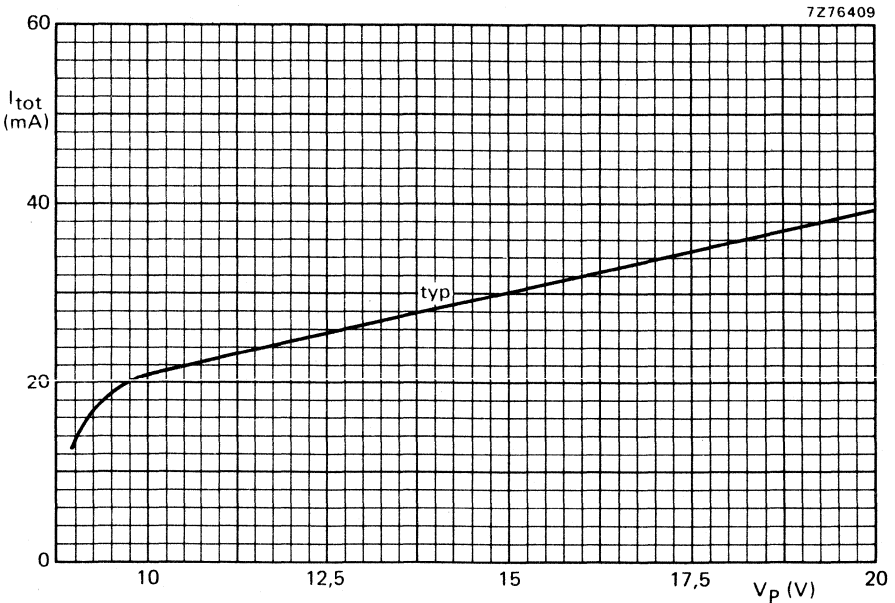


With bootstrap



APPLICATION INFORMATION (continued)

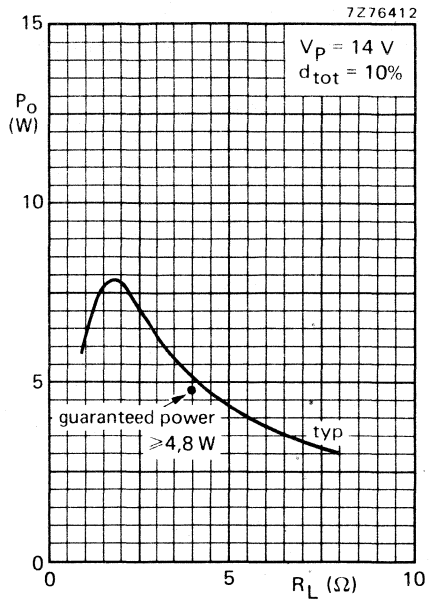
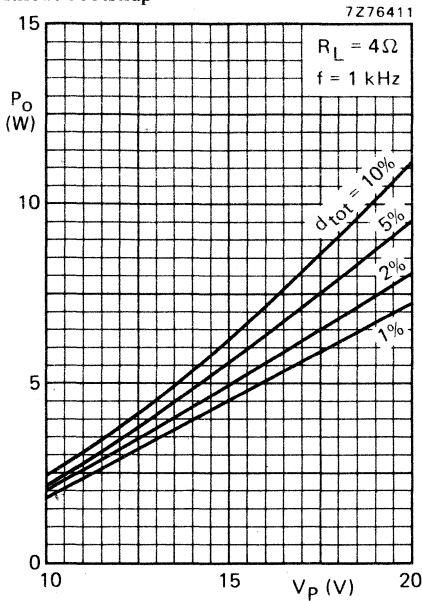
Supply voltage (V_{11-14})	V_P	14			20		V
Load resistance	R_L	2	4	8	4	8	Ω
Total quiescent current	I_{tot}	30	30	30	40	40	mA
Output power at $d_{tot} = 10\%$ with bootstrap	P_O	7,0 ¹⁾	6	3,5	12	7	W
	P_O	7,5	5	3,0	11	6	W
Distortion at $P_O = 2$ W	d_{tot}	1	0,2	0,2	0,2	0,2	%
Input sensitivity for $P_O = 1$ W	V_i	4,8	6,6	9,1	6,6	9,1	mV
Ripple rejection at $f = 100$ Hz at $f = 1$ kHz	RR	32,5	32,5	32,5	32,5	32,5	dB
	RR	50,0	50,0	50,0	50,0	50,0	dB
Noise output voltage at $B = 60$ Hz to 15 kHz $R_S = 0 \Omega$	V_n	0,30	0,30	0,30	0,30	0,30	mV
	V_n	0,45	0,45	0,45	0,45	0,45	mV
		$R_S = 2$ k Ω					
Input impedance	$ Z_i $	23	23	23	23	23	k Ω
Maximum power dissipation	P_{tot}	5,2	2,8	1,6	5,5	3,0	W



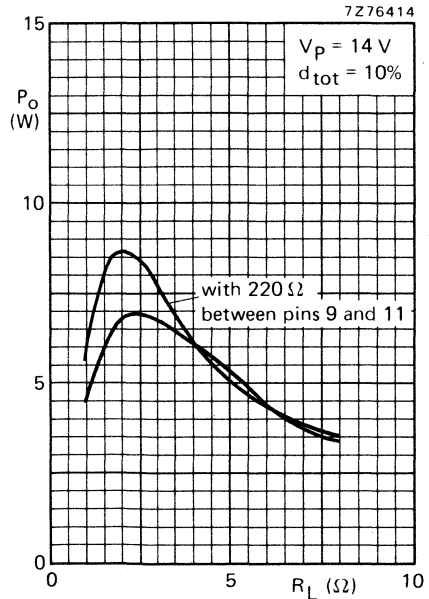
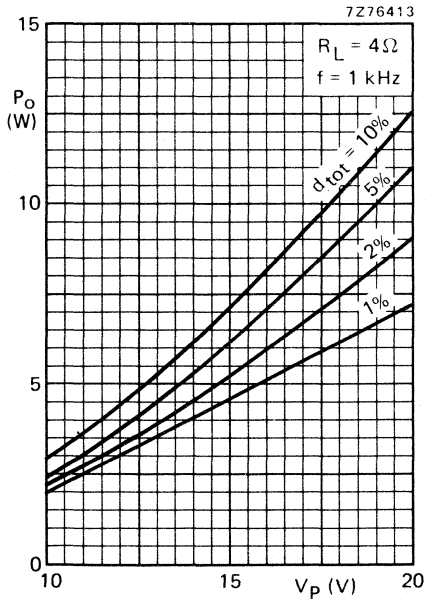
¹⁾ $P_O = 9$ W, when a resistor of 220 Ω is connected between pins 9 and 11.

APPLICATION INFORMATION (continued)

Without bootstrap



With bootstrap



MOUNTING INSTRUCTIONS

When using an external heatsink, connected to the heat spreader of the IC, the thermal power in the circuit can be reduced to a negligible value.

The optimum heatsink dimensions (blackened aluminium) for a given operating ambient temperature, can be found from the derating curves on page 3.

The fact that the thermal resistance of the encapsulation is very good, results in a relatively small heatsink for thermal power reduction: e. g. $P_O = 2 \text{ W}$ at $T_{\text{amb}} = 50 \text{ }^\circ\text{C}$ can be obtained without an external heatsink.

Two mounting methods are shown below.

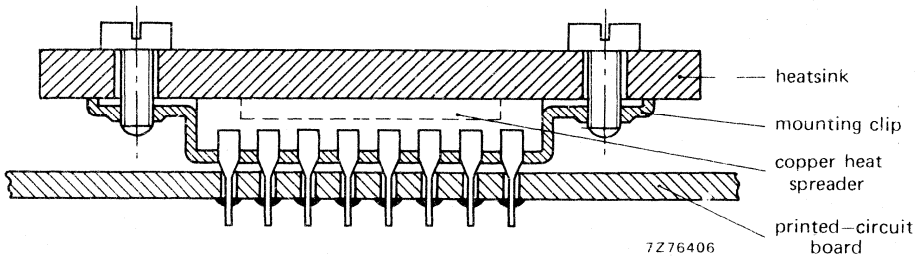
By using these methods, no extra copper area is required on the printed-circuit board, so a saving in printed-wiring area is obtained.

Mounting the external heatsink can be done by screwing or clipping.

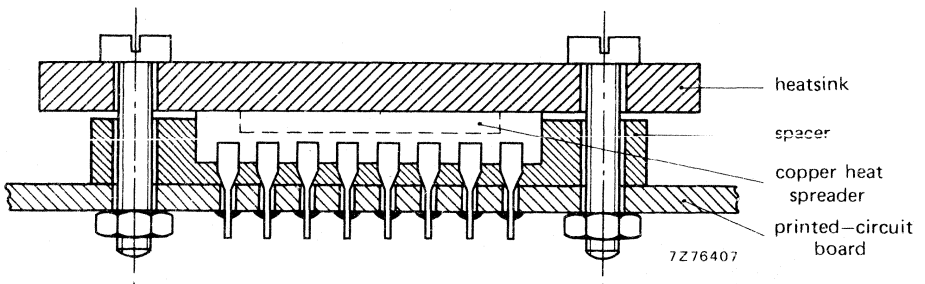
Mechanical stresses do not damage the IC.

It is recommended that a heatsink-compound be used between IC heat spreader and heatsink.

Method 1



Method 2



FREQUENCY MULTIPLEX PLL STEREO DECODER

The TDA1005 is a high quality PLL stereo decoder based on the frequency-division multiplex (f. d. m.) principle, performing:

- excellent ACI (Adjacent Channel Interference) and SCA (Storecast) rejection
- very low BFC (Beat-Frequency Components) distortion in the higher frequency region

The circuit incorporates the following features:

- with simplified peripheral circuitry the circuit can perform as a time-division multiplex (t. d. m.) decoder, for use in economic medium and low-class apparatus
- for car radios: operation at a supply voltage of 8 V
- extra pin for smooth mono/stereo take-over without "clicks"
- automatic mono/stereo switching, controlled by both pilot signal and field strength level
- low distortion in the loop resonance frequency region (≈ 300 Hz; $d_{tot} = 0, 25\%$ typ.)
- external adjustment for obtaining optimum channel separation in the complete receiver
- internal amplification: t. d. m., 6 dB; f. d. m., 10 dB
- driver for stereo indicator lamp
- externally switchable: VCO-off or mono condition
- guaranteed VCO capture range ($> 3, 5\%$ or 2, 7 kHz)

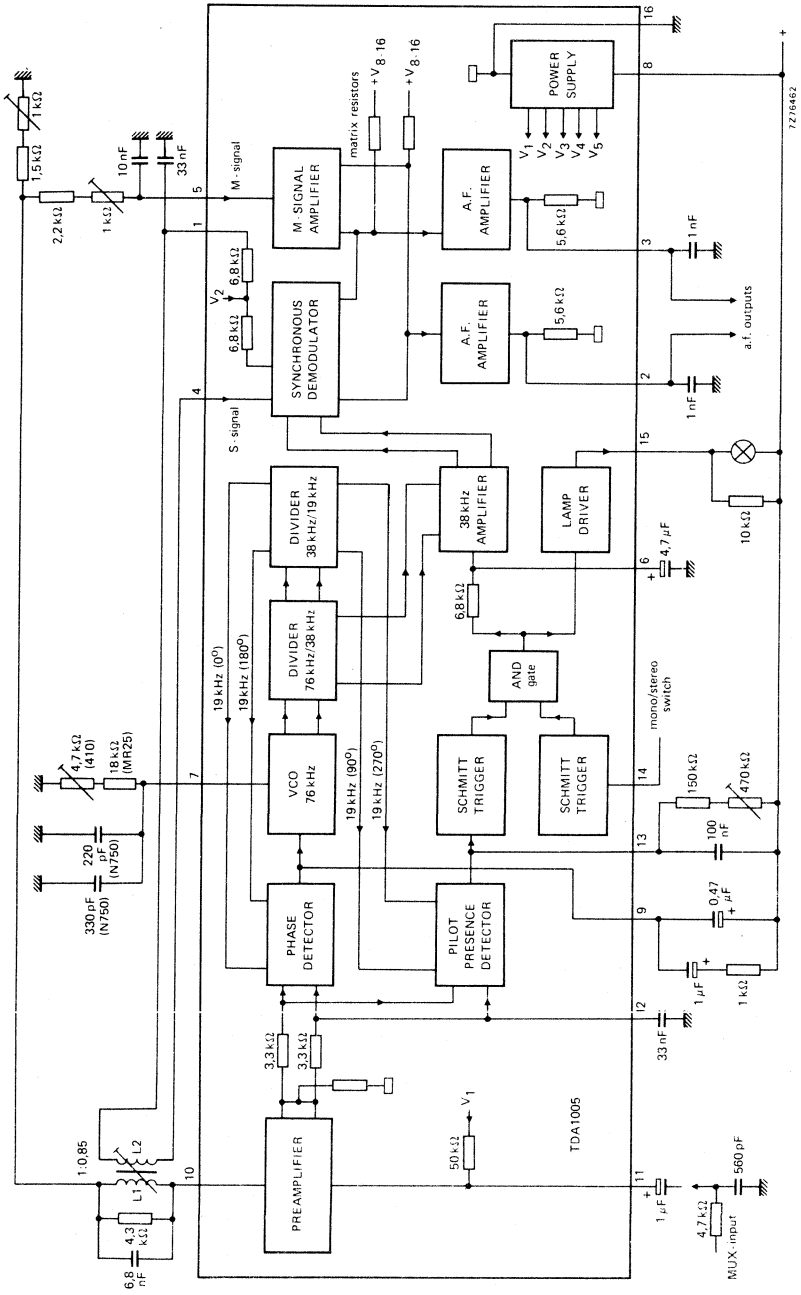
QUICK REFERENCE DATA

Supply voltage range		V_{8-16}	8 to 18	V
Supply voltage		V_{8-16}	typ. 15	V
Ambient temperature		T_{amb}	typ. 25	$^{\circ}C$
			t. d. m.	f. d. m.
Channel separation at f = 1 kHz	α	typ.	45	50 dB
Carrier suppression at f = 19 kHz	α_{19}	typ.	35	35 dB
at f = 38 kHz	α_{38}	typ.	45	40 dB
at f = 76 kHz	α_{76}	typ.	-	75 dB
ACI rejection at f = 114 kHz	α_{114}	typ.	52	70 dB
SCA rejection at f = 67 kHz	α_{67}	typ.	85	90 dB
VCO capture range		$>$	3, 5	%
Distortion: f = 1 kHz	d_{tot}	typ.	0, 25	%
at loop resonance	d_{tot}	typ.	0, 35	%
BFC suppression	d_{BFC}	$>$	40	60 dB

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage	V_{8-16}	max.	18	V
Indicator lamp voltage	V_{15-16}	max.	22	V

Currents

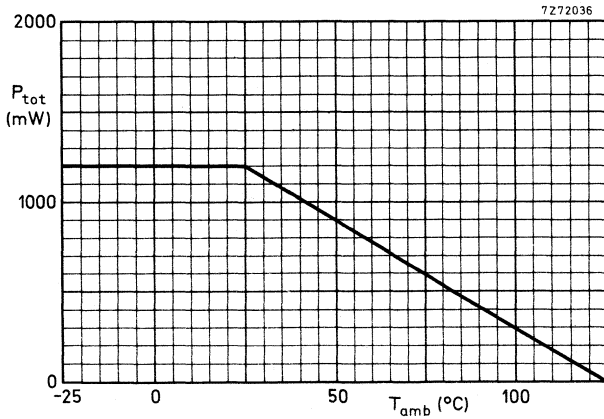
Indicator lamp current	I_{15}	max.	100	mA
Indicator lamp turn-on current (peak value)	I_{15M}	max.	200	mA

Dissipation

Total power dissipation See derating curve below

Temperatures

Storage temperature	T_{stg}	-55 to +125	°C
Operating ambient temperature (see derating curve below)	T_{amb}	-25 to +125	°C



A.C. CHARACTERISTICS and APPLICATION INFORMATION

at $T_{amb} = 25^{\circ}\text{C}$; $V_{8-16} = 15\text{ V}$ (unless otherwise specified) see circuit diagrams on pages 7 (Fig. 1 but with modified output circuitry; without filter) and 8 (Fig. 2)

	note	pin	parameter	t. d. m.	f. d. m.	unit	
Channel separation: adjustable with R ₅₋₁₀ ; see Figs. 3 and 4	1, 2	2, 3	α	>	40	40	dB
			typ.		45	50	dB
F. M. - I. F. roll-off correction range	1, 2			48 to 72	-	kHz	
Input MUX-voltage $d_{tot} < 0,35\%$; L = 1; R = 1	1, 2	11	$V_{11-16(p-p)}$	typ.	1	1	V
Input impedance		11	$ Z_i $	>	35	35	k Ω
				typ.	50	50	k Ω
Voltage gain per channel	1, 2		G_v	typ.	6	10	dB
					4, 8 to 7, 6	8, 8 to 11, 6	dB
Channel balance	1, 2		$\pm\Delta G_v$	<	1	1	dB
Output voltage (r. m. s. value) L = 1; R = 1	1, 2	2	$V_{2-16(rms)}$	typ.	0, 8	1, 1	V
		3	$V_{3-16(rms)}$	typ.	0, 8	1, 1	V
Output impedance	3	2, 3	$ Z_o $	typ.	5, 6	5, 6	k Ω
					4 to 7	4 to 7	k Ω
Distortion: see Figs. 5 and 6 $f_m = 1\text{ kHz}$ (all conditions) $f_m = 1\text{ kHz}$; L = 1; R = 1 at loop resonance: $f_m \approx 300\text{ Hz}$ L = 1; R = 0	1	2, 3	d_{tot}	typ.	0, 25	0, 2	%
	1	2, 3	d_{tot}	<	0, 35	0, 35	%
		2, 3	d_{tot}	typ.	0, 35	0, 25	%
BFC suppression: Fig. 6	10	2, 3	d_{BFC}	>	40	60	dB
Intermodulation at $f_m = 13\text{ kHz}$	6		d_{13}	typ.	55	65	dB
Carrier suppression f = 19 kHz f = 38 kHz f = 76 kHz	1		α_{19}	typ.	35	35	dB
	1		α_{38}	>	40	38	dB
				typ.	45	40	dB
	1		α_{76}	typ.	-	75	dB
ACI rejection at f = 114 kHz at f = 190 kHz	4		α_{114}	typ.	52	70	dB
	4		α_{190}	typ.	55	74	dB
SCA rejection at f = 67 kHz	5		α_{67}	typ.	85	90	dB
Ripple rejection f = 100 Hz; $V_{8-16(rms)} = 200\text{ mV}$			RR	>	40	40	dB
				typ.	50	50	dB

A.C. CHARACTERISTICS and APPLICATION INFORMATION (continued)

	note	pin	parameter	t. d. m.	f. d. m.	unit
VCO: adjustable with R ₇₋₁₆ nominal frequency	7		f _{VCO} typ.	76	76	kHz
capture range (deviation from 76 kHz centre frequency) 19 kHz pilot signal of 32 mV	7		>	3,5	3,5	%
temperature coefficient uncompensated	7		-TC typ.	800	800	ppm
compensated	7		±TC typ.	300	300	ppm
Stereo/mono switch						
19 kHz pilot-tone threshold voltage; adjustable with R ₁₃₋₈	8	11	V ₁₁₋₁₆	10 to 100	10 to 100	mV
threshold voltage at R ₁₃₋₈ = 300 kΩ		11	V ₁₁₋₁₆ typ.	23	23	mV
hysteresis	9	11	ΔV ₁₁₋₁₆ typ.	3,5	3,5	dB
Smooth take-over circuit						
full mono	10	6	V ₆₋₁₆ <	0,65	0,65	V
full stereo	10	6	V ₆₋₁₆ >	1,3	1,3	V

Notes

- $V_{11-16(p-p)} = 1 \text{ V}$; 9% pilot signal (19 kHz).
- $f_m = 1 \text{ kHz}$.
- At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.
- Measured with a composite input signal: L = R; $f_m = 1 \text{ kHz}$; 90% M-signal; 9% pilot signal; 1% spurious signal of 110 kHz (for α₁₁₄) or 186 kHz (for α₁₉₀).
ACI suppression is defined as: $20 \log \frac{V_o \text{ (at 4 kHz)}}{V_o \text{ (at 1 kHz)}}$.
- Measured with a composite input signal: L = R; $f_m = 1 \text{ kHz}$; 80% S-signal; 9% pilot signal; 10% SCA carrier (67 kHz); $d_{13} = 20 \log \frac{V_o \text{ (at 9 kHz)}}{V_o \text{ (at 1 kHz)}}$.
- Measured with a composite input signal: L = R; $f_m = 13 \text{ kHz}$; interference at 1 kHz (3 x 13 kHz - 38 kHz sub-carrier).
- See also Figs. 7 and 9. Compensated with RC network on pin 7.
Capacitor : -TC = 750 ppm.
Carbon resistor : -TC ≈ 250 ppm or metal film resistor : +TC = 100 ppm.
- Adjustable with R₁₃₋₈; see also Fig. 8; for field strength dependent input (pin 14) see page 6.
- $\Delta V_{11-16} = 20 \log \frac{V_{11-16} \text{ (mono/stereo)}}{V_{11-16} \text{ (stereo/mono)}}$.
- For additional circuitry on pin 6 see Figs. 1 and 2; for graph see Fig. 10.

D.C. CHARACTERISTICS at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{8-16} = 15\text{ V}$ (unless otherwise specified)

Supply voltage range	V_{8-16}	8 to 18	V 1)
Total current (except indicator lamp)	I_8	typ. 21	mA
Power dissipation (operating) at lamp current $I_{15} = 100\text{ mA}$; $V_{8-16} = 18\text{ V}$	P_{tot}	< 570	mW
Saturation voltage of lamp driver at $I_{15} = 100\text{ mA}$	V_{15-16}	typ. 0,9	V
Maximum lamp driver voltage	V_{15-16}	< 22	V
Switching voltage: to mono	V_{14-16}	> 1,2	V 2)
to stereo	V_{14-16}	< 0,65	V
hysteresis	V_{14-16}	typ. 0,2	V

APPLICATION NOTES1. Switching-off the VCO

If the internal gain is used with AM-reception, the VCO can be switched off by connecting pin 9 via a 100 k Ω resistor to ground (no h. f. signal on the leads), or connecting pin 7 to ground.

2. Mono button

The decoder can be switched to the mono-position by connecting pin 12 to ground. The VCO then remains operational so this possibility cannot be used with AM-reception.

1) At supply voltages of 8 to 11 V, resistors of 5, 6 k Ω have to be connected from ground to pins 2 and 3.

2) Maximum voltage for safe operation: $V_{14-16} < 6\text{ V}$.

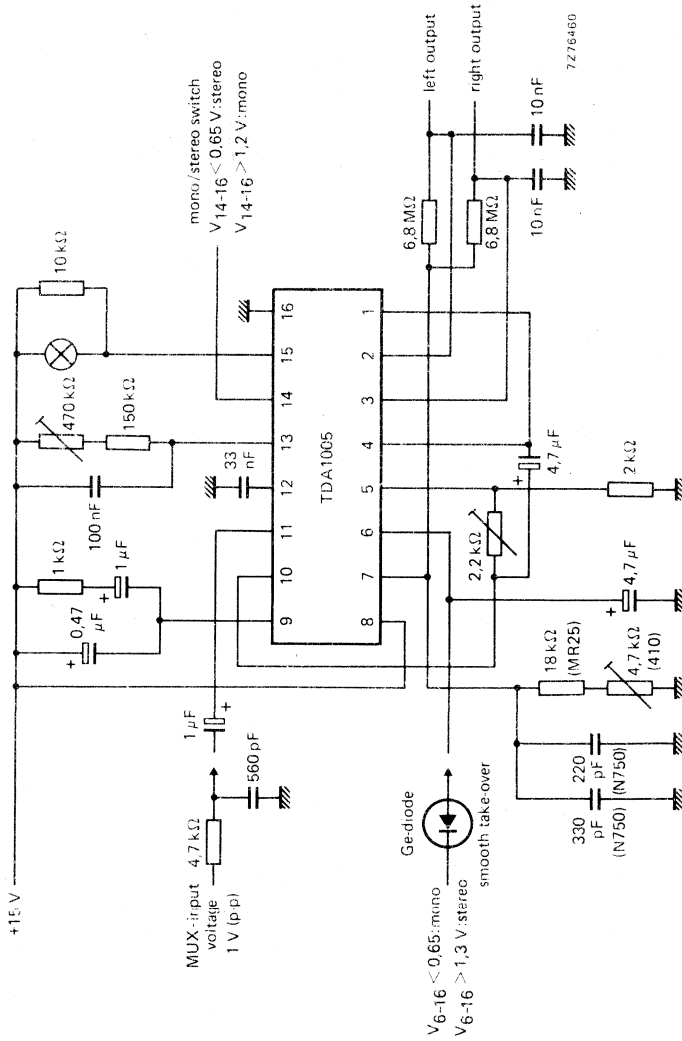


Fig.2 Time-division multiplex stereo decoder.

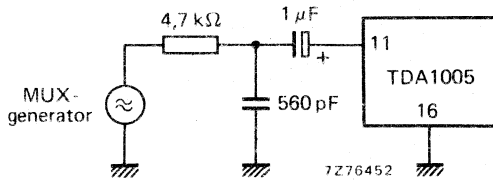
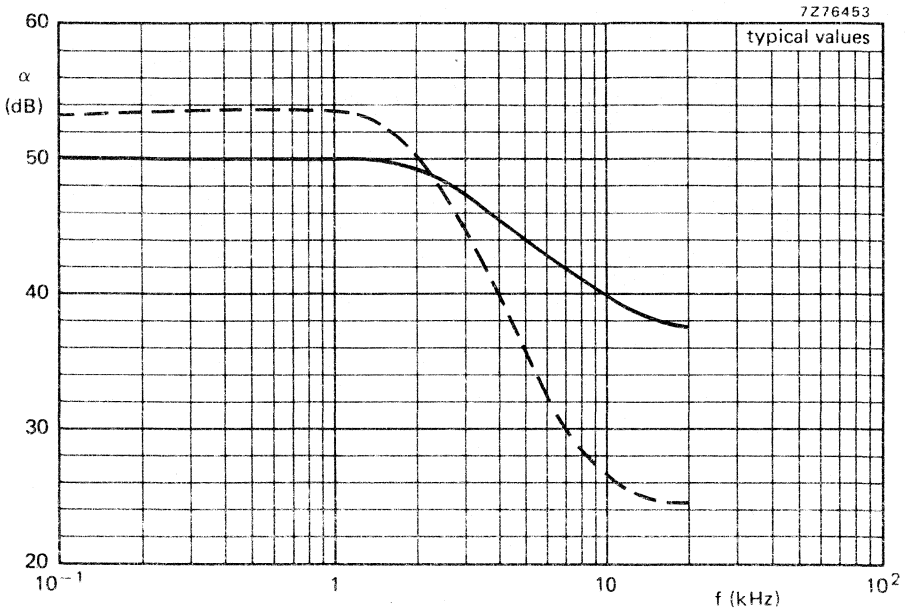


Fig. 3 Channel separation as a function of frequency.

- time-division multiplex system
- - - frequency-division multiplex system

Conditions: $V_{8-16} = 15 \text{ V}$; $V_{11-16(p-p)} = 1 \text{ V}$; optimized only for $f = 1 \text{ kHz}$;

additional adjustment at $f = 5 \text{ kHz}$ results in about 10 dB improvement.

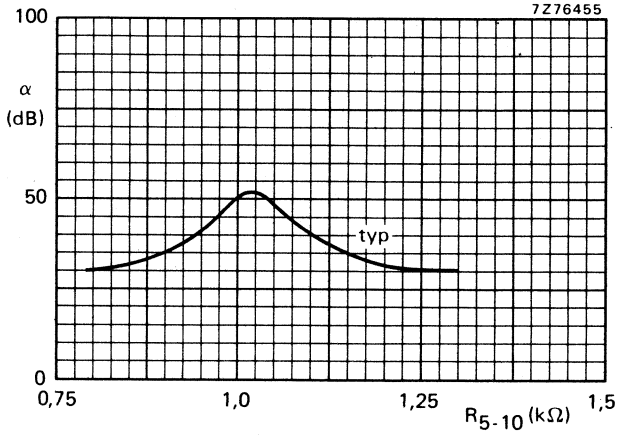


Fig. 4 Channel separation as a function of resistance between pins 5 and 10 (t. d. m.).
For test circuit see page 9.

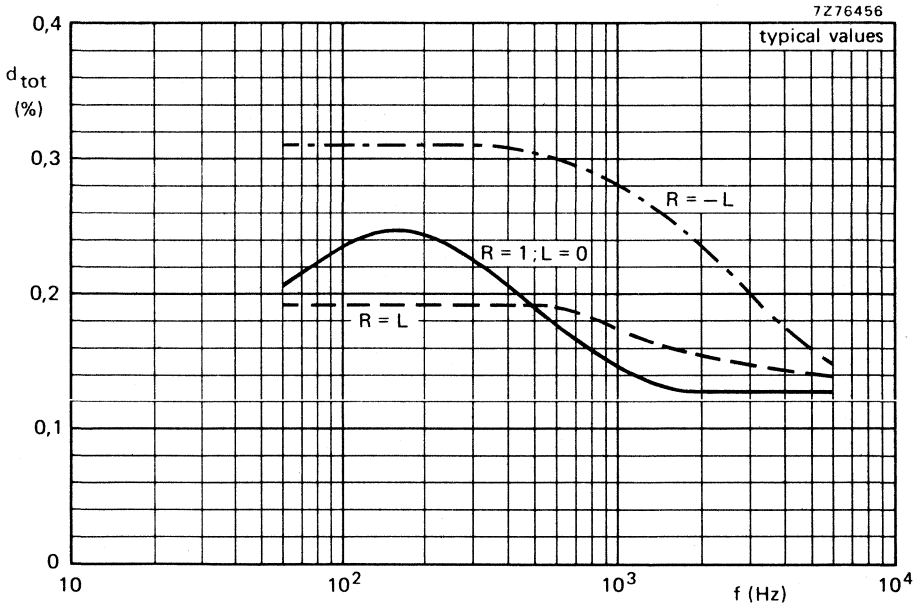


Fig. 5 Distortion as a function of audio frequency (f. d. m.).

Conditions: $V_{8-16} = 15 V$; $V_{2-16} = V_{3-16} = 1 V$ (r. m. s.).

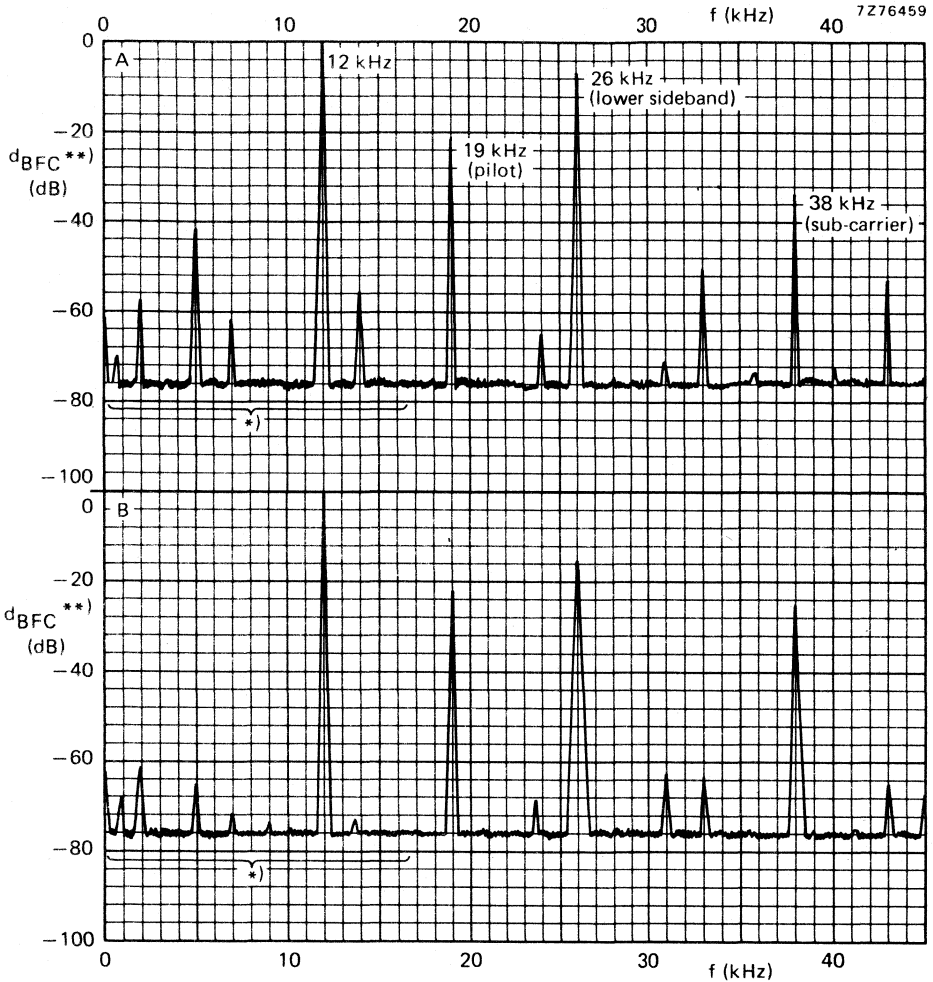


Fig. 6
 A. Spectrum at the decoder outputs (t. d. m.).
 B. Spectrum at the decoder outputs (f. d. m.).

Conditions : $V_{11-16(p-p)} = 1 \text{ V}$; $R = 1$; $L = 0$

for $f = 12 \text{ kHz}$: $m = 90\%$

for $f = 19 \text{ kHz}$: $m = 10\%$

*) Audible interferences (BFC-distortion) and desired 12 kHz signal.

$$***) d_{BFC} = 20 \log \frac{V_{BFC}}{V(\text{at } 12 \text{ kHz})}$$

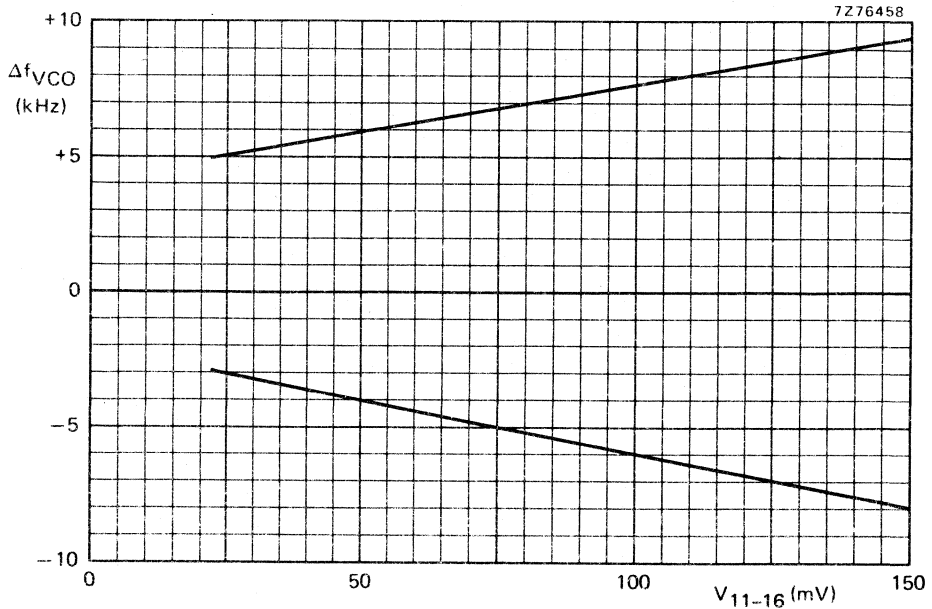


Fig. 7 Typical values of the capture range of the oscillator as a function of the pilot threshold voltage at MUX-input (pin 11).

Conditions: $V_{8-16} = 15$ V; pilot threshold voltage adjusted to $V_{11-16} = 30$ mV

$\Delta f_{VCO} = f_{VCO} - 76$ kHz in which,

f_{VCO} = modulated, free-running oscillator frequency

Δf_{VCO} = max. f_{VCO} deviation which will be captured if pilot signal (pin 11) is switched-on.

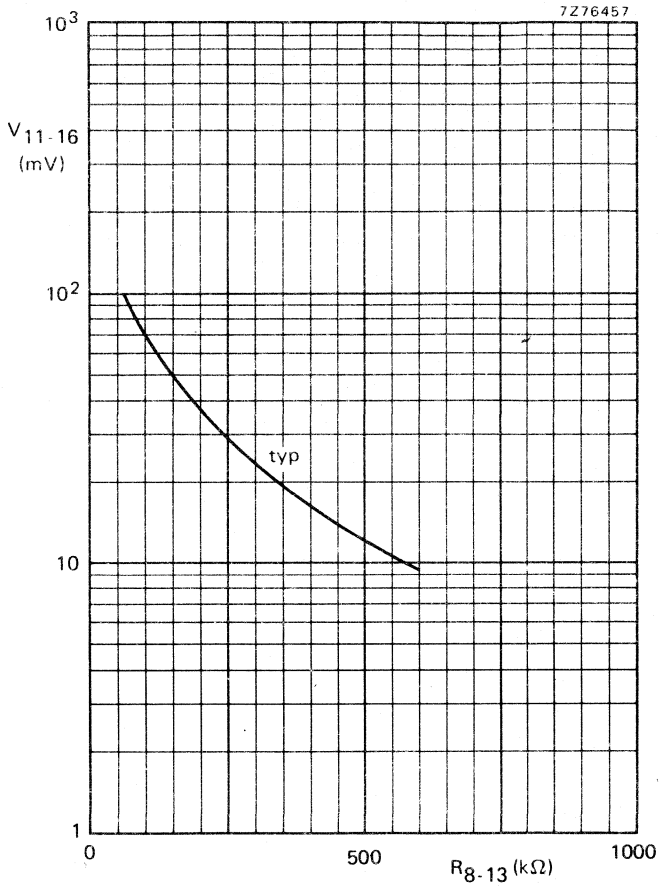


Fig. 8 Pilot input voltage switching level as a function of resistance between pins 8 and 13.

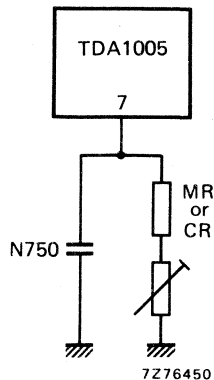
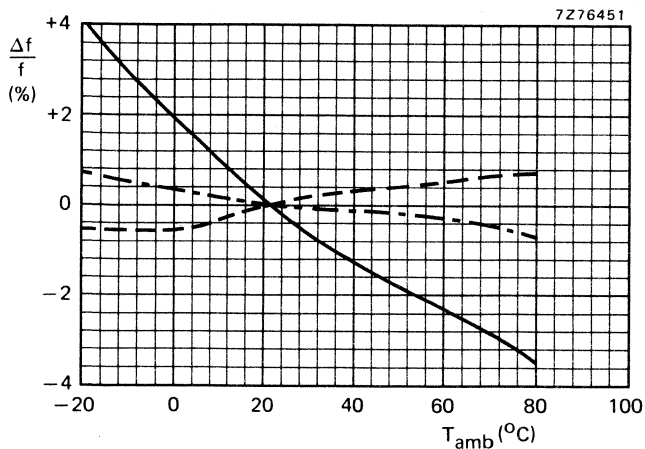


Fig. 9 Relative frequency deviation as a function of ambient temperature (VCO free-running).

- pin 7 open
- - - pin 7 connected with N750 capacitor and carbon resistor
- · - · - pin 7 connected with N750 capacitor and metal-film resistor.

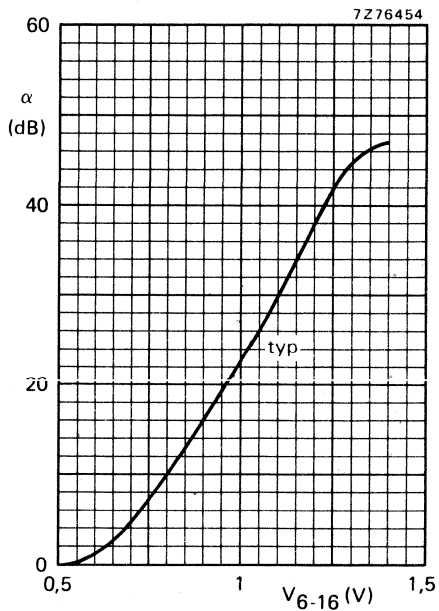


Fig. 10 Channel separation as a function of V_{6-16} at 1 kHz (smooth take-over).

MOTOR REGULATOR WITH AUTOMATIC TAPE-END INDICATOR

The TDA1006 is for use in car radio tape-decks.

The circuit incorporates the following functions:

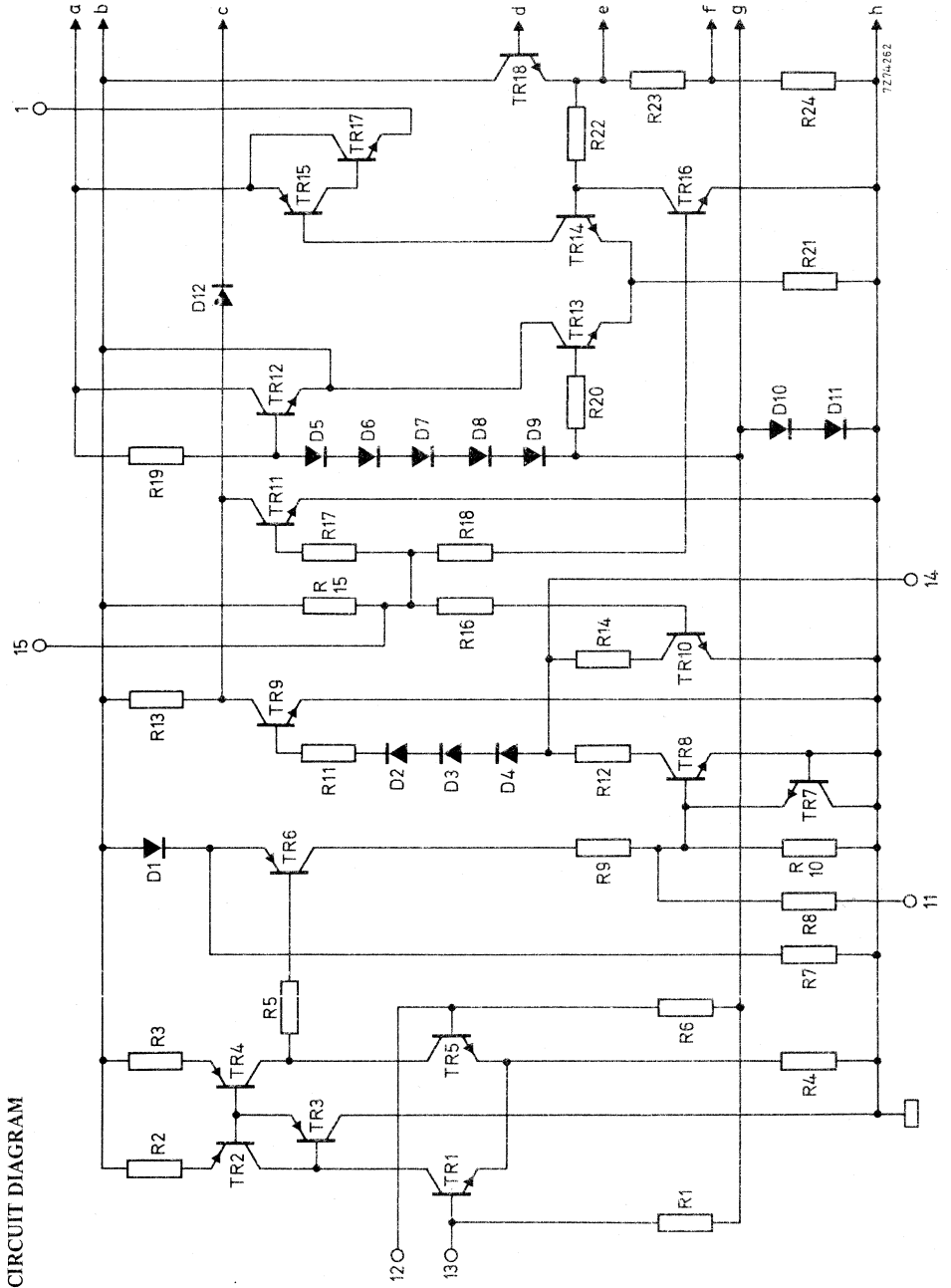
- capstan motor speed control;
- an electronic motor stop in conjunction with hysteresis slip-coupling or commutator pulses;
- an automatic switch from playback to radio at tape-end;
- playback indication with lamp;
- tape-end indication with intermittent light.

QUICK REFERENCE DATA

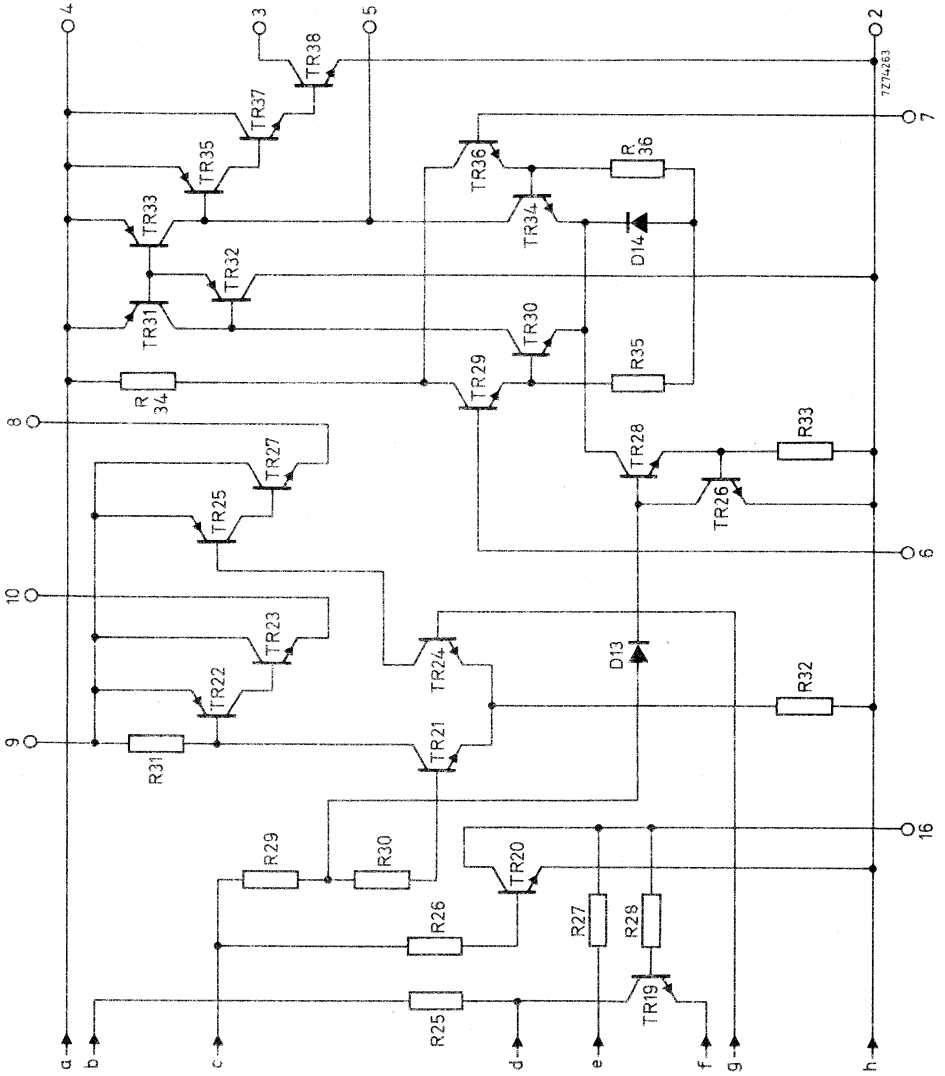
Supply voltage range	V_p	6 to 22	V
Ambient temperature	T_{amb}	typ. 25	°C
Supply voltage	V_p	typ. 14	V
<hr style="border-top: 1px dashed black;"/>			
<u>Motor regulator</u>			
Current consumption ($R_{3-4} = 7,5 \text{ k}\Omega$)			
radio	I_4	typ. 9	mA
playback ($I_1 = 0$)	I_4	typ. 12	mA
playback	I_4	typ. 52	mA
tape-end	I_4	typ. 32	mA
Operating motor current	I_3	typ. 200	mA
Supply voltage rejection	$\Delta V_{3-2}/\Delta V_{4-2}$	typ. 1	mV/V
<u>Automatic stop circuit</u>			
Input current	I_{14}	> 25	μA
Input voltage at commutator	V_{11-2}	-6 to +6	V

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic power.



CIRCUIT DIAGRAM



|||||

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

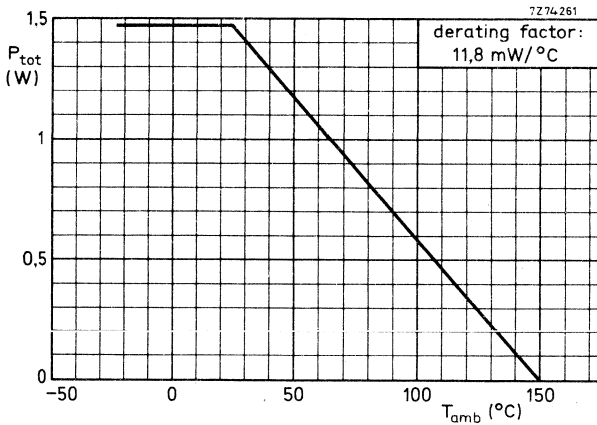
Supply voltage on: pin 4	V_{4-2}	max.	24	V
pin 9	V_{9-2}	max.	24	V

Currents

Output current at: pin 1 (d. c. value)	$-I_1$	max.	40	mA
(peak value)	$-I_{1M}$	max.	100	mA
pin 3 (d. c. value)	I_3	max.	250	mA
(non-repetitive peak value)	I_{3SM}	max.	600	mA
pin 8 (d. c. value)	$-I_8$	max.	45	mA
(peak value)	$-I_{8M}$	max.	80	mA
pin 10 (d. c. and peak value)	$-I_{10}$	max.	20	mA

Temperatures

Storage temperature	T_{stg}	-65 to +150	°C
Operating ambient temperature see power derating curve below	T_{amb}	-25 to +150	°C



CHARACTERISTICS at $V_P = 14$ V; $T_{amb} = 25$ °C unless otherwise specified (see test circuit on page 7).

Supply voltage range (pins 4 and 9)	V_P	6 to 22	V
<u>Motor regulator</u>			
Current consumption ($R_{3-4} = 7.5$ k Ω)			
radio	I_4	typ. 9	mA
playback ($I_1 = 0$)	I_4	{ typ. 12 9,5 to 17	{ mA mA
playback	I_4	typ. 52	mA
tape-end	I_4	typ. 32	mA
Input offset voltage at $I_3 = 3$ mA	$ V_{7-6} $	{ typ. 2 < 8	{ mV mV
Input voltage range (common mode)	$V_{6-2}; V_{7-2}$	2, 4 to $V_P - 0,2$	V
Input bias current	$I_6; I_7$	{ typ. 80 < 700	{ nA nA
Input sensitivity (for $\Delta I_3 = 100$ mA)	ΔV_{7-6}	< 13	mV
Operating voltage of TR38 at $I_{3SM} = 600$ mA	V_{3-2}	{ typ. 900 < 1800	{ mV mV
Supply voltage rejection	$\Delta V_{3-2} / \Delta V_{4-2}$	typ. 1	mV/V
Operating motor current	I_3	{ typ. 200 < 250	{ mA mA
<u>Automatic motor "stop" circuit</u>			
Input current	I_{14}	> 25	μ A
Voltage when TR20 is not conducting (pin 16; peak-to-peak value)	$V_{16-2}(p-p)$	0.9 to 1,4	V
Voltage when TR20 is conducting (pin 16)	V_{16-2}	< 250	mV
Input voltage at commutator (pin 11)	V_{11-2}	-6 to +6	V
<u>Stop signal amplifier</u>			
Differential input voltage	V_{12-13}	{ typ. 3,5 2,6 to 4,4	{ mV mV
Voltage without input signal	V_{11-2}	85 to 170	mV
Input voltage (r. m. s. value)	$V_{12-13}(rms)$	> 10	mV

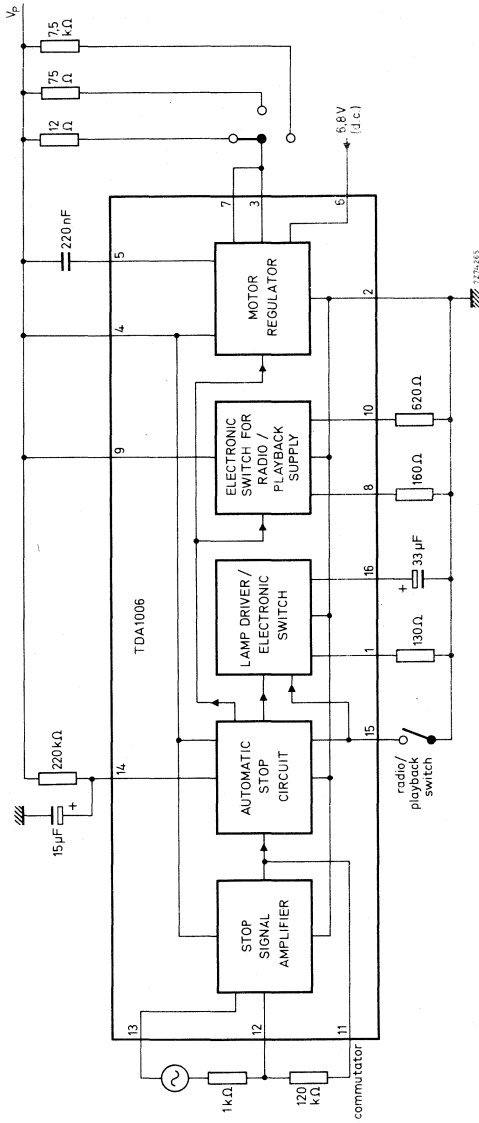
CHARACTERISTICS (continued)Radio and preamplifier supply

Radio supply current (d. c.)	$-I_8$	\leq	45	mA
Saturation voltage at $-I_{8M} = 80$ mA	V_{8-9}	\leq	1,35	V
Preamplifier supply current (d. c.)	$-I_{10}$	\leq	20	mA
Saturation voltage at $-I_{10} = 20$ mA	V_{10-9}	\leq	1,2	V

Lamp driver

Output current (d. c.)	$-I_1$	\leq	40	mA
Saturation voltage at $-I_{1M} = 100$ mA	V_{4-1}	\leq	1,85	V
D. C. voltage level	V_{15-2}		0,75 to 1,2	V

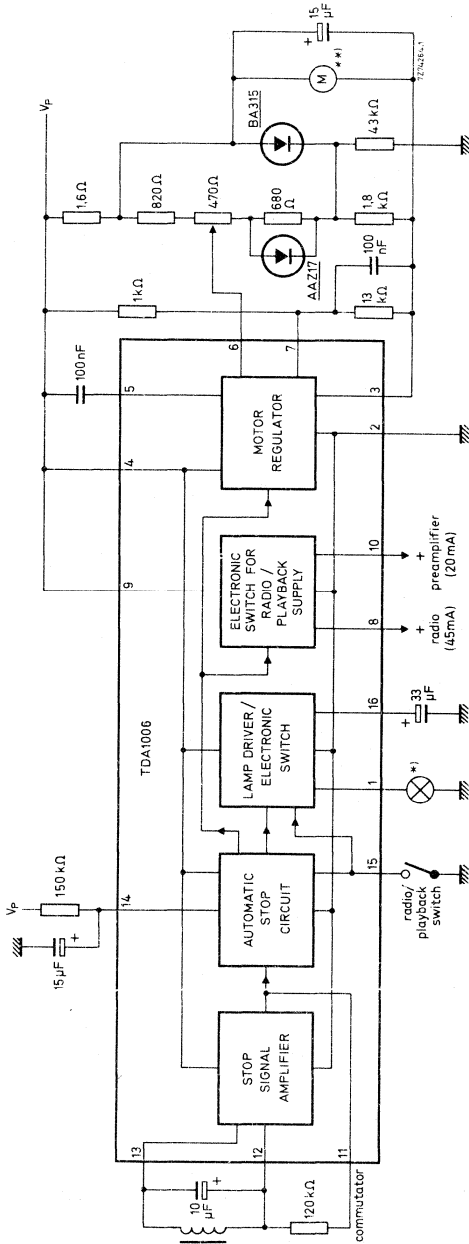
TEST CIRCUIT (for characteristics see pages 5 and 6)



7274-565



APPLICATION INFORMATION



- *) Radio : lamp off
- Playback : lamp on
- Tape-end : intermittent light
- **) D.C. motor
- E₃₀₀₀ = 7, 2 to 8, 3 V
- R_m = 27 Ω

2 x 6 W STEREO AUDIO POWER AMPLIFIER

This stereo audio power IC is intended for use as a low frequency class-B amplifier for mains-fed and battery supplied record players, tape recorders and domestic radio receivers.

The maximum current is based on 6 W output power at 10% distortion into a 4 Ω load impedance. The maximum supply voltage is such that 6 W can be delivered into a speaker impedance of 8 Ω .

The circuit **philosophy** is based on a low-cost total amplifier and use in a.c./d.c. apparatus is taken into account. The number of external components must, therefore, be kept to an absolute minimum, and the current consumption must be low.

This IC contains the complete stereo output power function, in addition to control functions. In practical applications the following functions have to be adapted:

1. An emitter-follower input stage is preferred for adaption to a ceramic pick-up.
2. For radio applications, an extra input stage has to be used for gain improvement.
3. For tape recorders an additional preamplifier is required for tone correction.

For a good adaption to one of these external input stages, the IC input impedance is 45 k Ω . The voltage gain of 39 dB provides an input sensitivity of 50 mV for an output power of 6 W into a 4 Ω load. This gain allows control losses of about 16 dB, for a typical sensitivity requirement of 350 mV. The internally limited frequency response provides good stability.

The output power can be increased by using the bootstrap arrangement; however, the circuit is designed for maximum performance without the bootstrap capacitor.

The advantages of a monolithic stereo power amplifier are that only one encapsulation has to be mounted. No insulation of the heatsink is required.

The circuit has the following additional features:

- low number of external components
- thermal protection
- no cross-over distortion
- low thermal resistance
- short-circuit protection of the load for supply voltages up to 16 V

QUICK REFERENCE DATA see page 2.

PACKAGE OUTLINE (see general section)

16-lead DIL: plastic power (SOT-69B).

QUICK REFERENCE DATA

Supply voltage (pins 12 and 13)	V_P	5 to 24	V
D.C. output current (peak value)	I_{OM}	< 2,5	A
Output power at $d_{tot} = 10\%$; per channel			
at $V_P = 16\text{ V}; R_L = 8\ \Omega$	P_O	typ. 3.4	W
at $V_P = 16\text{ V}; R_L = 4\ \Omega$	P_O	typ. 6	W
Total harmonic distortion at $P_O < 2,5\text{ W}; R_L = 4\ \Omega$	d_{tot}	typ. 0.4	%
Input impedance	$ Z_i $	typ. 45	k Ω
Total quiescent current at $V_P = 9\text{ V}$	I_{tot}	typ. 35	mA
at $V_P = 16\text{ V}$	I_{tot}	typ. 50	mA
Sensitivity at $P_O = 1\text{ W}; R_L = 4\ \Omega$	V_i	typ. 23	mV
Channel separation			
at $f = 1\text{ kHz}; V_O = 1\text{ V}; R_S = 600\ \Omega$	α	typ. 45	dB
Operating ambient temperature	T_{amb}	-25 to +150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_P max. 24 V

Currents

Non-repetitive peak output current I_{OSM} max. 4 A

Repetitive peak output current I_{ORM} max. 2,5 A

Power dissipation

Total power dissipation see derating curve on page 3

Temperatures

Operating ambient temperature T_{amb} -25 to +150 $^{\circ}\text{C}$

Storage temperature T_{stg} -55 to +150 $^{\circ}\text{C}$

Short-circuiting

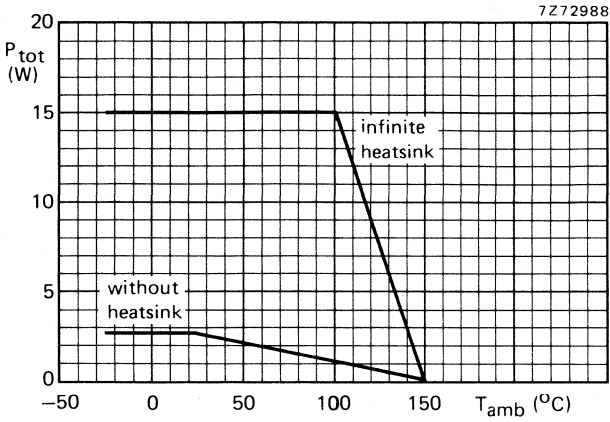
A.C. short-circuit of load impedance during sine-wave signal drive at $V_P = 16\text{ V}$ t_{sc} max. 100 hours

THERMAL RESISTANCE (The power derating curve below is based on the following data)

From junction to case $R_{th\ j-c} = 3,3\ ^\circ C/W$

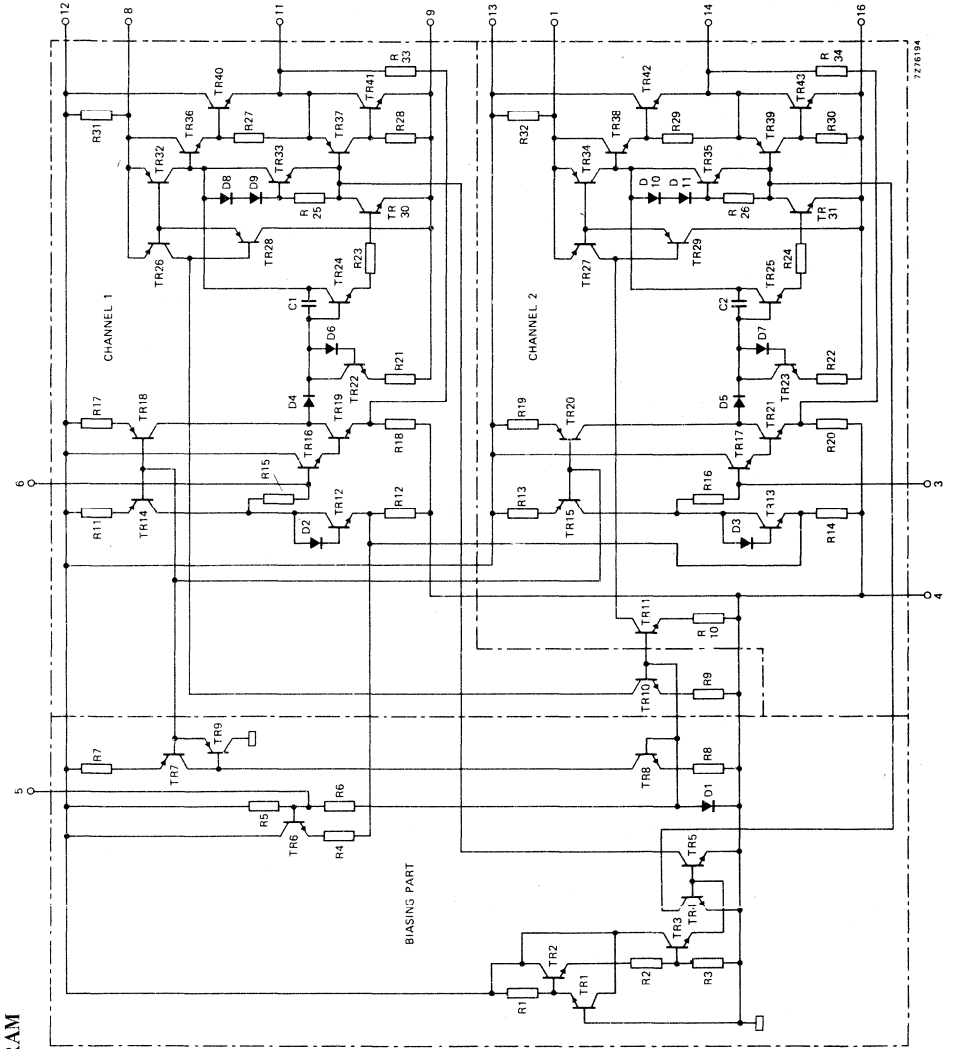
From junction to ambient $R_{th\ j-a} = 45\ ^\circ C/W$

Total power dissipation



DEVELOPMENT SAMPLE DATA





CIRCUIT DIAGRAM

CHARACTERISTICS

D.C. characteristics

Supply voltage range	V_P	5 to 24	V
Output current (peak value)	I_{OM}	< 2,5	A
Total quiescent current (both channels) at $V_P = 9$ V	I_{tot}	typ.	35 mA
		<	55 mA
at $V_P = 16$ V	I_{tot}	typ.	50 mA
		<	80 mA

A.C. characteristics at $T_{amb} = 25$ °C; $V_P = 16$ V; $R_L = 4$ Ω ; $f = 1$ kHz unless otherwise specified; see also test circuits on page 6.

A.F. output power per channel at $d_{tot} = 10\%$ ¹⁾	P_O	typ.	3,4	W
		>	5,5	W
at $V_P = 16$ V; $R_L = 8$ Ω	P_O	typ.	6,0	W
at $V_P = 16$ V; $R_L = 4$ Ω				
Voltage gain	G_V	typ.	39	dB
			37 to 41	dB
Difference in gain of both channels	ΔG_V	<	1	dB
Difference in d.c. output voltage of both channels	ΔV_O	typ.	0,2	V
Total harmonic distortion at $P_O = 2,5$ W	d_{tot}	typ.	0,4	%
		<	1,0	%
Input impedance	$ Z_i $	>	30	k Ω
		typ.	45	k Ω
Channel separation at $V_O = 1$ V; $R_S = 600$ Ω	α	typ.	45	dB
Signal-to-noise ratio at $P_O = 50$ mW (note 2); $R_S = 5$ k Ω	S/N	>	53	dB
		typ.	60	dB
$R_S = \infty$	S/N	typ.	56	dB
Ripple rejection at $f = 100$ Hz; $R_S = 5$ k Ω	RR	typ.	38	dB ³⁾

¹⁾ Measured with an ideal coupling capacitor to the speaker load.

²⁾ Bandwidth of 60 Hz to 15 kHz is defined as being the -3 dB points of the filter with slopes of 12 dB per octave.

³⁾ The ripple rejection is defined as: $20 \log \frac{V_{PR}}{V_{OR}}$ in which

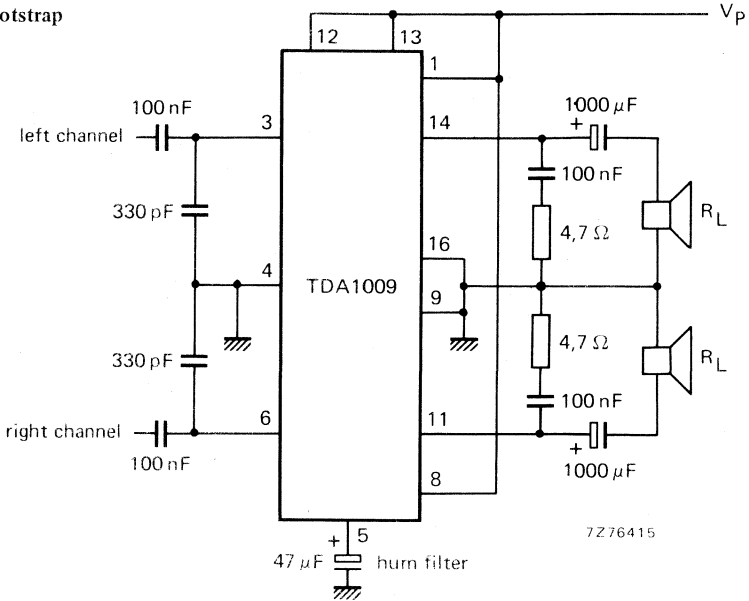
V_{PR} = ripple voltage on supply line ($V_{PR} = 500$ mV)

V_{OR} = ripple voltage across speaker load.

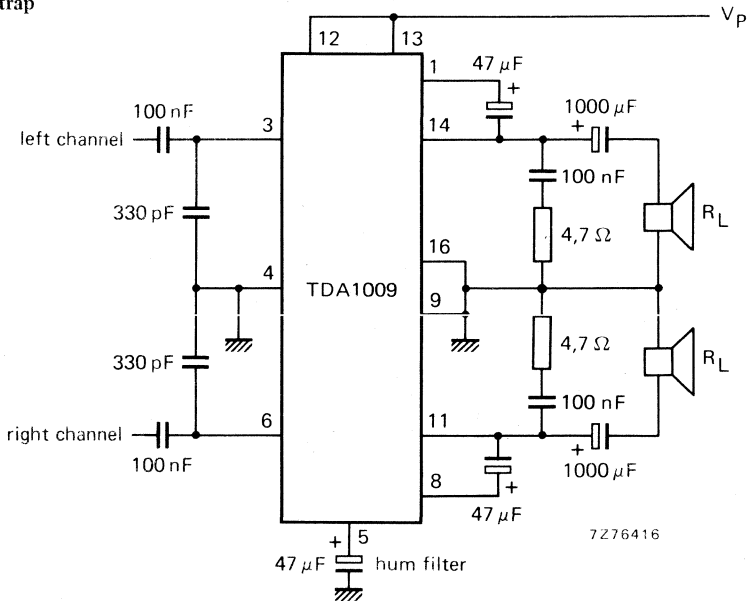
TDA1009

APPLICATION INFORMATION (test circuits)

Without bootstrap



With bootstrap



DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION (continued)

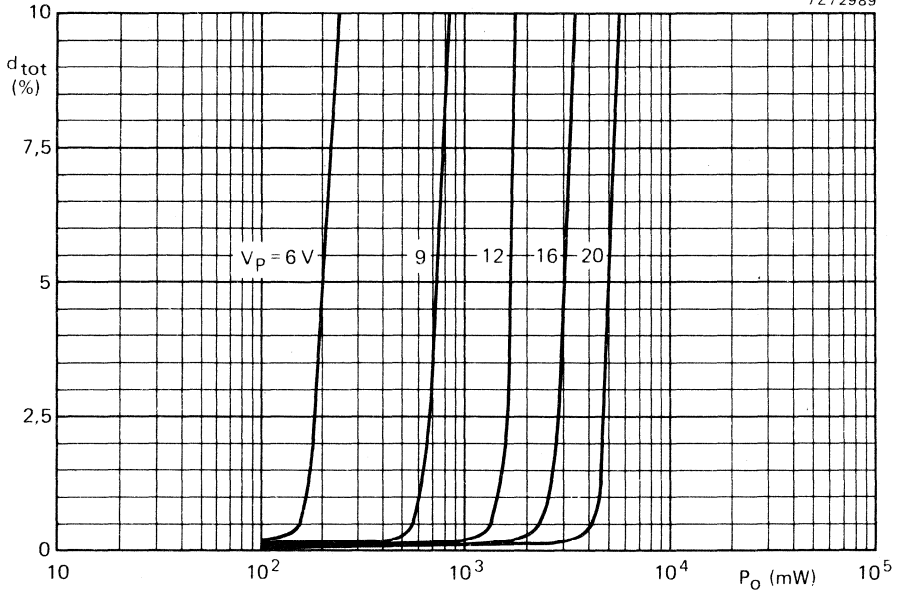
	V _p		9		12		14		16		20		V
	4	8	4	8	4	8	4	8	4	8	4	8	Ω
Supply voltage													V
Load resistance													Ω
Total quiescent current (2 channels)	35												61
Output power at $c_{tot} = 10\%$ with bootstrap	2.0		4.0		2.2		5.5		7.1		4.1		6.6
without bootstrap	1.5		3.1		1.7		4.4		6.0		3.4		5.7
Distortion at $P_0 = 2.5$ W with bootstrap	-		1		-		0.7		0.5		0.4		0.25
without bootstrap	-		3		-		0.55		0.4		0.35		0.15
Sensitivity for $P_0 = 1$ W	23		23		32		23		23		32		32
Ripple rejection at $f = 100$ kHz	←												38
Noise output voltage at $B = 60$ Hz to 15 kHz at $R_S = 5$ kΩ	←												0.27
at $R_S = \infty$	←												0.45
Input impedance	←												45
Channel separation	←												45
Maximum power dissipation	2.25	1.1	4	1.9	5.5	2.6	7.2	3.3	5				W

All values per channel unless otherwise specified.

APPLICATION INFORMATION (continued)

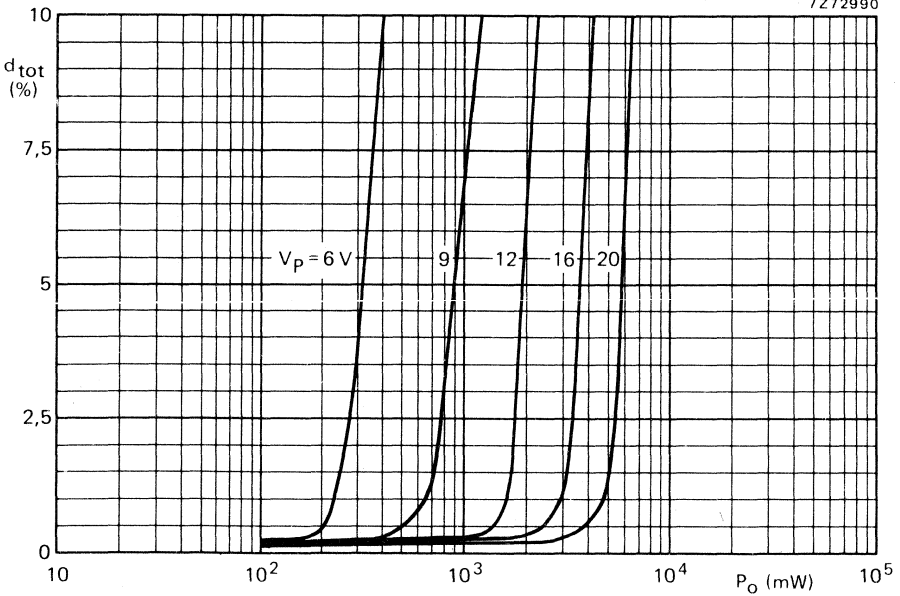
Without bootstrap; $R_L = 8 \Omega$

7Z72989



With bootstrap; $R_L = 8 \Omega$

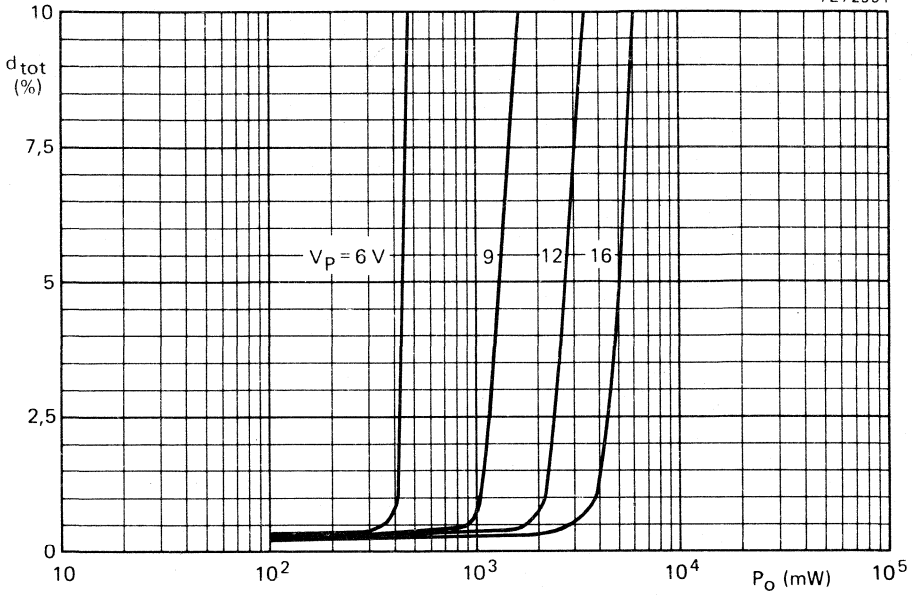
7Z72990



APPLICATION INFORMATION (continued)

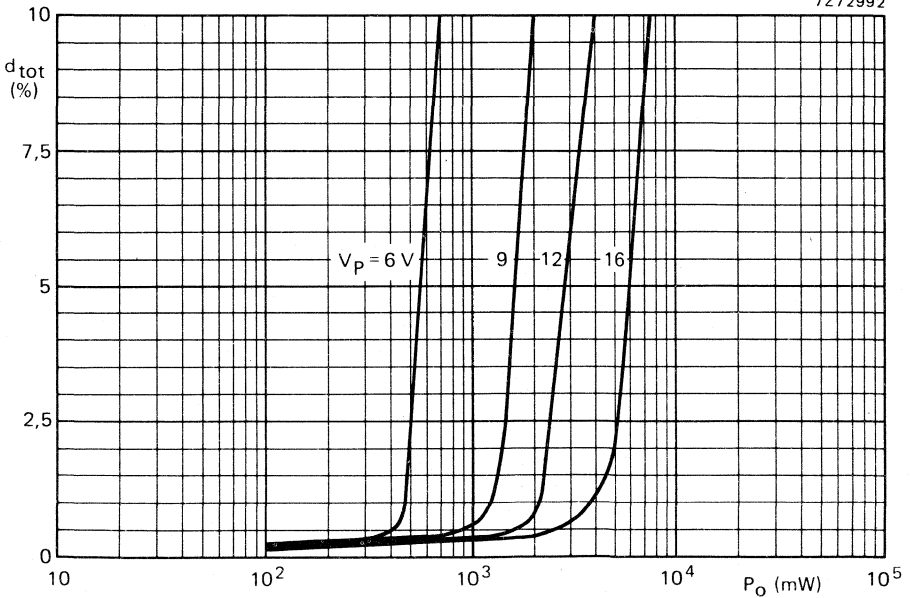
Without bootstrap; $R_L = 4 \Omega$

7272991



With bootstrap; $R_L = 4 \Omega$

7272992



DEVELOPMENT SAMPLE DATA



MOUNTING INSTRUCTIONS

When using an external heatsink, connected to the heat spreader of the IC, the thermal power in the circuit can be reduced to a negligible value.

The optimum heatsink dimensions (blackened aluminium) for a given operating ambient temperature, can be found from the derating curves on page 3.

The fact that the thermal resistance of the encapsulation is very good, results in a relatively small heatsink for thermal power reduction; e.g. $P_o = 2 \text{ W}$ at $T_{amb} = 50 \text{ }^\circ\text{C}$ can be obtained without an external heatsink.

Two mounting methods are shown below.

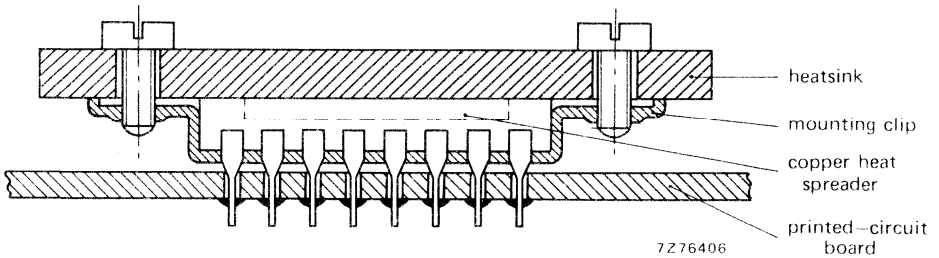
By using these methods, no extra copper area is required on the printed-circuit board, so a saving in printed-wiring area is obtained.

Mounting the external heatsink can be done by screwing or clipping.

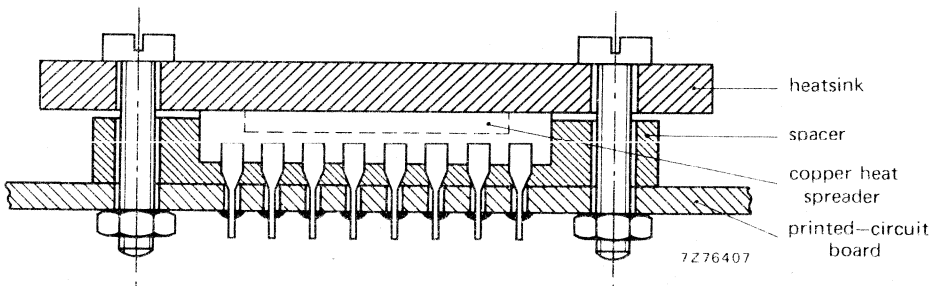
Mechanical stresses do not damage the IC.

It is recommended that a heatsink-compound be used between IC heat spreader and heatsink.

Method 1



Method 2



6 W AUDIO POWER AMPLIFIER

in a single in-line package

The TDA1010 is a monolithic integrated circuit in a 9-lead single in-line plastic package intended as a low-cost amplifier that can deliver 6 W output power into a 4 Ω load or a 2 Ω load.

This device is primarily suitable for car radio applications. The maximum allowable supply voltage of 20 V makes it also suitable for domestic radios, tape recorders and record players.

Special features are :

- single in-line (SIL) construction for easy mounting
- high output power
- low-cost external components
- good ripple rejection
- thermal protection
- **separated** preamplifier and power amplifier

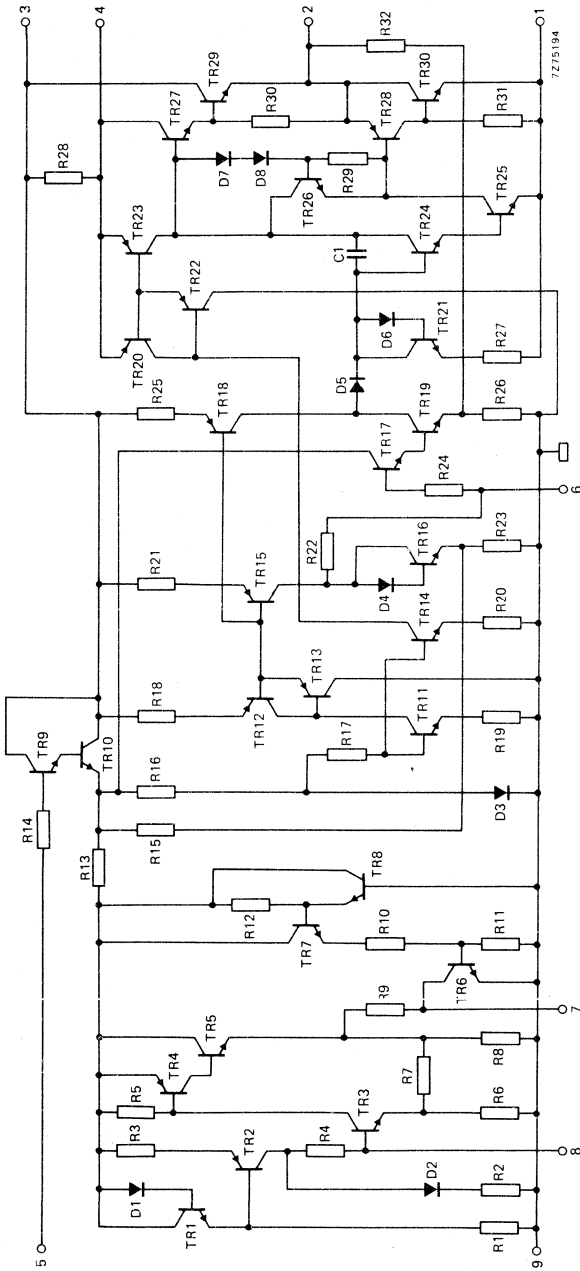
QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 20	V
D. C. output current (peak value)	I_{OM}	max. 2,5	A
Output power at $d_{tot} = 10\%$			
at $V_P = 14$ V; $R_L = 8$ Ω	P_O	typ. 3,3	W
at $V_P = 14$ V; $R_L = 4$ Ω	P_O	typ. 6	W
at $V_P = 14$ V; $R_L = 2$ Ω	P_O	typ. 6	W
Total harmonic distortion at $P_O < 3$ W; $R_L = 4$ Ω	d_{tot}	typ. 0,3	%
Input impedance: preamplifier	$ Z_i $	typ. 30	k Ω
power amplifier	$ Z_i $	typ. 20	k Ω
Total quiescent current at $V_P = 14$ V	I_{tot}	typ. 25	mA
Sensitivity at $P_O = 1$ W; $R_L = 4$ Ω	V_i	typ. 4	mV
Operating ambient temperature	T_{amb}	-25 to +150	$^{\circ}$ C
Storage temperature	T_{stg}	-55 to +150	$^{\circ}$ C

PACKAGE OUTLINE (see general section)

9-lead SIL; plastic.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_P max. 24 V

Currents

Non-repetitive peak output current I_{OSM} max. 3 A

Repetitive peak output current I_{ORM} max. 2,5 A

Power dissipation

Total power dissipation see derating curve below

Temperatures

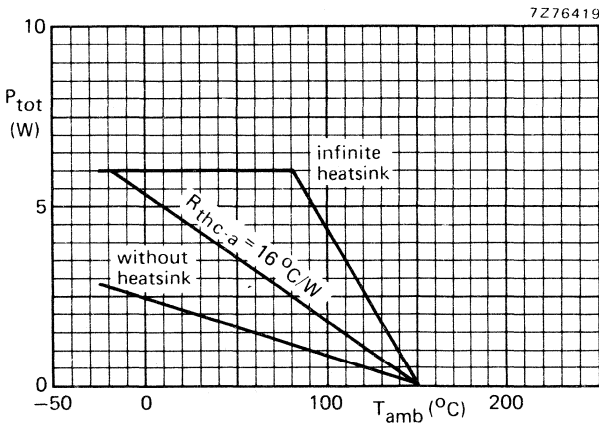
Storage temperature T_{stg} -55 to +150 °C

Operating ambient temperature T_{amb} -25 to +150 °C

Short-circuiting

A. C. short-circuit duration of load impedance during sine-wave signal drive; without heatsink at $V_P = 14$ V

t_{sc} max. 100 hours



The **single** in-line encapsulation offers a solution for a simple and low-cost heatsink connection. The thermal resistance of the encapsulation is: $R_{th j-c} \approx 12$ °C/W. For a 6 W application into a load impedance of 4 Ω, the maximum dissipation is 3,2 W. This means the thermal resistance of the heatsink (at $T_{amb} = 60$ °C) is:

$$R_{th c-a} = \frac{T_{j max} - T_{amb max}}{P_{tot}} - R_{th j-c} = \frac{150 - 60}{3,2} - 12 = 16 \text{ °C/W.}$$

DEVELOPMENT SAMPLE DATA



CHARACTERISTICS

D.C. characteristics

Supply voltage range	V_P	6 to 20	V
Output current (peak value)	I_{OM}	< 2,5	A
Total quiescent current at $V_P = 14$ V	I_{tot}	typ.	25 mA
		<	50 mA

A.C. characteristics at $T_{amb} = 25$ °C; $V_P = 14$ V; $R_L = 4$ Ω ; $f = 1$ kHz unless otherwise specified; see also test circuit on page 5.

A.F. output power at $d_{tot} = 10\%$ ¹⁾

at $V_P = 14$ V; $R_L = 4$ Ω : without bootstrap

P_O typ. 5.4 W

at $V_P = 14$ V; $R_L = 2$ Ω } with bootstrap ¹⁾²⁾

P_O typ. 6.0 W

at $V_P = 14$ V; $R_L = 4$ Ω } with bootstrap ¹⁾²⁾

P_O > 5.5 W

typ. 6.0 W

at $V_P = 14$ V; $R_L = 8$ Ω }

P_O typ. 3.3 W

Voltage gain

preamplifier

G_{V1} typ. 24 dB
21 to 27 dB

power amplifier

G_{V2} typ. 30 dB ³⁾
27 to 33 dB

total amplifier

G_{Vtot} typ. 54 dB
51 to 57 dB

Total harmonic distortion at $P_O = 3$ W

d_{tot} typ. 0.3 %

Efficiency at $P_O = 6$ W

η 70 %

Frequency response (-3 dB) at $C_4 = 1$ nF

B 60 Hz to 15 kHz

Input impedance: preamplifier

$|Z_i|$ typ. 30 k Ω ⁴⁾
20 to 40 k Ω

power amplifier

$|Z_i|$ typ. 20 k Ω ⁵⁾
14 to 26 k Ω

Output impedance of preamplifier (pin 7)

$|Z_o|$ typ. 20 k Ω ⁵⁾
14 to 26 k Ω

Output voltage preamplifier (r. m. s. value)

at $d_{tot} < 1\%$ (pin 7)

$V_{O(rms)}$ > 0,7 V

Noise output voltage at $R_S = 0$ Ω } ⁶⁾
at $R_S = 8,2$ k Ω }

$V_{n(rms)}$ typ. 0,3 mV

$V_{n(rms)}$ typ. 0,7 mV
< 1,0 mV

Ripple rejection at $f = 1$ to 10 kHz

RR > 42 dB ⁷⁾

For notes see page 5.

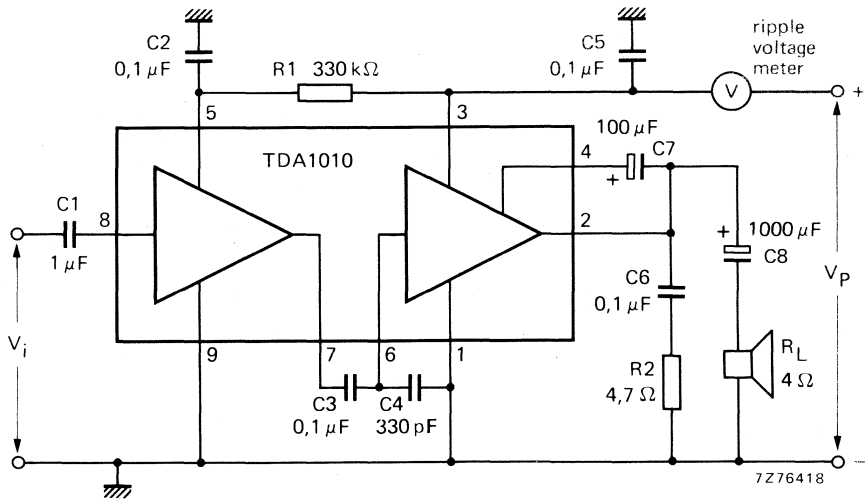
CHARACTERISTICS (continued)

Sensitivity at $P_o = 1\text{ W}$	V_i	typ.	4 mV
Bootstrap current at onset of clipping (r. m. s. value)	$I_4(\text{rms})$	typ.	30 mA

Notes from page 4

- 1) Measured with an ideal coupling capacitor to the speaker load.
- 2) Up to $P_o \leq 3\text{ W}$: $d_{\text{tot}} \leq 1\%$.
- 3) Measured with a load impedance of $20\text{ k}\Omega$.
- 4) Independent of load impedance of preamplifier.
- 5) Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
- 6) Unweighted r. m. s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
- 7) Ripple rejection measured with a source impedance between 0 and $2\text{ k}\Omega$ (maximum ripple amplitude : 2 V).

Test circuit



DEVELOPMENT SAMPLE DATA

SIGNAL-SOURCES SWITCH

The TDA1028 is a quadruple operational amplifier connected as an impedance converter. Each amplifier has 2 switchable inputs which are protected by clamping diodes.

The input currents are independent of the switch position and the outputs are short-circuit protected.

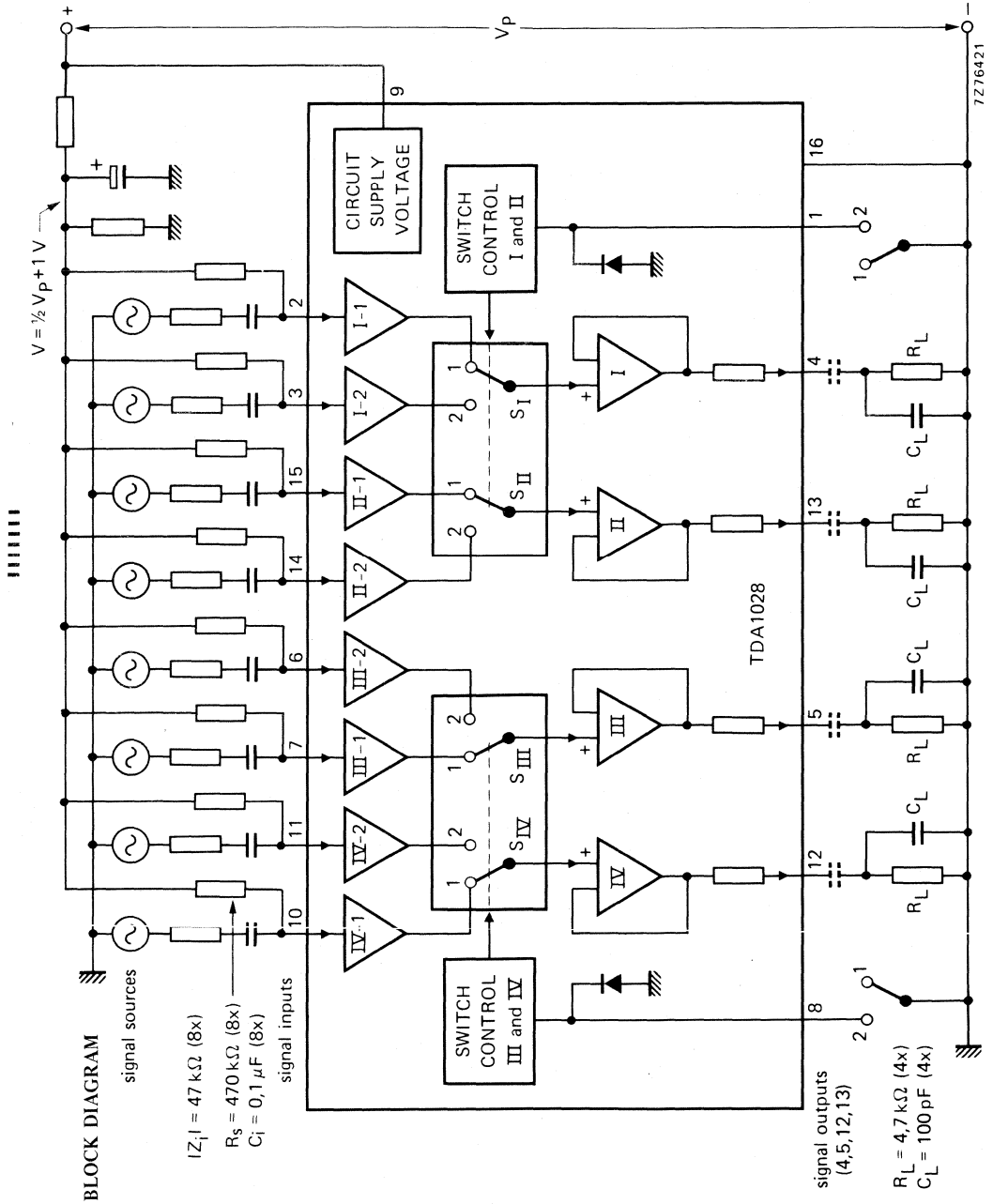
The device is intended as an electronic four-channel signal-sources switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 9)	V_P	6 to 23	V
Operating ambient temperature	T_{amb}	-30 to +80	°C
Supply voltage (pin 9)	V_P	typ. 20	V
Current consumption (pins 4, 5, 12, 13 unloaded)	I_q	typ. 2,5	mA
Signal-input voltage (r. m. s. value)	$V_{i(rms)}$	< 5	V
Voltage gain	G_V	typ. 1	
Distortion	d_{tot}	< 0,1	%
Crosstalk	a	typ. 70	dB
Signal-to-noise ratio	S/N	typ. 100	dB

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (pin 9)	V_P	max.	23	V
Input voltages (pins 2, 3, 6, 7, 10, 11, 14, 15)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pin 1 and 8)	V_S		0 to 23	V

Currents

Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA

Dissipation

Total power dissipation	P_{tot}	max.	800	mW
-------------------------	-----------	------	-----	----

Temperatures

Storage temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$
Operating ambient temperature	T_{amb}	-30 to +80	$^{\circ}\text{C}$

CHARACTERISTICS at $V_P = 20\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified

Current consumption

without load; $I_{4;5;12;13} = 0$

I_9	2,5	mA
-------	-----	----

Supply voltage range

V_P	6 to 23	V
-------	---------	---

Signal inputs

Input offset voltage of

switched-on inputs ($R_i < 1\text{ k}\Omega$)

V_{io}	typ.	2	mV
	<	10	mV

Input offset current of

switched-on inputs

I_{io}	typ.	20	nA
	<	200	nA

Input offset current of

a switched-on input with respect to
a non-switched-on input

I_{io}	typ.	20	nA
	<	200	nA

Input bias current

independent of switch position

I_j	typ.	250	nA
-------	------	-----	----

Capacitance between adjacent inputs

C	typ.	0,5	pF
---	------	-----	----

D.C. input voltage range

V_I	3 to 19	V
-------	---------	---

Supply voltage rejection ratio; $R_i < 10\text{ k}\Omega$

SVRR	typ.	100	$\mu\text{V/V}$
------	------	-----	-----------------

Equivalent input noise voltage

$R_i \leq 1\text{ k}\Omega$; $f = 20\text{ Hz to }20\text{ kHz}$ (r. m. s. value)

$V_{n(\text{rms})}$	typ.	3,5	μV
---------------------	------	-----	---------------

CHARACTERISTICS (continued)

Equivalent input noise current

f = 20 Hz to 20 kHz

 $I_{n(\text{rms})}$ typ. 0,05 nA

Crosstalk between a switched-on input

and a non-switched-on input;

measured at the output at $R_i < 1 \text{ k}\Omega$; f = 1 kHz

a typ. 100 dB

Signal amplifier

Voltage gain of a switched-on input

at $I_{4;5;12;13} = 0$; $R_L = \infty$ G_V typ. 1

Current gain of a switched-on amplifier

 G_i typ. 10^5 **Signal outputs**

Output resistance

 R_o typ. 400 Ω

Output current (pin 4, 5, 12 and 13)

 $\pm I_o > 5 \text{ mA}$

Frequency limit of the output voltage

at $V_i(\text{p-p}) = 1 \text{ V}$; $R_i < 1 \text{ k}\Omega$; $R_L = 10 \text{ M}\Omega$; $C_L = 10 \text{ pF}$

f typ. 1,3 MHz

Slew rate (unity gain) $\Delta V_{4;5;12;13}/\Delta t$ at $R_L = 10 \text{ M}\Omega$; $C_L = 10 \text{ pF}$ S typ. 2 V/ μs **Switch control**

switched-on inputs	interconnected pins	control voltage	
		V_{1-16}	V_{8-16}
I-1, II-1	2-4, 15-13	H	-
I-2, II-2	3-4, 14-13	L	-
III-1, IV-1	7-5, 10-12	-	H
III-2, IV-2	6-5, 11-12	-	L

Control inputs (pins 1 and 8)

Required voltage: HIGH

 $V_{SH} > 3,3 \text{ V}^1)$

LOW

 $V_{SL} < 2,1 \text{ V}$

Input current HIGH (leakage current)

 $I_{SH} < 1 \mu\text{A}$

LOW (control current)

 $-I_{SL}$ typ. 100 μA
< 250 μA ¹⁾ Or control inputs open.

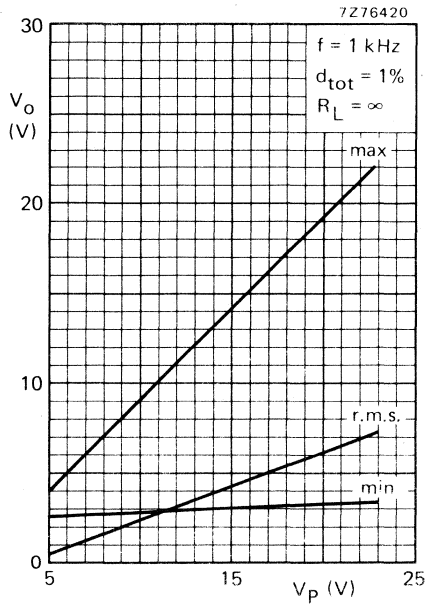
APPLICATION INFORMATION at $V_P = 20$ V; $T_{amb} = 25$ °C; measured in circuit on page 2;
 $|Z_i| = 47$ k Ω ; $C_i = 0,1$ μ F; $R_S = 470$ k Ω ; $R_L = 4,7$ k Ω ;
 $C_L = 100$ pF (unless otherwise specified)

Voltage gain	G_v	typ.	-1,5	dB
D. C. output voltage variation when switching the inputs (pins 4, 5, 12 and 13)	ΔV_O	typ.	10	mV
		<	100	mV
Distortion at $V_i = 5$ V; $f = 1$ kHz	d_{tot}	typ.	0,02	%
		<	0,1	%
at $V_i = 5$ V; $f = 20$ Hz to 20 kHz	d_{tot}	typ.	0,04	%
Noise output voltage (unweighted) $f = 20$ Hz to 20 kHz (r. m. s. value)	$V_{n(rms)}$	typ.	5	μ V
Noise output voltage (weighted) $f = 20$ Hz to 20 kHz (in accordance with DIN45405)	V_n	typ.	12	μ V
Amplitude response (pins 4, 5, 12 and 13) $V_i = 5$ V; $f = 20$ Hz to 20 kHz	ΔV_O	typ.	0,1	dB ¹⁾
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $f = 1$ kHz	a	typ.	75	dB ²⁾
Crosstalk between switched-on inputs and the outputs of the other channels; at $f = 1$ kHz	a	typ.	90	dB ²⁾

1) The lower cut-off frequency depends on values of R_S and C_i .

2) Depends on external circuitry and R_i . The value will be fixed mostly by capacitive crosstalk of the external components.

APPLICATION INFORMATION (continued)



SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs.

The input currents are independent of switch position and the outputs are short-circuit protected.

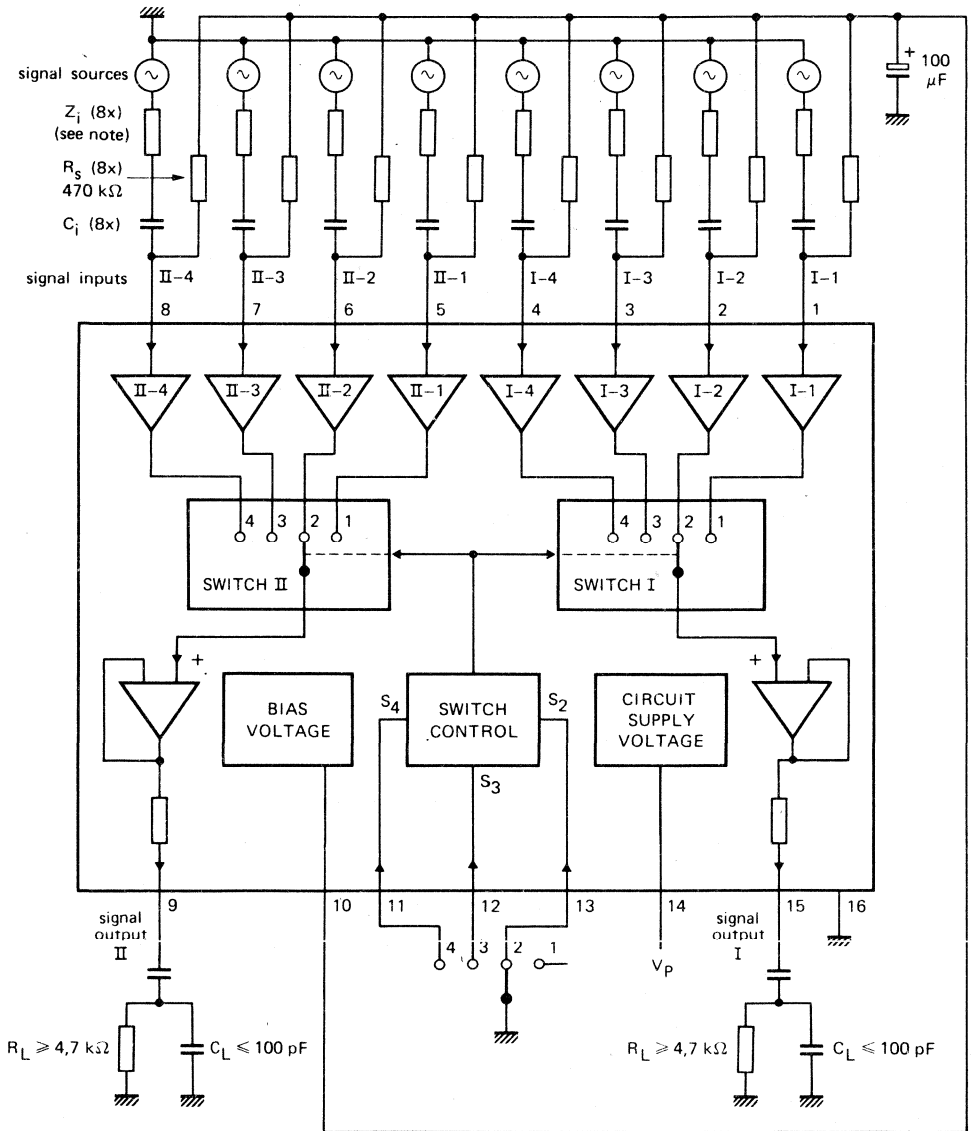
The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers, e.g. as stereo/quadrophony switch.

QUICK REFERENCE DATA			
Supply voltage range (pin 14)	V_P	6 to 23	V
Operating ambient temperature	T_{amb}	-30 to +80	°C
Supply voltage (pin 14)	V_P	typ. 20	V
Current consumption	I_{14}	typ. 4	mA
Signal-input voltage (r. m. s. value)	$V_{i(rms)}$	typ. 6	V
Voltage gain	G_V	typ. 1	
Distortion	d_{tot}	< 0,1	%
Crosstalk	a	typ. 70	dB
Signal-to-noise ratio	S/N	typ. 100	dB

PACKAGE OUTLINE (see general section)

16-lead DIL: plastic.

BLOCK DIAGRAM



7276181

Note: $|Z_i| = 47 \text{ k}\Omega$ in parallel with 200 pF.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V

Currents

Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA

Dissipation

Total power dissipation	P_{tot}	max.	800	mW
-------------------------	-----------	------	-----	----

Temperatures

Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		-30 to +80	°C

CHARACTERISTICS at $V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

Current consumption without load; $I_9 = I_{15} = 0$	I_{14}	typ.	4	mA
Supply voltage range (pin 14)	V_{14-16}		6 to 23	V

Signal inputs

Input offset voltage total of all inputs of both channels $R_i \leq 1$ k Ω	V_{io}	typ. <	2 10	mV mV
Input offset current total of all inputs of both channels	I_{io}	typ. <	20 200	nA nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ. <	20 200	nA nA
Input bias current independent of switch position	I_i	typ.	250	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D. C. input voltage range	V_I		3 to 19	V
A. C. input signal handling (peak-to-peak value)	$V_{i(p-p)}$	<	16	V
Supply voltage rejection ratio; $R_i \leq 10$ k Ω	SVRR	typ.	100	μ V/V

CHARACTERISTICS (continued)

Equivalent input noise voltage

 $R_i = 0$; $f = 20 \text{ Hz to } 20 \text{ kHz}$ (r. m. s. value) $V_{n(\text{rms})}$ typ. 3,5 μV

Equivalent input noise current

 $f = 20 \text{ Hz to } 20 \text{ kHz}$ $I_{n(\text{rms})}$ typ. 0,05 nA
Crosstalk between a switched-on input
and a non-switched-on input;
 measured at the output at $R_i = 1 \text{ k}\Omega$; $f = 1 \text{ kHz}$ a typ. 100 dB
Signal amplifier

Voltage gain of a switched-on input

 at $I_9 = I_{15} = 0$; $R_L = \infty$ G_V typ. 1

Current gain of a switched-on amplifier

 G_i typ. 10^5
Signal outputs

Output resistance (pins 9 and 15)

 R_O typ. 400 Ω
Output current at $V_p = 6$ to 23 V
 $\pm I_9$; $\pm I_{15}$ typ. 5 mA

Frequency limit of the output voltage

 $V_i(\text{p-p}) = 1 \text{ V}$; $R_i = 1 \text{ k}\Omega$; $R_L = 10 \text{ M}\Omega$; $C_L = 10 \text{ pF}$ f typ. 1,3 MHz
Slew rate (unity gain): $\Delta V_{9-16}/\Delta t$; $\Delta V_{15-16}/\Delta t$
 $R_L = 10 \text{ M}\Omega$; $C_L = 10 \text{ pF}$ S typ. 2 $\text{V}/\mu\text{s}$
Bias voltage

D.C. output voltage

 V_{10-16} typ. 11 V ¹⁾
10,2 to 11,8 V

Output impedance

 $|Z_{10-16}|$ typ. 8,2 $\text{k}\Omega$
Switch control

switched-on inputs	interconnected pins	control voltages		
		V_{11-16}	V_{12-16}	V_{13-16}
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leq 1,5 \text{ V}$.

¹⁾ V_{10-16} is typically $V_{14-16}/2 + 0,7 \text{ V}$.

CHARACTERISTICS (continued)**Control inputs** (pins 11, 12 and 13)

Required voltage : HIGH	V_{SH}	>	3,3	V ¹⁾
LOW	V_{SL}	<	2,1	V

Input current

HIGH (leakage current)	I_{SH}	<	1	μA
LOW (control current)	$-I_{SL}$	{	typ. 100	μA
		<	250	μA

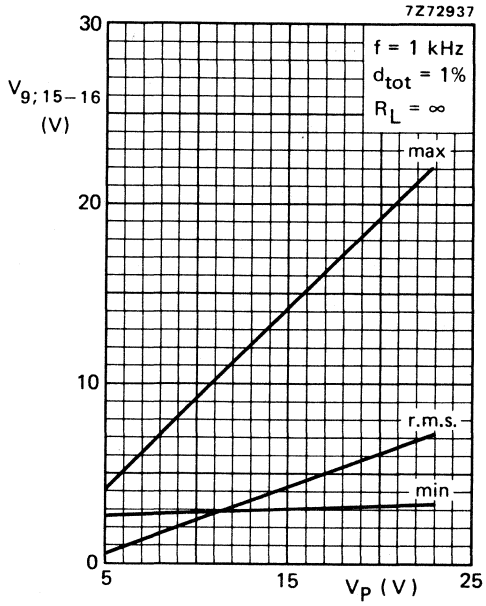
APPLICATION INFORMATION at $V_p = 20$ V; $T_{amb} = 25$ °C; measured in circuit on page 2:
 $|Z_i| = 47$ k Ω // 220 pF; $C_i = 100$ nF; $R_s = 470$ k Ω ; $R_L = 4,7$ k Ω ;
 $C_L = 100$ pF (unless otherwise specified)

Voltage gain	G_v	typ.	-1,5	dB
Output voltage variation when switching the inputs	ΔV_{9-16} ; ΔV_{15-16} }	typ.	10	mV
		<	100	mV
Distortion		{	typ. 0,02	%
$V_i = 5$ V; $f = 1$ kHz	d_{tot}	<	0,1	%
$V_i = 5$ V; $f = 20$ Hz to 20 kHz	d_{tot}	typ.	0,04	%
Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r. m. s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN45405)	V_n	typ.	12	μV
Amplitude response	ΔV_{9-16} ; ΔV_{15-16} }	<	0,1	dB ²⁾
$V_i = 5$ V; $f = 20$ Hz to 20 kHz; $C_i = 0,22$ μF				
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $f = 1$ kHz	a	typ.	75	dB ³⁾
Crosstalk between switched-on inputs and the outputs of the other channels	a	typ.	90	dB ³⁾

1) Or control inputs open.

2) The lower cut-off frequency depends on values of R_s and C_i .

3) Depends on external circuitry and R_i . The value will be fixed mostly by capacitive crosstalk of the external components.



5 W AUDIO POWER AMPLIFIER

in a single in-line encapsulation

The TDA2611 is a monolithic integrated circuit in a 9-lead single in-line plastic package with a high supply voltage audio amplifier.

Special features are:

- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting, and fixed integrated closed loop gain.

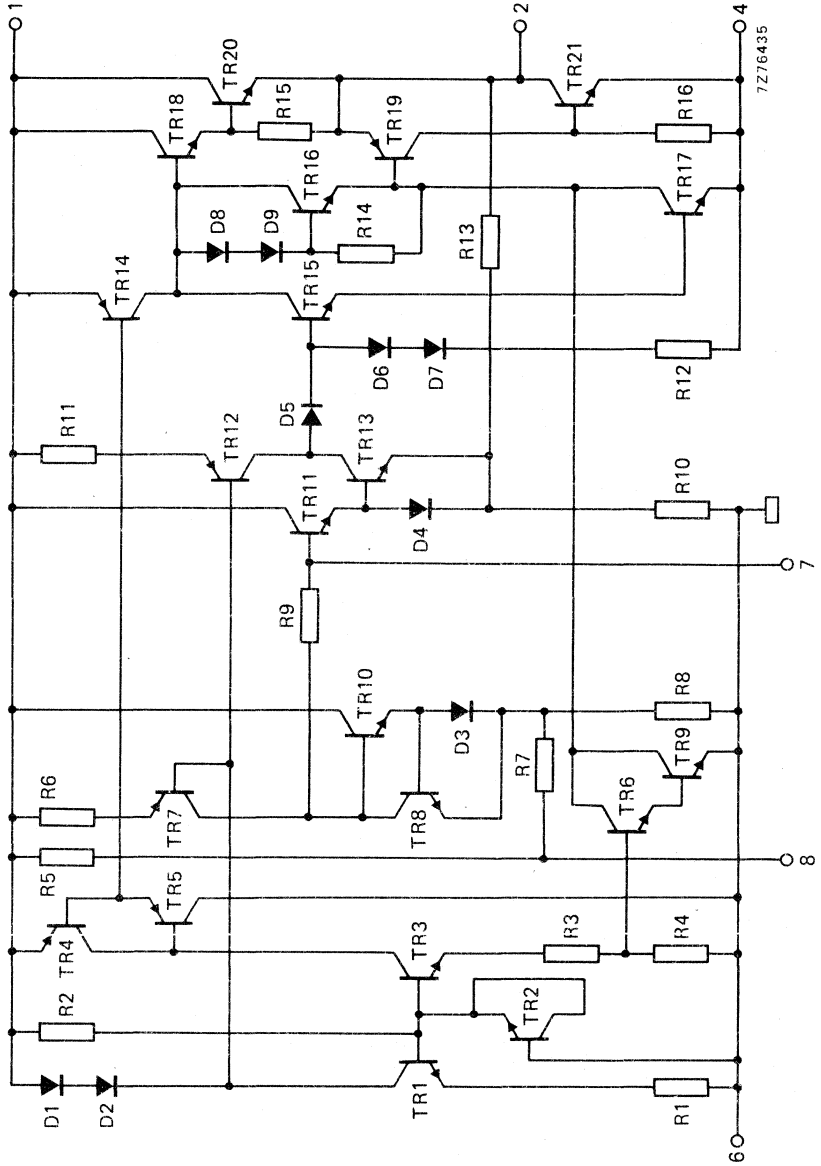
QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 35	V
D.C. output current (peak value)	I_{OM}	< 1, 2	A
Output power at $d_{tot} = 10\%$			
at $V_P = 25\text{ V}; R_L = 15\ \Omega$	P_O	typ. 5	W
at $V_P = 18\text{ V}; R_L = 8\ \Omega$	P_O	typ. 4, 5	W
Total harmonic distortion at $P_O < 2\text{ W}; R_L = 15\ \Omega$	d_{tot}	typ. 0, 3	%
Input impedance	$ Z_i $	typ. 45 30 to 60	k Ω k Ω
Total quiescent current at $V_P = 25\text{ V}$	I_{tot}	typ. 35	mA
Sensitivity for $P_O = 3\text{ W}; R_L = 15\ \Omega$	V_i	typ. 90	mV
Operating ambient temperature	T_{amb}	-25 to +150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-25 to +150	$^{\circ}\text{C}$

PACKAGE OUTLINE (see general section)

9-lead SIL; plastic.

CIRCUIT DIAGRAM (pin 3 not connected; pins 5 and 9 internally connected)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_p max. 35 V

Currents

Non-repetitive peak output current I_{OSM} max. 3 A

Repetitive peak output current I_{ORM} max. 1.5 A

Power dissipation

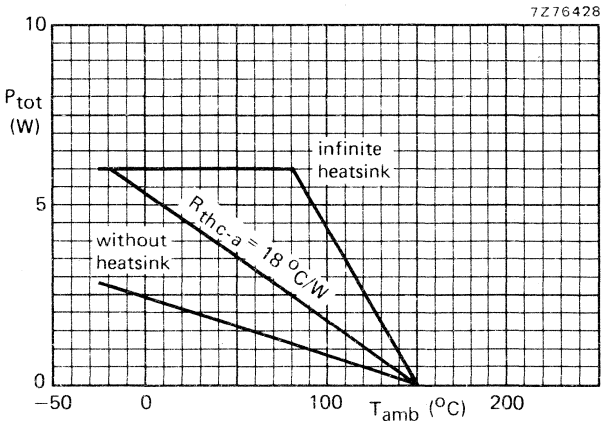
Total power dissipation see derating curve below

Temperatures

Operating ambient temperature T_{amb} -25 to +150 °C

Storage temperature T_{stg} -25 to +150 °C

Total power dissipation



DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

D.C. characteristics

Supply voltage range	V_P	6 to 35	V
Output current (peak value)	I_{OM}	< 1, 2	A
Total quiescent current at $V_P = 25$ V	I_{tot}	typ.	35 mA
		<	60 mA

A.C. characteristics at $T_{amb} = 25$ °C: $V_P = 25$ V; $R_L = 15$ Ω ; $f = 1$ kHz unless otherwise specified; see also test circuit on page 5.

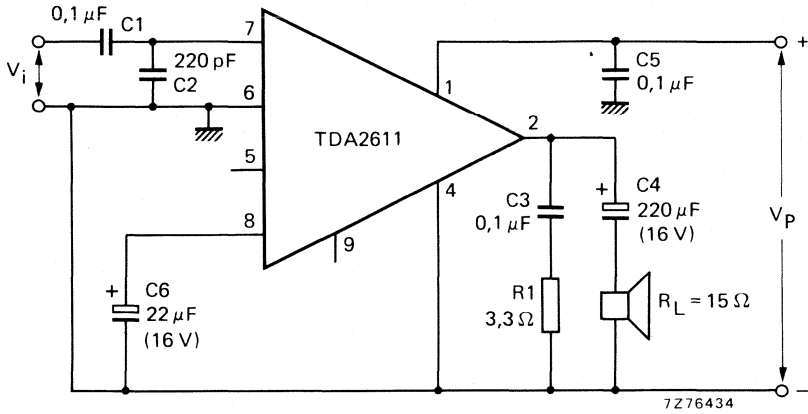
A.F. output power at $d_{tot} = 10\%$

at $V_P = 25$ V; $R_L = 15$ Ω	P_O	typ.	5	W
at $V_P = 12$ V; $R_L = 8$ Ω	P_O	typ.	1, 5	W
at $V_P = 18$ V; $R_L = 8$ Ω	P_O	typ.	4, 5	W
at $V_P = 20$ V; $R_L = 8$ Ω	P_O	typ.	6	W
Total harmonic distortion at $P_O = 2$ W	d_{tot}	typ.	0, 3	%
		<	1	%
Efficiency at $P_O = 5$ W	η		75	%
Frequency response		>	15	kHz
Input impedance	$ Z_i $	typ.	45	k Ω
			30 to 60	k Ω
Noise output voltage at $R_G = 5$ k Ω ¹⁾	V_n	typ.	0, 2	mV
		<	0, 5	mV
Sensitivity for $P_O = 3$ W	V_i	typ.	90	mV
			60 to 120	mV

¹⁾ Measured at a bandwidth of 60 Hz to 15 kHz.

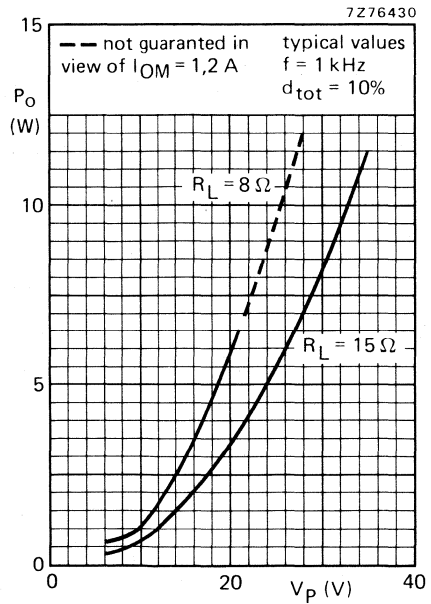
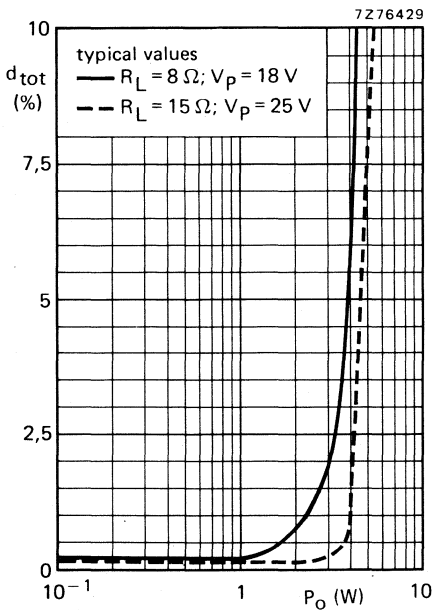
APPLICATION INFORMATION

Test circuit



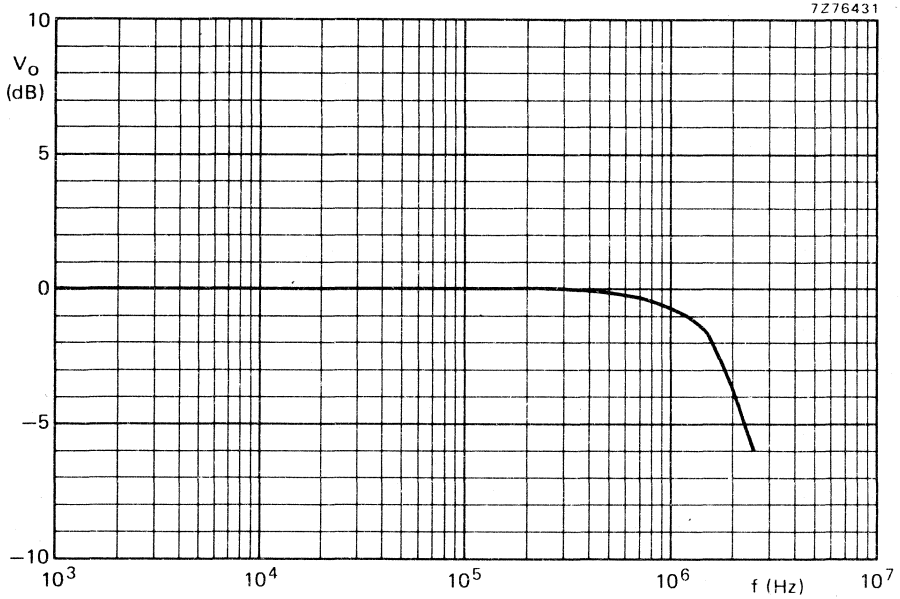
Note : pin 3 not connected
pins 5 and 9 internally connected

DEVELOPMENT SAMPLE DATA

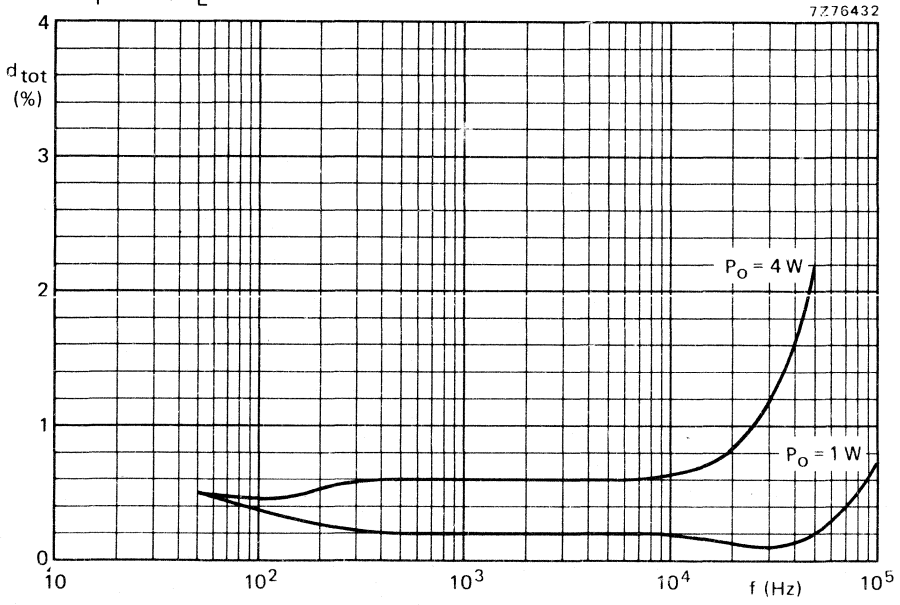


APPLICATION INFORMATION (continued)

$V_p = 25\text{ V}$; $R_L = 15\ \Omega$; $V_i = 6,4\text{ mV}$



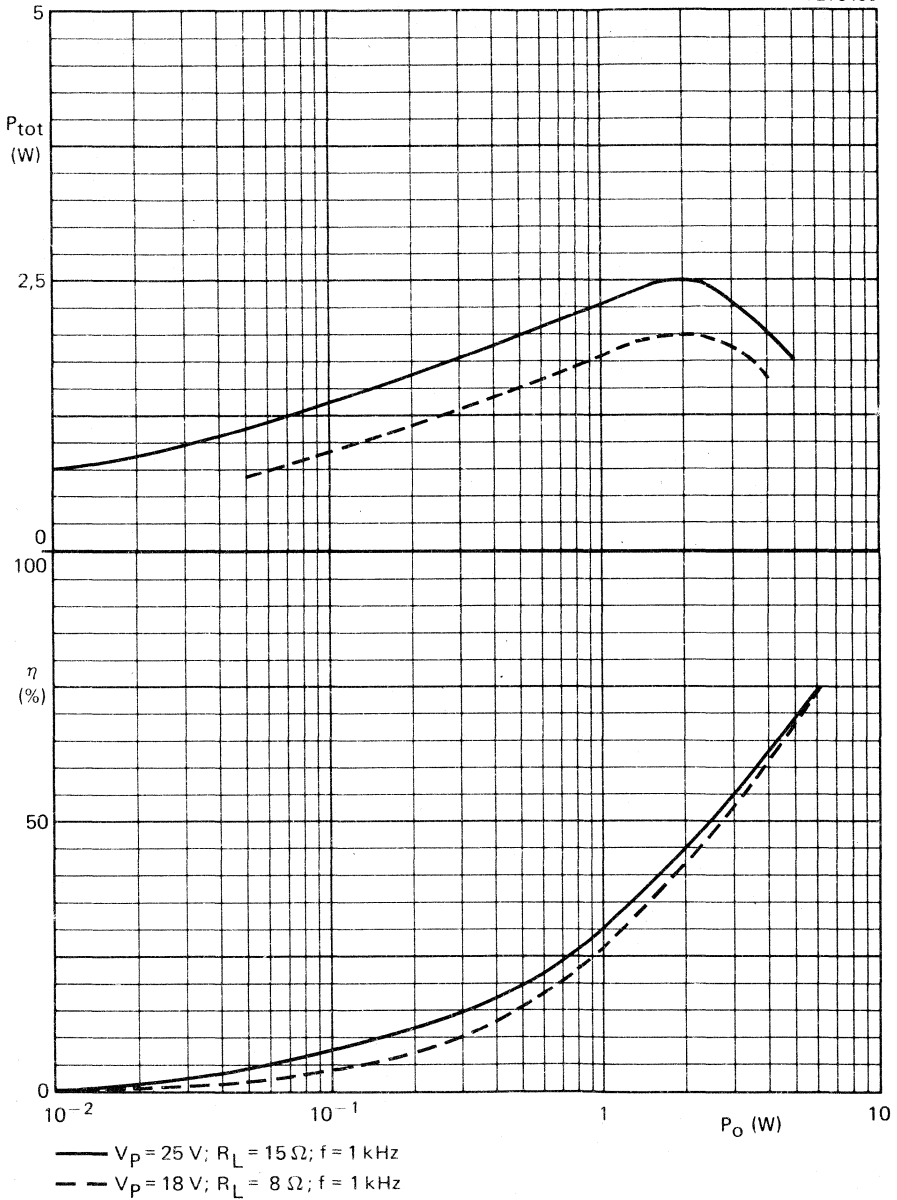
$V_p = 25\text{ V}$; $R_L = 15\ \Omega$



APPLICATION INFORMATION (continued)

7276433

DEVELOPMENT SAMPLE DATA



DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not form part of our data handbook system and does not necessarily imply that the device will go into production

TDA2611A

5 W AUDIO POWER AMPLIFIER in a single in-line encapsulation

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line plastic package with a high supply voltage audio amplifier. Special features are :

- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting, and fixed integrated closed loop gain
- **possibility for increasing the input impedance.**

QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 35	V
D. C. output current (peak value)	I_{OM}	< 1,5	A
Output power at $d_{tot} = 10\%$ at $V_P = 18\text{ V}; R_L = 8\ \Omega$	P_O	typ. 4,5	W
	P_O	typ. 5	W
at $V_P = 25\text{ V}; R_L = 15\ \Omega$			
Total harmonic distortion at $P_O < 2,5\text{ W}; R_L = 8\ \Omega$	d_{tot}	typ. 0,3	%
Input impedance	$ Z_i $	typ. 45	k Ω
		45 k Ω to 1	M Ω
Total quiescent current at $V_P = 18\text{ V}$	I_{tot}	typ. 25	mA
Sensitivity for $P_O = 2,5\text{ W}; R_L = 8\ \Omega$	V_i	typ. 55	mV
Operating ambient temperature	T_{amb}	-25 to +150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$

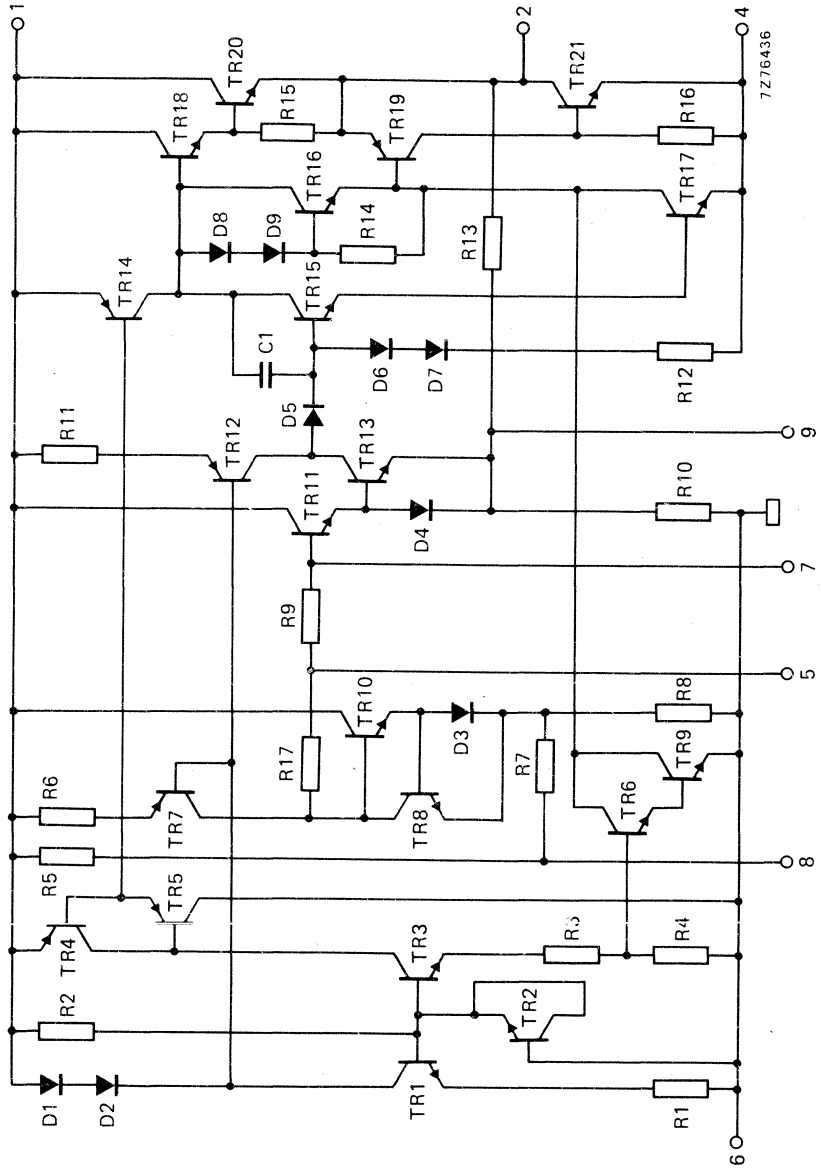
PACKAGE OUTLINE (see general section)

9-lead SIL; plastic.

TDA2611A

|||||

CIRCUIT DIAGRAM (pin 3 not connected)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_P max. 35 V

Currents

Non-repetitive peak output current I_{OSM} max. 3 A

Repetitive peak output current I_{ORM} max. 1.5 A

Power dissipation

Total power dissipation see derating curve below

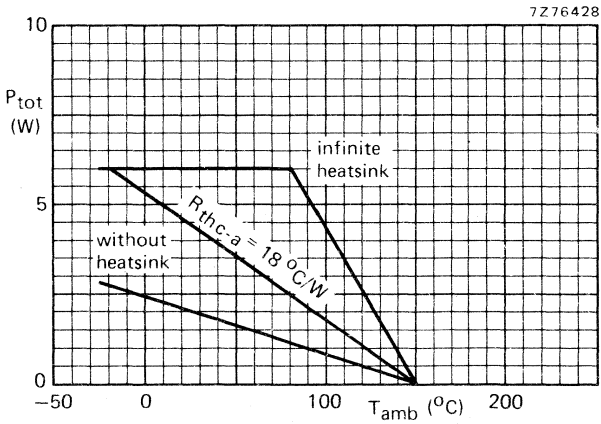
Temperatures

Operating ambient temperature T_{amb} -25 to +150 °C

Storage temperature T_{stg} -55 to +150 °C

Total power dissipation

DEVELOPMENT SAMPLE DATA



CHARACTERISTICS

D.C. characteristics

Supply voltage range	V_P	6 to 35	V
Output current (peak value)	I_{OM}	< 1,5	A
Total quiescent current at $V_P = 18$ V	I_{tot}	typ. 25	mA

A.C. characteristics at $T_{amb} = 25$ °C: $V_P = 18$ V; $R_L = 8$ Ω ; $f = 1$ kHz unless otherwise specified: see also test circuit on page 5.

A.F. output power at $d_{tot} = 10\%$

at $V_P = 18$ V; $R_L = 8$ Ω	P_O	> 4	W
		typ. 4,5	W
at $V_P = 12$ V; $R_L = 8$ Ω	P_O	typ. 1,7	W
at $V_P = 8,3$ V; $R_L = 8$ Ω	P_O	typ. 0,65	W
at $V_P = 20$ V; $R_L = 8$ Ω	P_O	typ. 6	W
at $V_P = 25$ V; $R_L = 15$ Ω	P_O	typ. 5	W

Total harmonic distortion at $P_O = 2,5$ W	d_{tot}	typ. 0,3	%
		< 1	%

Frequency response		> 15	kHz
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Input impedance	$ Z_i $	typ. 45	k Ω
		45 k Ω to 1	M Ω

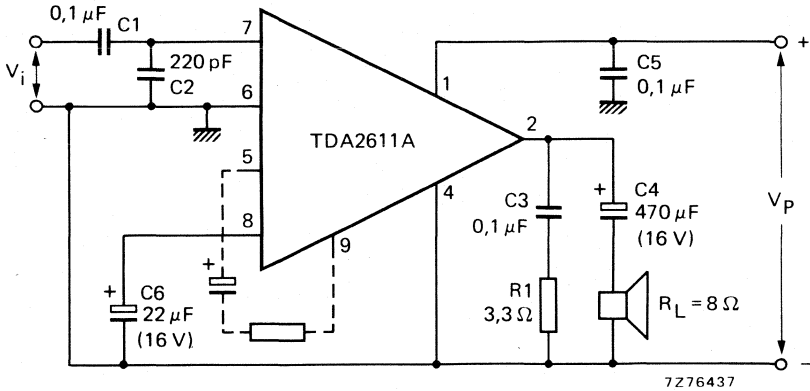
Noise output voltage at $R_S = 5$ k Ω ¹⁾	V_n	typ. 0,2	mV
		< 0,5	mV

Sensitivity for $P_O = 2,5$ W	V_i	typ. 55	mV
		44 to 66	mV

¹⁾ Measured at a bandwidth of 60 Hz to 15 kHz.

APPLICATION INFORMATION

Test circuit

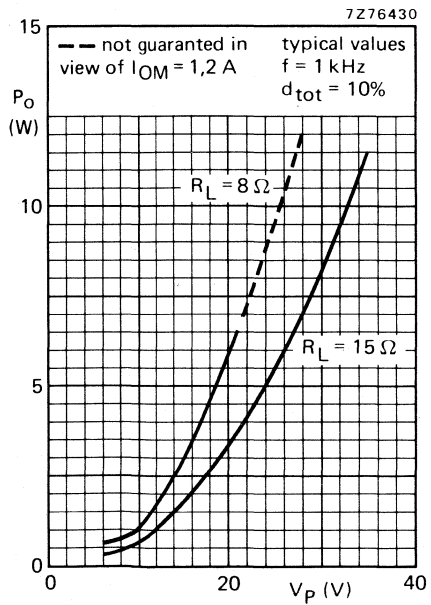
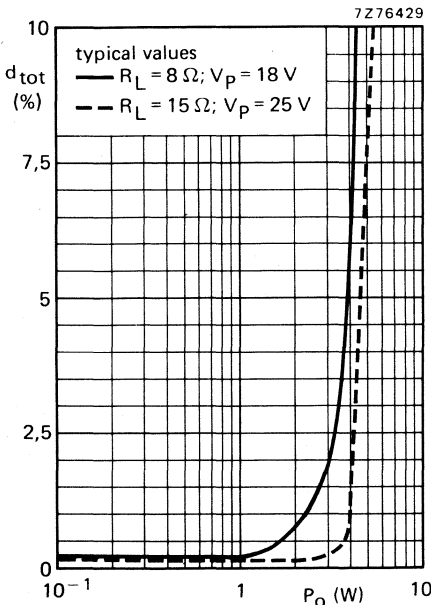


DEVELOPMENT SAMPLE DATA

Z _i	between pins 5 and 9	
	R =	C =
45 kΩ	not connected	
100 kΩ *	410 Ω	47 μF
0,5 MΩ *	47 Ω	47 μF
1 MΩ *	0 Ω	47 μF

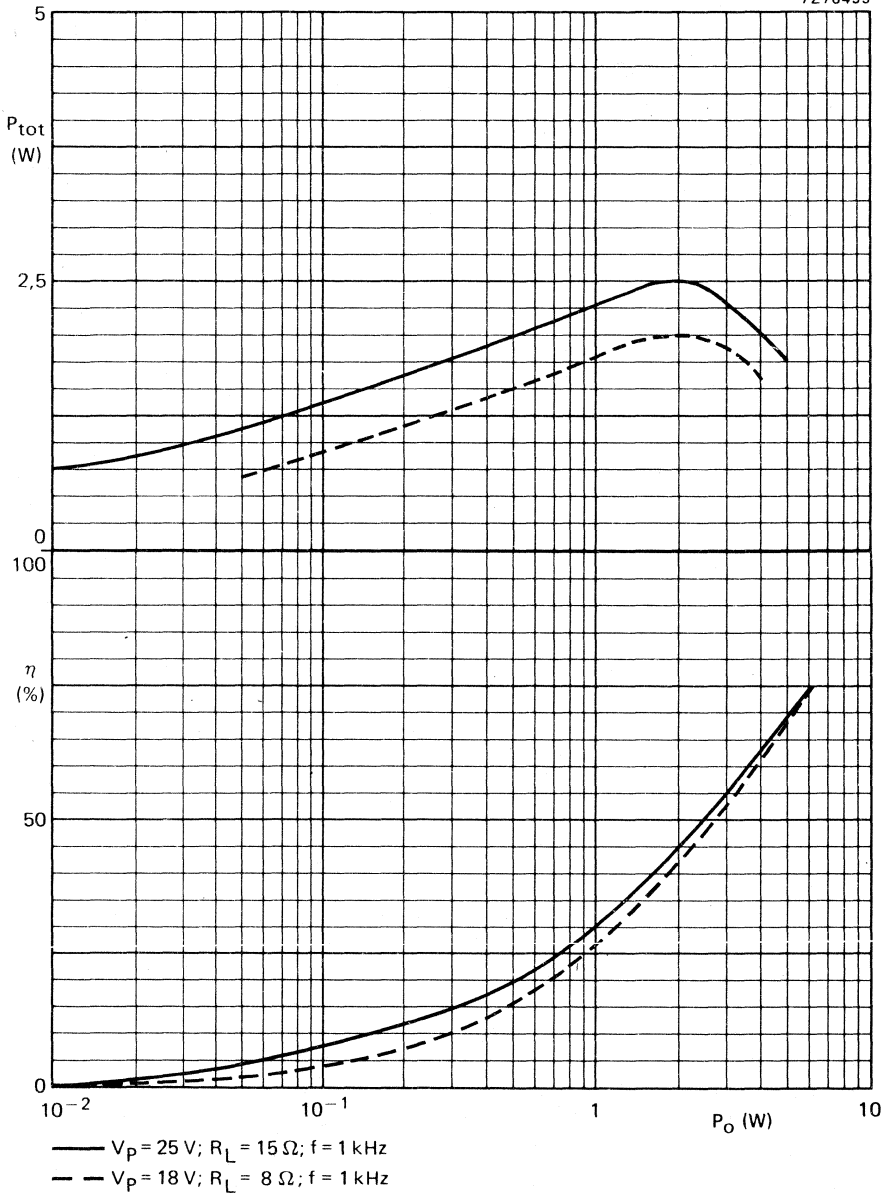
Note : pin 3 not connected

* C2 must be 10 pF.



APPLICATION INFORMATION (continued)

7Z76433



Television



TYPE SELECTION

Vision i.f. demodulators

TCA270S	signal processing circuit
TCA540	synchronous demodulator
TDA2540	i.f. amplifier (n-p-n tuner) and signal processor
TDA2541	as TDA2540, but for p-n-p tuner
TDA2670	i.f. amplifier/demodulator

Signal processors

TBA550, TBA890, TBA900, } TDA2680, TDA2690 }	video preamplifier, automatic horizontal sync and vertical sync separator, etc.
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Sound circuits

TBA750A	limiter-amplifier/demodulator
TDA2610: TDA2610A	output circuit

Sync processors; horizontal, vertical

TBA920: TBA920S	horizontal combination
TBA720A	horizontal oscillator circuit
TDA2571	horizontal oscillator with vertical divider
TDA2581	horizontal deflection stabilizer
TDA2590	horizontal combination

Vertical deflection circuit

TDA2600	switched mode
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Colour decoding

TBA500, TDA2500	luminance combination
TBA560C, TDA2560	luminance and chrominance control combination
TCA660B	contrast, saturation and brightness control for colour difference and luminance signals
TBA510, TDA2510	chrominance combination
TCA640	chrominance amplifier for SECAM or PAL/SECAM decoders
TCA650	chrominance demodulator for SECAM or PAL/SECAM decoders
TBA540	reference combination
TAA630S	synchronous demodulator for colour difference drive
TBA520, TBA990, TCA800	colour demodulator
TDA2520, TDA2522, TDA2523	colour demodulator combination
TBA530, TDA2530	RGB matrix preamplifier

Video recorder circuits

TDA2700	oscillator
TDA2710	chrominance signal/mixer
TDA2720	colour sub-carrier oscillator
TDA2730	f. m. limiter/demodulator

Miscellaneous

TDA2640	switched-mode power supply drive circuit
TAA550	voltage stabilizer (electronic tuning)
TDA2630, TDA2631	touch amplifier, logic and band selection switch
TDA2620	tuning voltage switch and driver for programme indicator

VOLTAGE STABILIZER

The TAA550 is an integrated monolithic voltage stabilizer, especially designed to provide the supply voltage for variable capacitance diodes in television tuners independent of supply voltage and temperature variations.

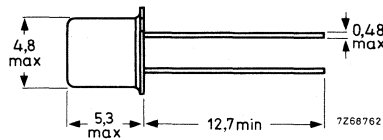
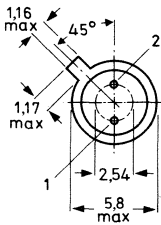
QUICK REFERENCE DATA

Supply current	I_1	typ.	5	mA
Stabilized voltage	V_{12}	32 to 35	V	←
Differential internal resistance	r_{12}	typ.	10	Ω

PACKAGE OUTLINE

Dimensions in mm

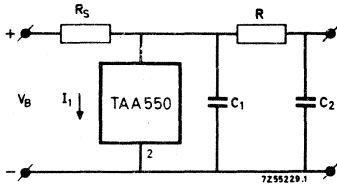
TO-18; 2 pins



pin 1 connected to the case

TAA550

RECOMMENDED CIRCUIT

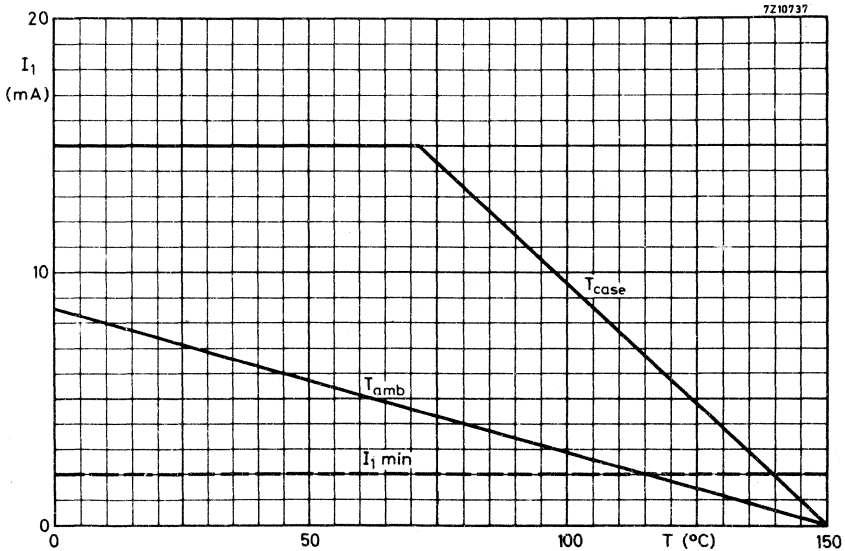


$V_B \gg V_{12}$
 I_1 typ. 5 mA
 $R \geq 22 \Omega$
 $C_1 = 300$ to 4700 pF

C_2 : to be connected if decoupling for low frequency noise is necessary
 In practice values up to $10 \mu\text{F}$ are used.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Maximum allowable supply current versus temperature



Temperatures

Storage temperature	T_{stg}	-55 to +150 °C
Operating ambient temperature	T_{amb}	-20 to +150 °C

CHARACTERISTICS

<u>Recommended supply current</u>	I_1	>	2 mA
		typ.	5 mA

<u>Stabilized voltage</u>	V_{12}		30 to 35 V
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<u>Differential internal resistance at $f = 1$ kHz</u>	r_{12}	typ.	10 Ω
$I_1 = 5$ mA		<	25 Ω

<u>Temperature coefficient at $T_{\text{amb}} = 10$ to 50 °C</u>	$\frac{\Delta V_{12}}{\Delta T_{\text{amb}}}$	typ.	-0,13 mV/°C
			-3,1 to +1,55 mV/°C

SYNCHRONOUS DEMODULATOR FOR COLOUR DIFFERENCE DRIVE

The TAA630 is a synchronous demodulator for direct drive of colour difference output stages with clamping circuits in television sets. The circuit consists of 2 amplifying synchronous demodulators for the B-Y and R-Y signals, a matrix, a PAL switch, a bistable multivibrator and colour killer switch.

QUICK REFERENCE DATA			
Supply voltage	V_{6-16}	nom.	12 V
Ambient temperature	T_{amb}		25 °C

Gain of R-Y demodulator	$G_{V(R-Y)}$	typ.	6
Gain of B-Y demodulator	$G_{V(B-Y)}$	typ.	10,7
Input impedance of B-Y and R-Y channel	$ Z_{9-16} $	typ.	1 kΩ
	$ Z_{13-16} $	typ.	1 kΩ
Output impedance of R-Y, B-Y and G-Y channel	$ Z_{4-16} $	≤	100 Ω
	$ Z_{5-16} $	≤	100 Ω
	$ Z_{7-16} $	≤	100 Ω

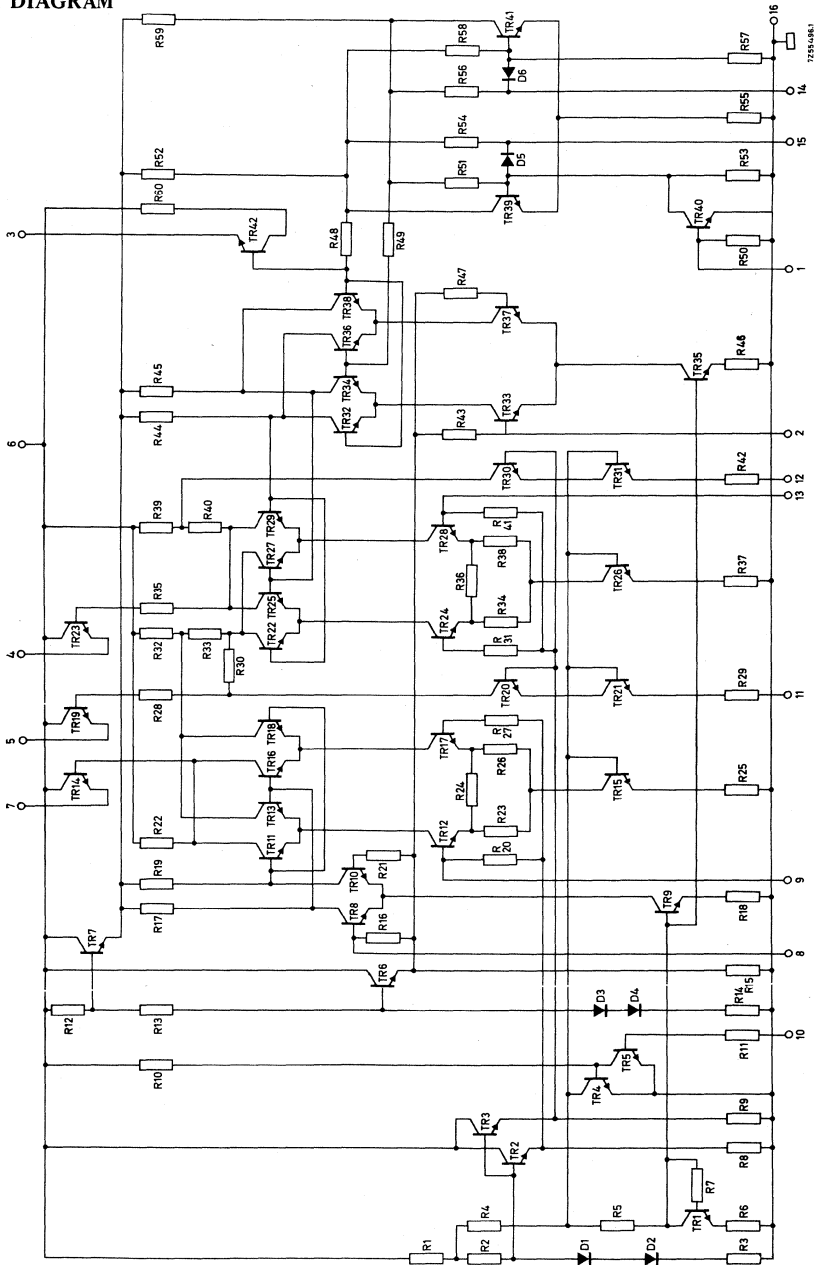
PACKAGE OUTLINES (see general section)

TAA630S: 16-lead DIL; plastic.

TAA630T: 16-lead QIL; plastic.

TAA630S TAA630T

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

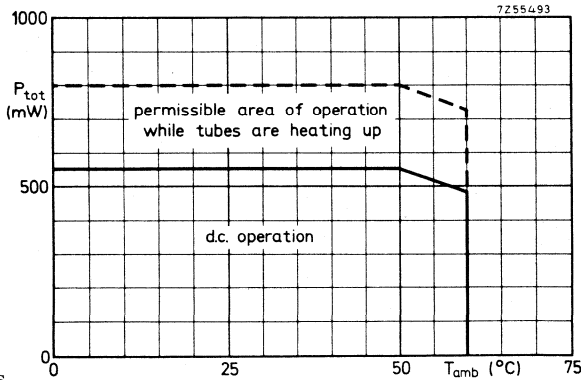
Supply voltage	V_{6-16}	max. 13.2 V
	V_{6-16}	max. 16 V ¹⁾
Pin No. 1 voltage	$-V_{1-16}$	max. 5 V

Currents

Pin No. 4 current	I_4	max. 5 mA
Pin No. 5 current	I_5	max. 5 mA
Pin No. 7 current	I_7	max. 5 mA
Pin No. 1 current	I_1	max. 1 mA

Power dissipation

Total power dissipation	P_{tot}	max. 550 mW
	P_{tot}	max. 800 mW ¹⁾



Temperatures

Storage temperature	T_{stg}	-20 to +125 °C
Operating ambient temperature	T_{amb}	-20 to +60 °C

¹⁾ Permissible while tubes are heating up.

CHARACTERISTICS at $V_{0-16} = 12 \text{ V}$; $V_{10-16} = 0.9 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

Gain of colour difference signals

$V_{i(\text{p-p})} = 50 \text{ mV}$; $f = 4.4 \text{ MHz}$	$G_{V(\text{R-Y})}$	typ.	6 ¹⁾
$G-Y = 0.51 (\text{R-Y}) - 0.19 (\text{B-Y})$	$\frac{G_{V(\text{B-Y})}}{G_{V(\text{R-Y})}}$	typ.	1.78

Input impedance of R-Y and B-Y channels

$V_{i(\text{rms})} = 20 \text{ mV}$ (sine wave); $f = 4.4 \text{ MHz}$

at input $F_{\text{R-Y}}$; input resistance	R_{13-16}	\geq	800 Ω
input capacitance	C_{13-16}	\leq	10 pF
at input $F_{\text{B-Y}}$; input resistance	R_{9-16}	\geq	800 Ω
input capacitance	C_{9-16}	\leq	10 pF

Input impedance of reference inputs

$V_{i(\text{rms})} = 400 \text{ mV}$ (sine wave); $f = 4.4 \text{ MHz}$

at reference R-Y input	$ Z_{2-16} $	660 to 1250 Ω
at reference B-Y input	$ Z_{8-16} $	660 to 1250 Ω

Colour difference output voltages

(peak to peak values) output R-Y	$V_{4-16(\text{p-p})}$	\leq	$3.2 \sqrt{V^2}^3)$
output B-Y	$V_{7-16(\text{p-p})}$	\leq	$4.0 \sqrt{V^2}^3)$
output G-Y	$V_{5-10(\text{p-p})}$	\leq	$1.8 \sqrt{V^2}^3)$

Output impedances of R-Y, B-Y and G-Y channels

at output R-Y	$ Z_{4-16} $	\leq	100 Ω
at output B-Y	$ Z_{7-16} $	\leq	100 Ω
at output G-Y	$ Z_{5-16} $	\leq	100 Ω

1) Ratio of peak to peak values of input and output voltage measured in test circuit on page 6.

$$G_{V(\text{R-Y})} = \frac{V_{4-16}}{V_{13-16}}; G_{V(\text{B-Y})} = \frac{V_{7-16}}{V_{9-16}}$$

2) Linearity of gain ≥ 0.7

3) Measured in the test circuit on page 6.

CHARACTERISTICS (continued)

Colour difference d.c. output voltages

at output B-Y	V ₇₋₁₆	typ. 7.4 V ¹⁾
at output R-Y	adjustable to the same level as V ₇₋₁₆	¹⁾²⁾
at output G-Y	adjustable to the same level as V ₇₋₁₆	¹⁾²⁾

Output voltage; 7.8 kHz (square wave; peak to peak value)

R _{load} = 4.7 kΩ; V ₁₄₋₁₆ = V ₁₅₋₁₆ = 2.5 to 5 V	V _{3-16(p-p)}	typ. 2.5 V
--	------------------------	------------

Input voltages

Reference voltages (peak to peak value)

at reference R-Y	V _{2-16(p-p)}	typ. 1 V ³⁾
at reference B-Y	V _{8-16(p-p)}	typ. 1 V ³⁾

Horizontal deflection pulses (peak value)

at pin No. 14	-V _{14-16M}	2.5 to 5 V
at pin No. 15	-V _{15-16M}	2.5 to 5 V

Identification signal (peak to peak value)

	V _{1-16(p-p)}	2 to 6 V
ident "on"	$\left\{ \begin{array}{l} V_{1-16} \\ I_1 \end{array} \right.$	≅ 0.75 V
		≅ 80 μA
ident "off"	V ₁₋₁₆	≅ 0.4 V

Colour killer voltage and current

colour "on"	V ₁₀₋₁₆	≅ 0.9 V
colour "off"	V ₁₀₋₁₆	≅ 0.3 V

¹⁾ Measured in the test circuit on page 6.

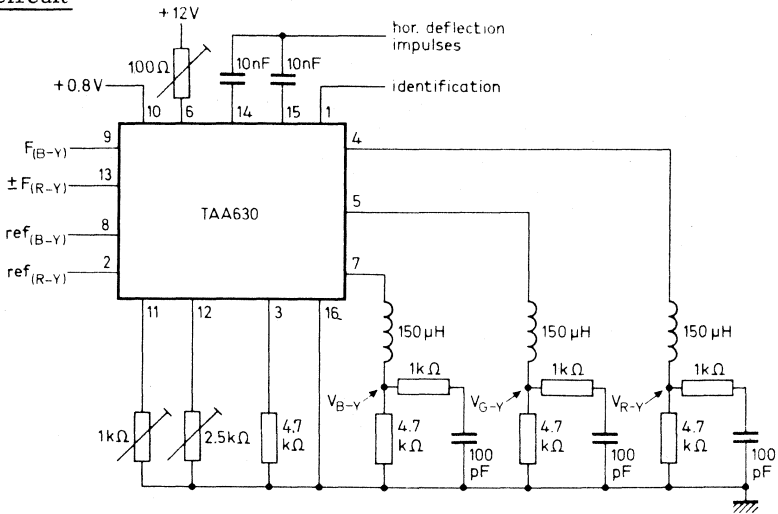
²⁾ To be adjusted with a variable voltage ($V \leq 1.2V$) or with resistors connected between pin 11 and pin 16 for G-Y and between pin 12 and pin 16 for R-Y.

³⁾ Permissible range 0.5 to 2 V.

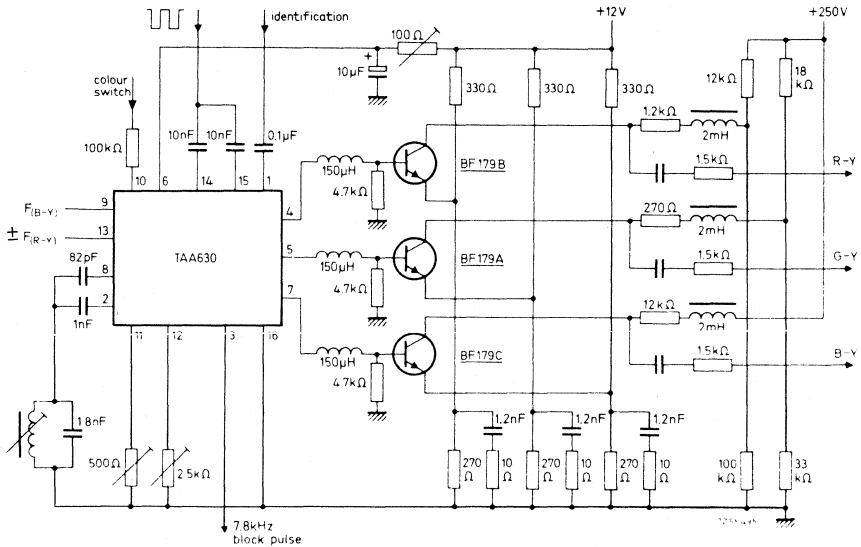
TAA 630S TAA 630T

CHARACTERISTICS (continued)

Test circuit



APPLICATION INFORMATION



CHROMINANCE COMBINATION

The TBA510 is an integrated chrominance amplifier circuit for colour television receivers incorporating a variable gain a.c.c. chroma amplifier circuit, a d.c. control for chroma saturation which can be ganged to the receiver contrast control, chroma blanking and burst gating functions, a burst output stage, a colour killer stage and a PAL delay line driver stage.

QUICK REFERENCE DATA

Supply voltage	V_{1-16}	nom.	12	V
Input signal (colour bars) peak-to-peak value	$V_{4-16(p-p)}$	nom.	150	mV
Output signal (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	1	V
Burst signal output (peak-to-peak value)	$V_{12-16(p-p)}$	typ.	1	V

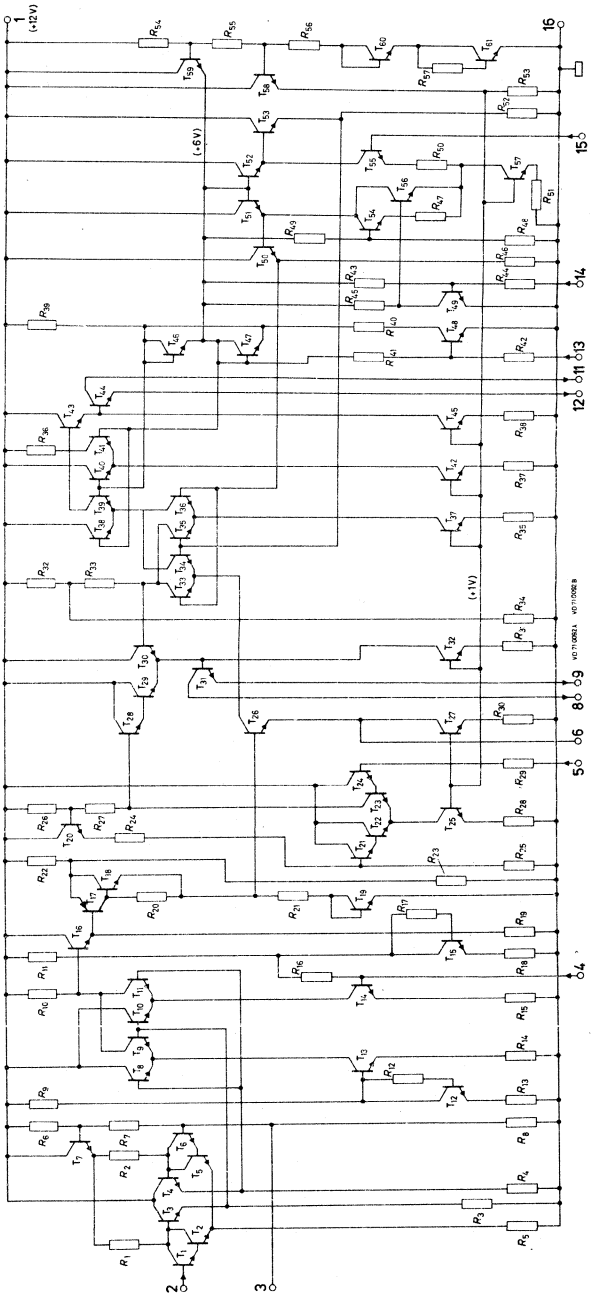
PACKAGE OUTLINES (see general section)

TBA510 : 16-lead DIL; plastic.

TBA510Q: 16-lead QIL; plastic.

TBA510 TBA510Q

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{1-16} max. 13.2 V

Currents

$I_8 ; I_{11}$ max. 20 mA
 $-I_9 ; -I_{12}$ max. 20 mA

Power dissipation

Total power dissipation P_{tot} max. 550 mW

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} -20 to +60 °C

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C ; See also test circuit on page 5.

Input of chrominance signal (fed in via 1 nF)

Input voltage (peak-to-peak value) $V_{4-16(p-p)}$ typ. 150 mV

Input voltage range V_{4-16} 15 to 300 mV

Input impedance

$|Z_{4-16}|$ > 2 kΩ
typ. 3 kΩ

Output of burst signal

D.C. voltage V_{12-16} typ. 8 V

Output signal (peak-to-peak value) $V_{12-16(p-p)}$ typ. 1 V¹⁾

Collector current of output transistor TR44

I_{11} typ. 4 mA

Chrominance signal output (without burst)

D.C. voltage V_{9-16} typ. 7 V

Output signal (colour bars)

at nominal saturation and maximum contrast (peak-to-peak value)

$V_{9-16(p-p)}$ typ. 1 V

Range of contrast and saturation control

+6 to -30 dB

Collector current of output transistor TR31

I_8 typ. 5 mA

Input of a. c. c.

A. C. C. voltage for maximum gain

V_{2-16} typ. 2.5 V

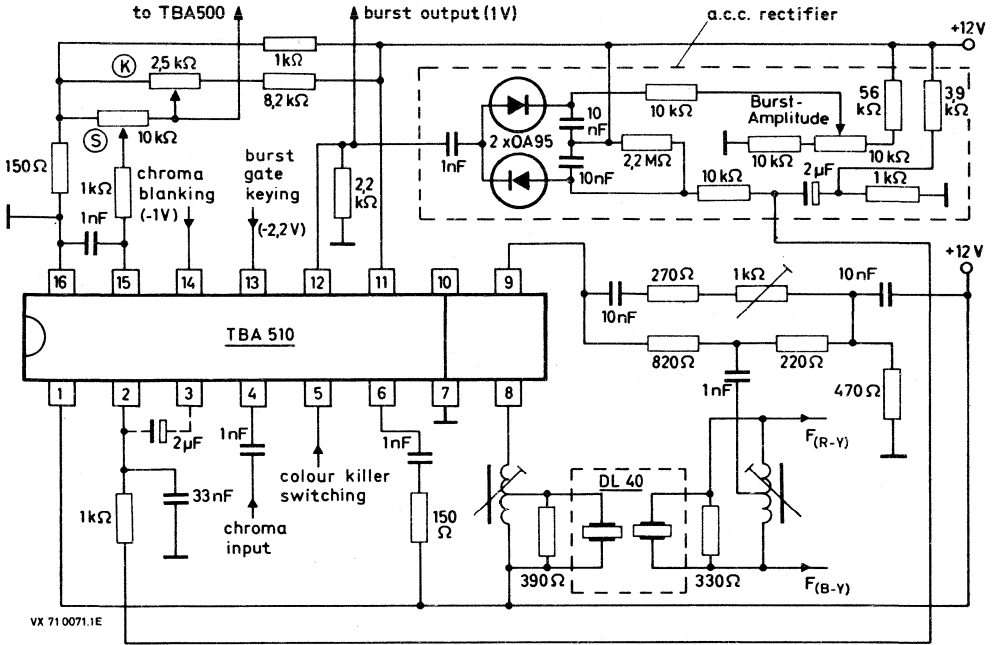
Input impedance

Z_{2-16} > 50 kΩ

1) Kept constant by a. c. c. circuit



APPLICATION INFORMATION



The function is quoted against the corresponding pin number

1. Positive 12V supply

2. A. C. C. control potential input

The potential required at pin 2 for maximum gain is about 2.5 V; gain reduction occurs when this potential is reduced. $Z_{in} > 50 \text{ k}\Omega$

3. A. C. C. bias ripple compensation

The internal A. C. C. circuit consists of a longtailed pair system. The "cold" side is established internally at +2.5 V and is brought out on pin 3. This enables a decoupling capacitor to be connected and returned to the point which secures the lowest supply line ripple amplitude injection into the a. c. c. loop.

4. Chroma signal input

The allowable input voltage range is from 15 mV to 300 mV peak-to-peak with a colour bar signal. The input impedance is greater than 2 k Ω .

APPLICATION INFORMATION (continued)

5. Colour killer switching input
The input impedance is greater than 50 k Ω . Colour "on" 2.5 to 4 V; colour "off" 0 to 1.8 V. The chroma signal suppression when killed is greater than 50 dB.
6. Emitter decoupling network
The series network decouples an emitter of an amplifier stage in the chroma channel. The value of resistance influences the chroma channel gain.
7. Screen
This pin must be connected to pin 10 and taken via a direct path to earth. The function of this is to prevent burst and unwanted chroma appearing at the chroma output of the integrated circuit.
8. Delay line driver (collector)
Supplies the chroma signal drive to the delay line driver transformer, the cold end of which is connected to +12 V. The maximum permitted voltage excursion at this pin is 20 V peak. Maximum current, 12 mA peak.
9. Delay line driver (emitter)
Supplies the chroma to the network which provides the non-delayed signal to the delay line output transformer. The emitter is established internally at a potential of $6.8 \pm 1V$ and the external network, which must incorporate a resistive d.c. path to earth, must not demand more than 20 mA peak current.
10. Screen
Connect to pin 7 and then to earth.
11. Colour burst output (collector)
If a low impedance colour burst is required (from the emitter of the colour burst output, pin 12) pin 11 will be connected to the +12 V supply. The maximum voltage and current excursions permitted on pin 11 are 20 V peak and 20 mA peak.
12. Colour burst output (emitter)
An external load resistor of 2 k Ω is required connected to earth and d.c. potential of $7.7 \pm 1V$ is established on pin 12 due to the internal circuitry. The burst output voltage is 1 V peak-to-peak.
13. Burst gate gating pulse
The horizontal flyback pulse can be used as a source of gating waveform. A negative-going pulse of not greater than 5 V amplitude is necessary, the input impedance is 4 k Ω and the switching level is between -2.2 V and -5 V.
14. Chroma blanking pulse input
A negative going horizontal flyback pulse can be used here. Its amplitude should not exceed -5 V. The input impedance at this pin is 2 k Ω and the switching level is about -1.0 V.
During scan time, the d.c. voltage on this pin should not be negative.

APPLICATION INFORMATION (continued)

15. Chroma saturation control

The d.c. control voltage range required is from 1.5 to 4.5 V (highest gain at 4.5 V).

The input impedance is $> 50 \text{ k}\Omega$ and a control range from +6 to -30 dB is given.

16. Negative supply or earth



COLOUR DEMODULATOR

The TBA520 is an integrated colour demodulator circuit for colour television receivers, incorporating two active synchronous demodulators for R-Y and B-Y chrominance signals, a matrix (producing the G-Y colour difference signal), PAL phase switch and flip-flop. It is suitable for d.c. -coupled drive to the picture tube when associated with the matrix integrated circuit (TBA530) and RGB output stages.

QUICK REFERENCE DATA				
Supply voltage (stabilized)	V ₆₋₁₆	nom.	12	V
Ambient temperature	T _{amb}		25	°C

Gain of R-Y demodulator	G ₁₃₋₄	typ.	7	
Gain of B-Y demodulator	G ₉₋₇	typ.	12,5	
Impedance of chrominance inputs	Z ₉₋₁₆	typ.	1 kΩ	in
	Z ₁₃₋₁₆		parallel	with 10 pF
Impedance of colour-difference signal outputs	Z ₄₋₁₆	typ.	2,7	kΩ
	Z ₇₋₁₆	typ.	2,7	kΩ
	Z ₅₋₁₆	typ.	2,7	kΩ

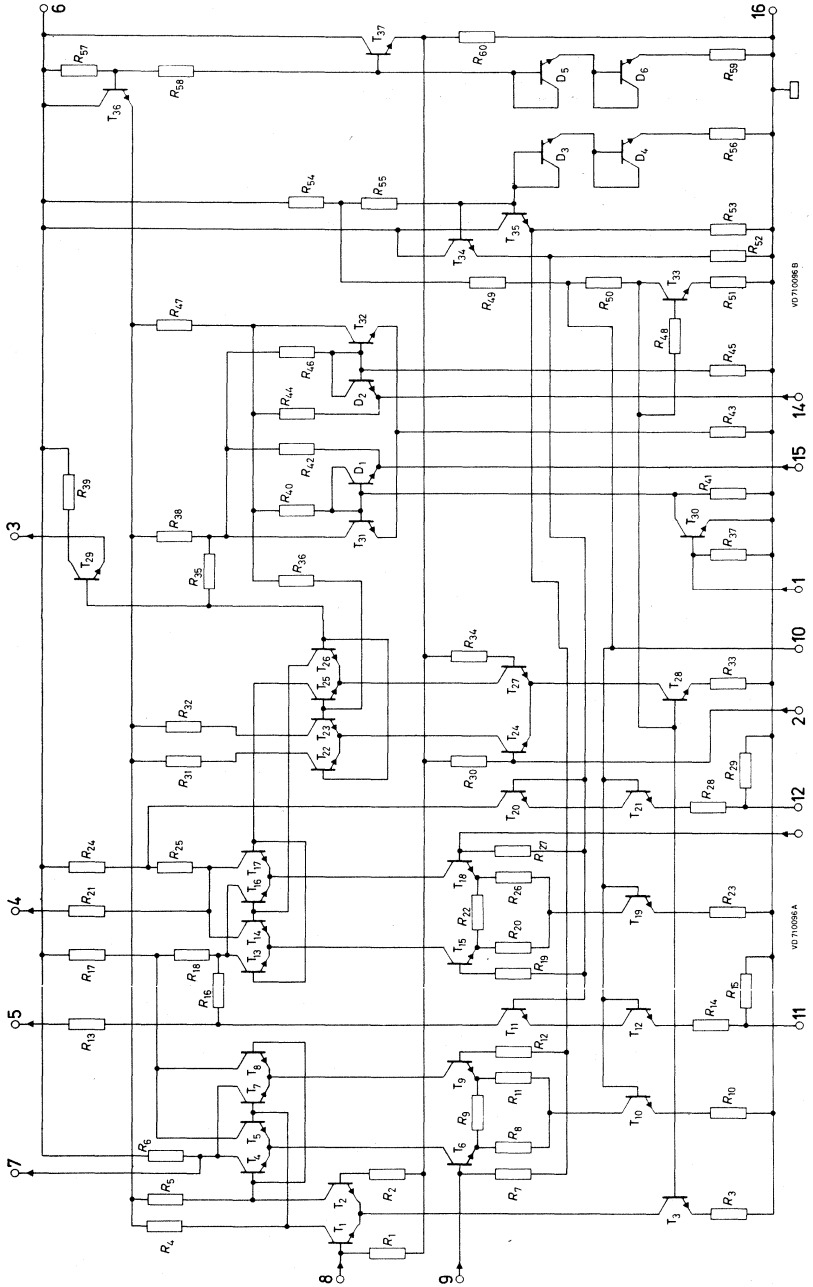
PACKAGE OUTLINES (see general section)

TBA520 16-lead DIL; plastic.

TBA520Q: 16-lead QIL; plastic.

**TBA520
TBA520Q**

CIRCUIT DIAGRAM



WD710096.B

WD710096.A

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Voltages

Supply voltage	V_{6-16}	max.	13.2	V
Ident voltage	$-V_{1-16}$	max.	5	V

Current

Ident current	I_1	max.	1	mA
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Power dissipation

Total power dissipation	P_{tot}	max.	550	mW
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Temperatures

Storage temperature	T_{stg}	-55 to +125	°C
Operating ambient temperature	T_{amb}	-20 to + 60	°C

CHARACTERISTICS at $V_{6-16} = 12$ V (stabilised); $T_{amb} = 25$ °C

Gain of chrominance (R-Y) signal

$V_{i(p-p)} = 50$ mV; $f = 4.4$ MHz	G_{13-4}	typ.	7	1)
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Ratio of gain of blue channel to red channel at identical input signal voltages

$\frac{G_{9-7}}{G_{13-4}}$	typ.	1.78
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Matrix for generation G-Y signal

-0.51 (R-Y) -0.19 (B-Y)

Colour-difference d.c. output voltages

V_{4-16}	typ.	7.9	V
V_{7-16}	typ.	7.9	V
V_{5-16}	typ.	7.9	V

Drift d.c. output voltage

$\Delta T_{amb} = 40$ °C	\leq	50	mV
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Relative change of d.c. output voltages

between channels at $\Delta T_{amb} = 40$ °C	\leq	20	mV
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Colour difference output signals

peak to peak values	R-Y	$V_{4-16(p-p)} \geq$	3.2	$V^2)^3$
	B-Y	$V_{7-16(p-p)} \geq$	4.0	$V^2)^3$
	G-Y	$V_{5-16(p-p)} \geq$	1.8	$V^2)^3$

Impedance of chrominance inputs

$V_{i(rms)} = 20$ mV (sinusoidal); $f = 4.4$ MHz	$\left. \begin{matrix} Z_{9-16} \\ Z_{13-16} \end{matrix} \right\} \geq$	800 Ω in paral- lel with 10 pF
---	--	--

1) Ratio of peak to peak values of input and output signals.

2) Linearity ≥ 0.7 measured in the circuit on page 5.

3) Maximum output signal. For driving the TBA530 the input signal should be reduced by a factor 2.2.



TBA520 TBA520Q

CHARACTERISTICS (continued)

Impedance of colour-difference signal outputs

$ Z_{4-16} $	typ.	2.7	k Ω
$ Z_{7-16} $	typ.	2.7	k Ω
$ Z_{5-16} $	typ.	2.7	k Ω

Impedance of reference signal inputs

$ Z_{2-16} $	typ.	1	k Ω
$ Z_{8-16} $	typ.	1	k Ω

Square wave output voltage

peak to peak value; $f = 7.8$ kHz

$V_{3-16(p-p)}$	>	3	V
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Input current

Supply current consumption

I_6	typ.	32	mA
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Input voltages

Reference voltages (peak to peak values)

at reference R-Y
at reference B-Y

$V_{2-16(p-p)}$	typ.	1	V
$V_{8-16(p-p)}$	typ.	1	V

Identification circuit active

in-active

{ I_1	\geq	80	μ A
	$>$	0.75	V
	\leq	0.4	V

Flip-flop drive pulses (15625 Hz; negative)

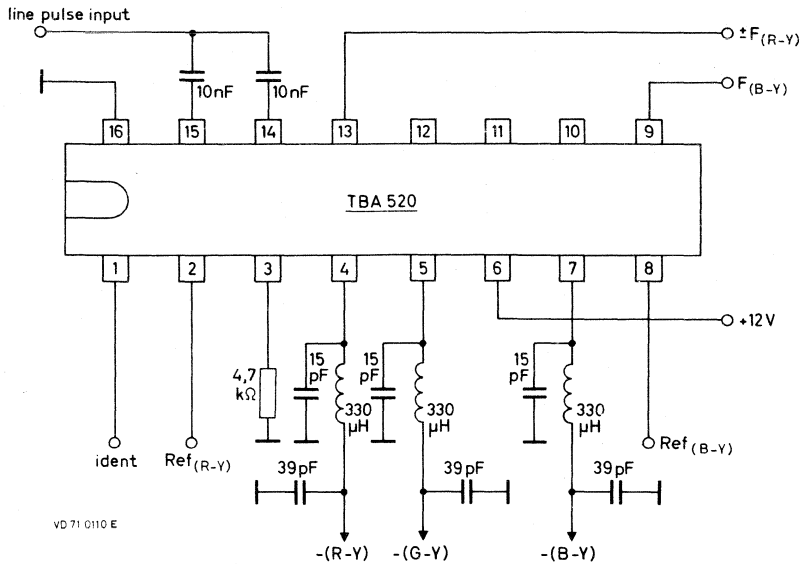
peak to peak values

$V_{14-16(p-p)}$	3 to 4.5	V
$V_{15-16(p-p)}$	3 to 4.5	V

PINNING

- | | |
|--|--|
| 1. Identification bias | 9. B-Y chrominance input signal |
| 2. R-Y subcarrier reference input | 10. n.c. |
| 3. P.A.L. square wave output (7.8 kHz) | 11. G-Y d.c. level setting |
| 4. R-Y signal output | 12. R-Y d.c. level setting |
| 5. G-Y signal output | 13. R-Y chrominance input signal |
| 6. Supply voltage (12 V) | 14. Line pulse input (flip-flop synchronising) |
| 7. B-Y signal output | 15. Line pulse input (flip-flop synchronising) |
| 8. B-Y subcarrier reference input | 16. Earth (negative supply) |

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number (see also page 5).

1. Identification bias

The input current required to stop the flip-flop, "Ident on": $I_{on} \geq 80 \mu A$.
For "Ident off": $V_{off} = -5$ to $+0.4 V$.

2. R-Y subcarrier reference input

An 1 V peak to peak signal is required via a d. c. blocking capacitor. Under no circumstances should this signal be less than 0.5 V peak to peak.
The input resistance at this pin lies between 670Ω and 1250Ω .
($Y_{2-16} = 0.8$ to $1.5 m\Omega^{-1}$)

3. P. A. L. square wave output

The amplitude is $\geq 3 V$ peak to peak from an emitter follower.

4. R-Y signal output (G-Y at pin 5 and B-Y at pin 7)

No external d. c. load needed except that direct connection must be made via the low pass filter to the R. G. B. matrix TBA530.

The signals produced are in the following ratios:

$$\begin{aligned} &V_{B-Y} = 1.3 V_{R-Y} \pm 10\% \\ (a) &V_{G-Y} = 0.76 V_{R-Y} \pm 10\% \\ (b) &V_{G-Y} = 0.26 V_{R-Y} \pm 15\% \end{aligned}$$

Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix.

Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

The d. c. levels should each be adjusted, starting with the (B-Y), to $+7.5 V$ at nominal supply voltage.

The maximum peak to peak voltages for the condition $m \geq 0.7$ ($m =$ ratio of minimum to maximum differential gains) are:

$$\begin{aligned} V_{R-Y(p-p)} &\geq 3.2 V \\ V_{G-Y(p-p)} &\geq 1.8 V \\ V_{B-Y(p-p)} &\geq 4.0 V \end{aligned}$$

The output impedance for each signal is $2.7 k\Omega$.

The drifts in d. c. levels of the colour difference output signals for a change in ambient temperature of $40^\circ C$ (after equilibrium is reached from switch-on) are typically:

Absolute shift	-50 to +50 mV
V_{R-Y} relative to V_{B-Y}	-20 to +20 mV
V_{G-Y} relative to V_{B-Y}	-20 to +20 mV
V_{R-Y} relative to V_{G-Y}	-20 to +20 mV

APPLICATION INFORMATION (continued)

The changes in d. c. level with supply voltage are approximately linear and track together.

The -3 dB bandwidth of the colour difference signals is 1.5 MHz.

5. G-Y signal output (see pin 4)
6. L.T. positive supply
Also d. c. level setting for B-Y output (pin 7). The maximum allowable voltage on this pin is 13.2 V. The minimum supply voltage to ensure setting the B-Y output d. c. level correctly (+7.5 V) is 11.6 V (in such case RV_1 would be set to zero).
7. B-Y signal output (see pin 4)
8. B-Y subcarrier reference input
The requirements here are identical with those for pin 2.
9. Chrominance B-Y input signal
An input signal up to 360 mV peak to peak (colour bars) is allowed. For driving the TBA530 an input signal of 160 mV is required. The input impedance is greater than 800Ω and the input capacitance is less than 10 pF (y_{9-16} and $y_{13-16} \leq 1.25 \text{ m} \Omega^{-1}$ in parallel with 10 pF). The spread in gain of the internal circuitry in the chrominance channel is $\pm 10 \%$.
10. Internally connected; no external connection should be made.
11. D.C. level setting for G-Y output signal (circuit diagram on page 5).
12. D.C. level setting for R-Y output (see circuit diagram on page 5).
13. Chrominance R-Y input signal
An input signal up to 500 mV peak to peak (colour bars) is allowed. The input impedance and spread in gain is the same as for pin 9.
14. Line pulse input (flip-flop synchronising)
A 4 V peak negative going line flyback pulse should be applied via separate 10 nF capacitors to pins 14 and 15. Pulse amplitude to lie between 3 V and 4.5 V peak to peak.
15. Line pulse input (see pin 14)
16. Negative supply (earth)

RGB MATRIX PREAMPLIFIER

The TBA530 is an integrated circuit for colour television receivers incorporating a matrix preamplifier for RGB cathode or grid drive of the picture tube without clamping circuits. The chip lay-out has been designed to ensure tight thermal coupling between all the transistors in each channel to minimise and equalise thermal drifts between channels. Also, each channel follows an identical lay-out to ensure equal frequency behaviour of the three channels.

This integrated circuit has been designed to be driven from the TBA520 synchronous demodulator integrated circuit.

QUICK REFERENCE DATA			
Supply voltage	V_{8-6}	nom.	12 V
Ambient temperature	T_{amb}		25 °C
Gain of luminance and colour-difference channels	G	typ.	100
Total current consumption	I_{tot}	typ.	30 mA

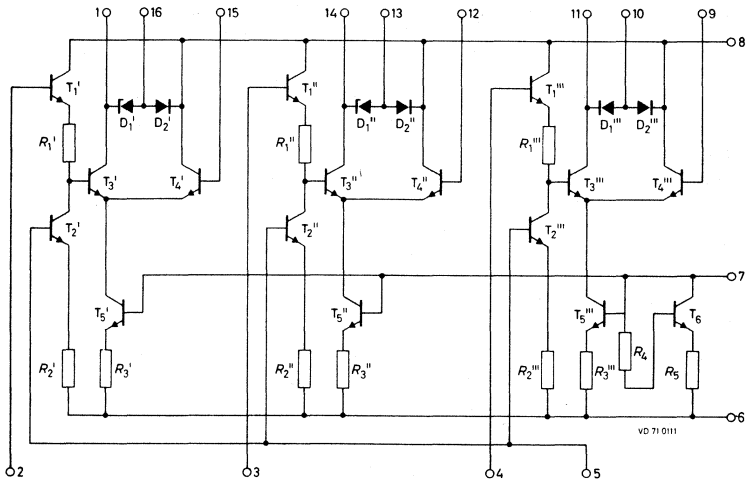
PACKAGE OUTLINES (see general section)

TBA530 : 16-lead DIL; plastic.

TBA530Q: 16-lead QIL; plastic.

TBA530 TBA530Q

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{8-6} max. 13.2 V

Currents

Supply currents $I_1 ; I_{11} ; I_{14}$ max. 10 mA
 $I_{10} ; I_{13} ; I_{16}$ max. 50 mA¹⁾

Power dissipation

Total power dissipation P_{tot} max. 400 mW¹⁾

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} -20 to +60 °C

CHARACTERISTICS measured in circuit on page 5

Measuring conditions: $V_{8-6} = 12 \text{ V}$; $T_{amb} = 25 \text{ °C}$
black level: $V_{R-Y} = V_{G-Y} = V_{B-Y} = 7.5 \text{ V}$
 $V_Y = 1.5 \text{ V}$

Colour difference input

peak-to-peak values $V_{2-6(p-p)}$ typ. 1.4 V
 $V_{3-6(p-p)}$ typ. 0.82 V
 $V_{4-6(p-p)}$ typ. 1.78 V

Luminance input signal (peak-to-peak value) $V_{5-16(p-p)}$ typ. 1 V

Gain of colour channels
(B-Y;G-Y;R-Y) at $f = 0.5 \text{ MHz}$ G_{2-6} } typ. 100 2)
 G_{3-6} }
 G_{4-6} }

Ratio of gain of luminance
amplifier to colour amplifiers typ. 1

D.C. output voltage V_R } typ. 165 V
 V_G }
 V_B }

¹⁾ At increased voltages due to external failures (e.g. collector-basis breakdown in the output transistors) a maximum current of 50 mA is permitted between pins 16 and 8, 13 and 8, 10 and 8, The maximum allowable dissipation in this case is 500 mW.

²⁾ G is defined as the voltage ratio between the input signals at the pins 2, 3, 4 and the output signals at the collectors of the output transistors.

CHARACTERISTICS (continued)

Input resistance of colour
difference amplifiers at $f = 1 \text{ kHz}$

R2-6	}	typ.	60	$\text{k}\Omega$
R3-6				
R4-6				

Input capacitance of colour
difference amplifiers at $f = 1 \text{ MHz}$

C2-6	}	typ.	3	pF
C3-6				
C4-6				

Input resistance of luminance
amplifier at $f = 1 \text{ kHz}$

R5-6	typ.	20	$\text{k}\Omega$
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Input capacitance of luminance
amplifier at $f = 1 \text{ MHz}$

C5-6	typ.	10	pF
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Bandwidth of all channels (3 dB)

B	typ.	6	MHz
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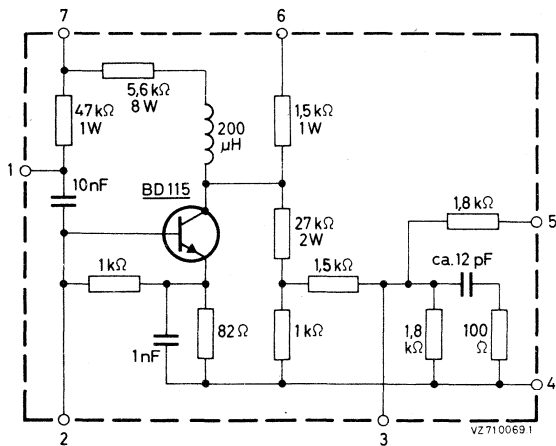
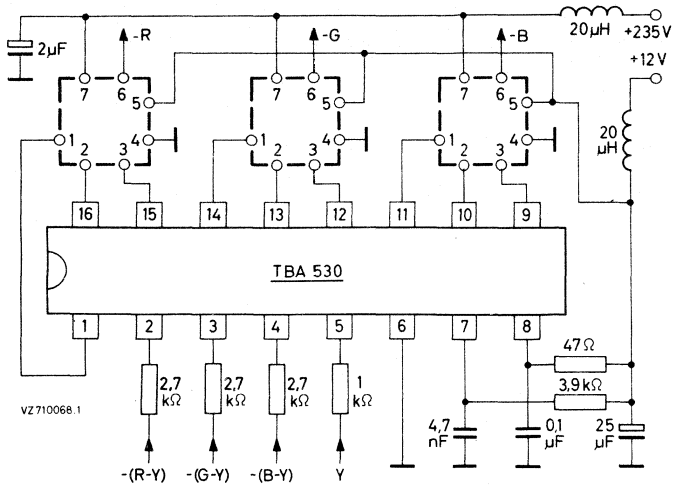
Total current drain

I_{tot}	typ.	30	mA
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PINNING see also APPLICATION INFORMATION circuit diagram on page 5.

- | | |
|--------------------------------------|---|
| 1. Output load resistor (red signal) | 9. Bluechannel feedback |
| 2. R-Y input signal | 10. Blue signal output |
| 3. G-Y input signal | 11. Output load resistor (blue signal) |
| 4. B-Y input signal | 12. Green channel feedback |
| 5. Luminance signal input | 13. Green signal output |
| 6. Earth (negative supply) | 14. Output load resistor (green signal) |
| 7. Current feed point | 15. Red channel feedback |
| 8. 12 V positive supply | 16. Red signal output |

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin numbering (see also page 5)

1. Output load resistor, red signal (pin 11: blue signal, pin 14: green signal)
Resistors (47 k Ω , 1 W) connected to +200 V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by an internal zener type junction and the d.c. feedback and is approximately +8 V. The maximum current which can be allowed at each of these pins is 10 mA.
2. R-Y input signal
This signal is fed via a low-pass filter from the TBA520 demodulator i.c. (pin 7) having a d.c. level of +7.5 V and an amplitude of 1.40 V peak to peak. The input resistance for this pin is typically 60 k Ω with an input capacitance of less than 3 pF (similarly for pins 3 and 4).
3. G-Y input signal
The d.c. black level of this signal is +7.5 V and its amplitude is 0.82 V peak to peak (see pin 2).
4. B-Y input signal
The d.c. black level of this signal is +7.5 V and its amplitude is 1.78 V peak to peak (see pin 2)
5. Luminance signal input
The d.c. level on this pin for picture black is +1.5 V. The required signal amplitude is 1 V black-to-white with negative-going sync (or blanking) for cathode drive as shown. The input resistance at this pin is 20 k Ω approximately with a capacitance of typ. 10 pF.
6. Negative supply (earth)
7. Current feed point
A current of approximately 2.5 mA is required at this pin, fed via a 3.9 k Ω resistor from +12 V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7 nF is necessary.
8. Positive 12 V supply
Maximum supply voltage permitted, 13.2 V. Current consumption approximately 30 mA.
9. Blue channel feedback (green channel, pin 12: red channel, pin 15)
The d.c. working points and gains of both the output stages and the i.c. amplifier stages are stabilised by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by setting correctly the d.c. level of the colour difference signals produced by the TBA520 demodulator i.c. The gains of the R-G-B output stages are adjusted to give the correct white points setting on the picture tube by adjusting the potentiometers in the feedback paths (VR1, VR2). (See notes on setting up decoder).

APPLICATION INFORMATION (continued)

10. Blue signal output (green and red signal outputs on 13 and 16)
These pins are internally connected with pins 11, 14 and 1 respectively via zener type junctions to give a d.c. level shift appropriate for driving the output transistor bases directly. To by-pass the zener junctions at h.f. three 10 nF capacitors are required.
11. Output load resistor, blue channel (pin 1).
12. Green channel feedback (see pin 9).
13. Green signal output (see pin 10).
14. Output load resistor, green channel (see pin 1).
15. Red channel feedback (see pin 9).
16. Red signal output (see pin 10).

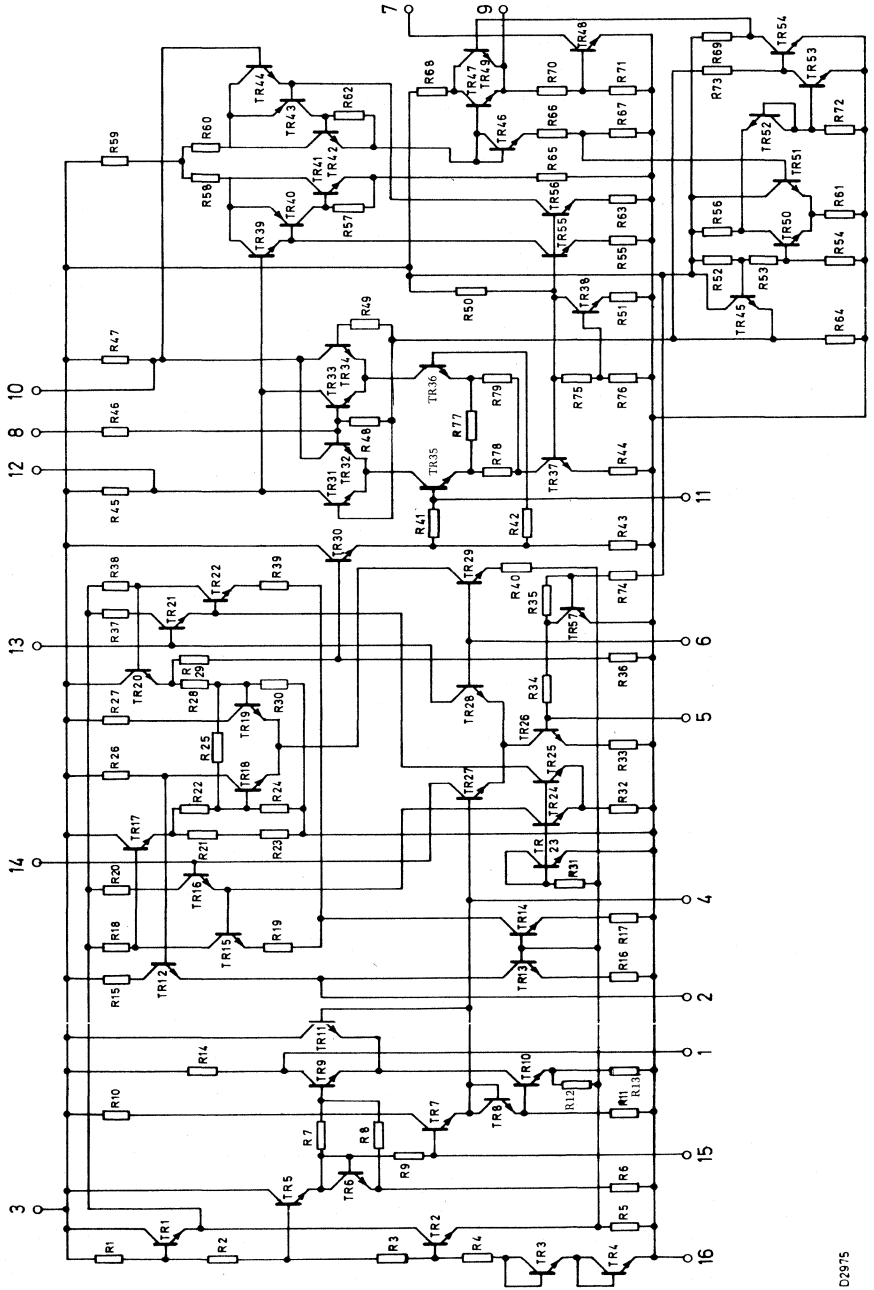
BRIEF PERFORMANCE DETAILS AND COMMENTS

1. Spread of the ratio of voltage gains for colour difference and luminance signal inputs 0.9 to 1.1.
2. Very careful attention to earth paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon h.f. response of inevitable differences, e.g., the absence of a potentiometer in one of the stages, the compensating capacitors C₁, C₂ and C₃ may be appropriately selected for any given board layout.
3. The signal black level at the collectors of the R-G-B output stages depends upon the +12V supply, the d.c. level of the colour difference signals from the TBA520 demodulator i.c. and the black level potential of the luminance signal applied to the TBA530 matrix i.c. The d.c. levels of the signals produced and handled by the i.c.'s are designed to have approximately proportional tracking with the 12V supply potential,

$$\text{i.e., } \frac{\Delta V(\text{d.c. level, signal})}{\Delta V_{12V}} \approx \frac{V_{\text{nom}}(\text{d.c. level, signal})}{12}$$

To ensure that changes in picture black level due to variations on the 12V supply to the i.c.'s occur in a predictable way, all the i.c.'s should be operated from a common supply line. This is specially important for the TBA520 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12V supply should have a stability of not worse than $\pm 3\%$ due to operational variations, and preferably be tracked with the screen-grid supply of the picture tube.

CIRCUIT DIAGRAM



D2975

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V₃₋₁₆ max. 13.2 V

Power dissipation

Total power dissipation at T_{amb} = 50 °C P_{tot} max. 680 mW

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} -20 to +60 °C

CHARACTERISTICS at V₃₋₁₆ = 12 V; T_{amb} = 25 °C; V_{5-16 M} = 0.7 V
(burst signal input); V_{8-16(p-p)} = 2.5 V (P. A. L. square wave in-
put) Measured in circuit shown on page 4.

Output signals

R-Y reference signal output
peak-to-peak value V_{4-16(p-p)} typ. 1.5 V

Colour killer output: colour on V₇₋₁₆ typ. 12 V
colour off V₇₋₁₆ < 250 mV

A.C.C. output signal range

at correct phase of P. A. L. switch V₉₋₁₆ +4 to +0.2 V
at incorrect phase of P. A. L. switch V₉₋₁₆ +4 to +11 V

Oscillator section (amplifier)

Input resistance R₁₅₋₁₆ typ. 3.5 kΩ

Input capacitance C₁₅₋₁₆ typ. 5 pF

Voltage gain G₁₅₋₁ typ. 4.7

Reactance control section

Voltage gain with pins 13 and 14 interconnected G₁₅₋₂ typ. 1.3

Rate of change of gain G₁₅₋₂ with phase difference
between burst and reference signal $\frac{\Delta G_{15-2}}{\Delta \varphi_{5-4}}$ typ. 5 $\frac{1}{\text{rad}}$

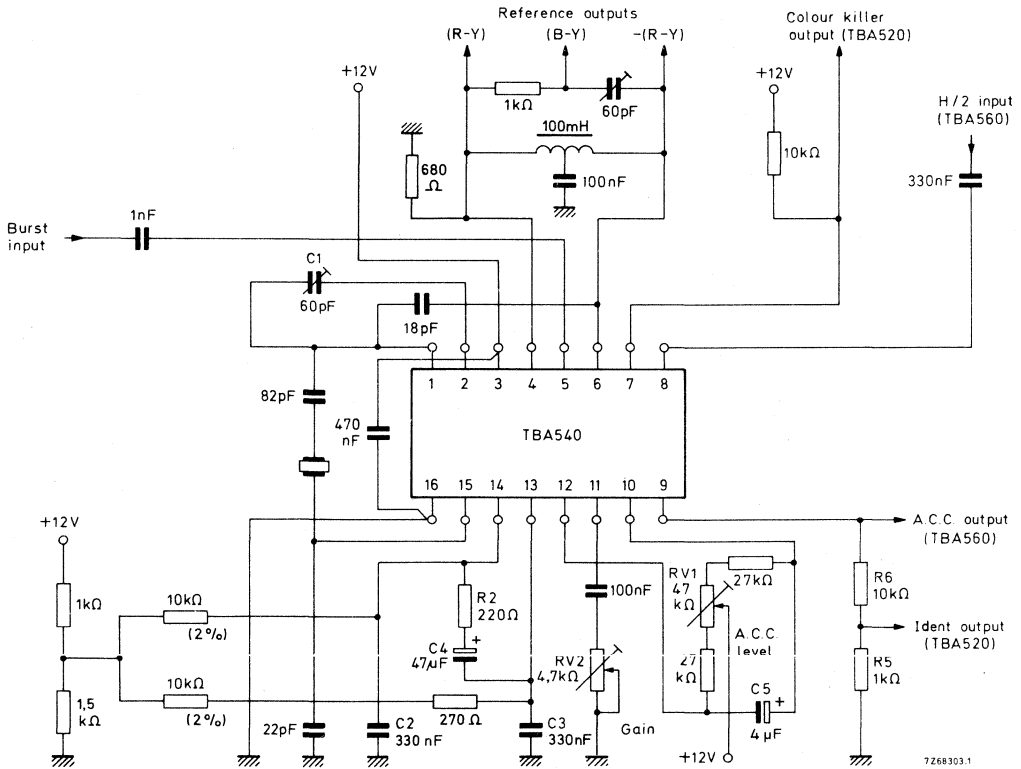
Supply current consumption I₃ typ. 33 mA

TBA540 TBA540Q

PINNING

- | | |
|---------------------------------------|--|
| 1. Oscillator feedback output | 9. A.C.C. output |
| 2. Reactance control stage feedback | 10. A.C.C. level setting (see also pin 12) |
| 3. Supply voltage (12 V) | 11. A.C.C. gain setting |
| 4. Reference waveform output | 12. A.C.C. level setting (see also pin 10) |
| 5. Burst waveform input | 13. } D.C. control points for |
| 6. Reference waveform input | 14. } oscillator phase control loop |
| 7. Colour killer output | 15. Oscillator feedback input |
| 8. P.A.L. flip-flop square wave input | 16. Earth (negative supply) |

APPLICATION INFORMATION



7268303.1

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Oscillator feedback output

The crystal receives its energy from this pin. The input impedance is approximately 2 k Ω in parallel with 5 pF.

2. Reactance control stage feedback

This pin is fed internally with a sinewave derived from the reference input (pin 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12 V supply

The maximum voltage must not exceed 13.2 V.

4. Reference waveform output

This pin is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No d.c. load to earth is required. A d.c. connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase ($-(R-Y)$) to that on pin 4. A centre tap on the inductor, connected to earth via a d.c. blocking capacitor, is therefore necessary.

5. Burst waveform input

A burst waveform amplitude of 1 V peak-to-peak is required to be a.c. -coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the a.c.c. circuit. The input impedance at this pin is approximately 1 k Ω and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A d.c. bias of 400 mV is internally derived for pin 5. The absolute level of the tip of the burst at pin 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the i.c. which inhibits the performance of the phase lock loop.

APPLICATION INFORMATION (continued)

6. Reference waveform input

This pin requires a reference waveform in the -(R-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A d.c. connection between pins 4 and 6 must be made via the transformer.

7. Colour killer output

This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 k Ω) connected to +12 V. The unkillled and killed voltages on this pin are then +12 V and < 250 mV respectively. (The voltage on pin 9 at which switching of the colour killer output on pin 7 occurs is nominally +2.5 V)

8. P.A.L. flip-flop square wave input

A 2.5 V peak-to-peak square wave derived from the P.A.L. flip-flop (in the TBA520 demodulator i.c.) is required at this pin, a.c. -coupled via a capacitor. The input impedance is about 3.3 k Ω .

9. A.C.C. output

An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal the d.c. potential produced at pin 9 is set to be +4 V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the P.A.L. flip-flop is identified to be in the correct phase. The range of potential over which full a.c.c. control is exercised at pin 9 is determined by the control characteristics of the a.c.c. amplifier i.e. for the TBA560 from 1 V to 0.2 V. The potential at pin 9 will fall to a value within this range as the burst input signal is stabilised at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the P.A.L. flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a P.A.L. switch cut-off function in the TBA520 demodulator i.c. The switching of the colour killer output at pin 7 is designed to occur as the potential on pin 9 moves past +2.5 V.

10. A.C.C. level setting

The network connected between pins 10 and 12 balances the a.c.c. circuit and RV1 is adjusted to give +4 V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. A.C.C. gain control

RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 V peak-to-peak) under a.c.c. control;

12. See pin 10.

13. See pin 14.

APPLICATION INFORMATION (continued)14. D.C. control points in reference control loop

Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes d.c. balancing of the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R₂, C₂, R₃, C₃ and R₄, C₄. The d.c. potentials on these pins are nominally +7.2 V.

15. Oscillator feedback input

The input impedance at this pin is nominally 3.5 k Ω in parallel with 5 pF. No d.c. connection is required on this pin. The voltage in the i.c. between pin 15 and pin 1 is nominally 4.7 times.

16. Negative supply (earth)PERFORMANCE AND COMMENTSInitial adjustment

- (a) Remove burst signal.
- (b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.
- (c) Set the a.c.c. level adjustment RV1, to give +4 V on pin 9.
- (d) Apply burst signal.
- (e) Adjust a.c.c. gain, RV2, to give a burst amplitude of 1.5 V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

- (a) Phase difference between reference and burst signals for ± 400 Hz deviation of crystal frequency, $\pm 10^\circ$.
- (b) Typical holding range, ± 600 Hz.
- (c) Typical pull-in range, ± 300 Hz.
- (d) Temperature coefficient of oscillator frequency, i.c. only, 2 Hz/ $^\circ\text{C}$.

TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA550 is a silicon monolithic integrated signal processing circuit for television receivers. It combines following functions:

- video preamplifier with emitter follower output
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner (delayed)
- noise inverter for gating the a.g.c. and sync separator circuits
- sync separator
- automatic horizontal synchronisation
- vertical sync pulse separator
- blanking facility for the video amplifier

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages, and with n-p-n transistors in the tuner and i.f. amplifier. Only signals with negative modulation can be handled by the circuit.

QUICK REFERENCE DATA

Supply voltage	V_p	typ.	12	V
Ambient temperature	T_{amb}		25	$^{\circ}C$

Video input voltage (peak-to-peak voltage)	$V_{10-16(p-p)}$	typ.	2	V
Voltage gain of the the video amplifier	G_v	typ.	9,5	dB
A.G.C. voltage for i.f. part ($R_{4-16} = 2\text{ k}\Omega$)	V_{4-16}	typ.	0 to 8	V
A.G.C. voltage for tuner ($R_{6-16} = 1\text{ k}\Omega$)	V_{6-16}	typ.	0 to 7	V
Output voltage horizontal phase detector	$\pm V_{2-1}$	typ.	3	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{15-16(p-p)}$	>	10	V

PACKAGE OUTLINES (see general section)

TBA550 : 16-lead DIL; plastic.

TBA550Q: 16-lead QIL; plastic.

**TBA550
TBA550Q**

CIRCUIT DIAGRAM

**VERTICAL SYNC PULSE
SEPARATOR AND AMPLIFIER**

**NOISE GATED
SYNC SEPARATOR**

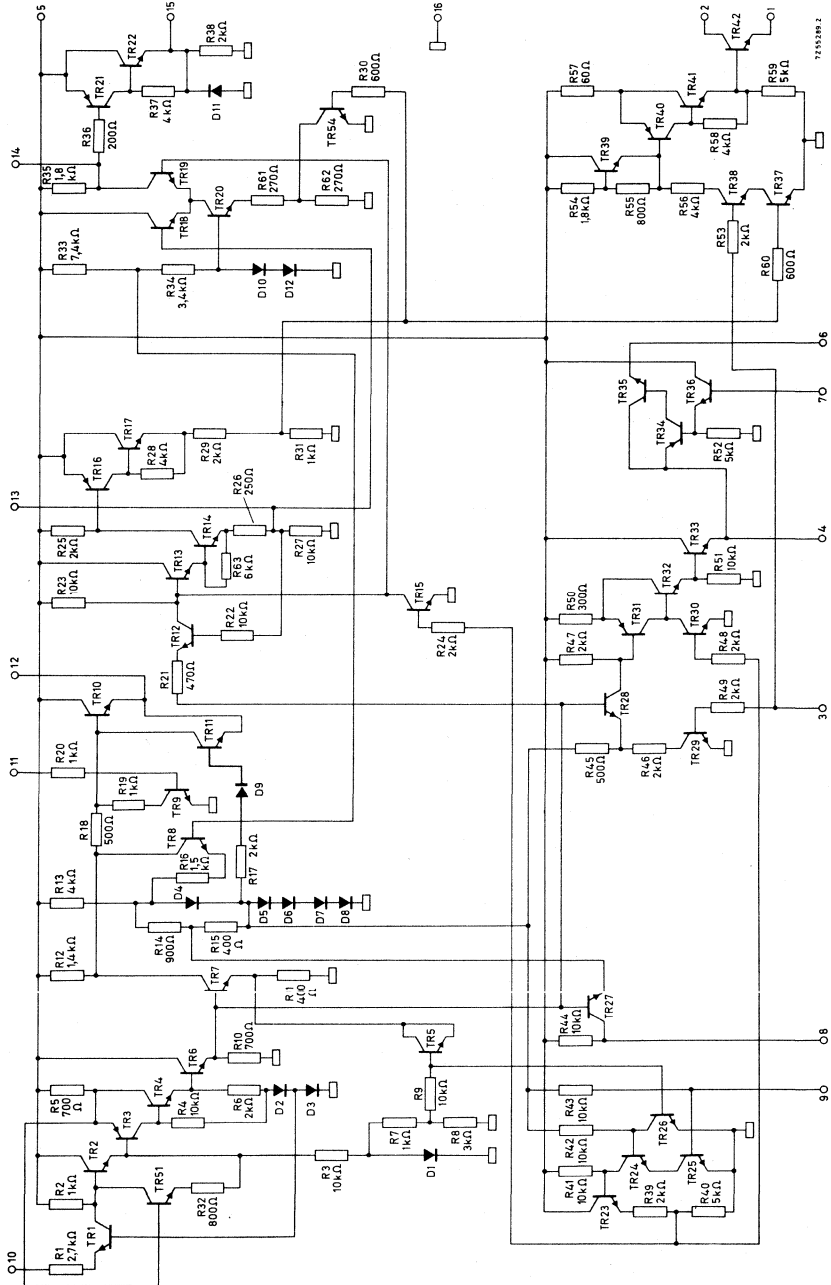
VIDEO PRE-AMPLIFIER

**HORIZONTAL PHASE
AND FREQUENCY
DETECTOR**

**TUNER A.G.C.
DELAY**

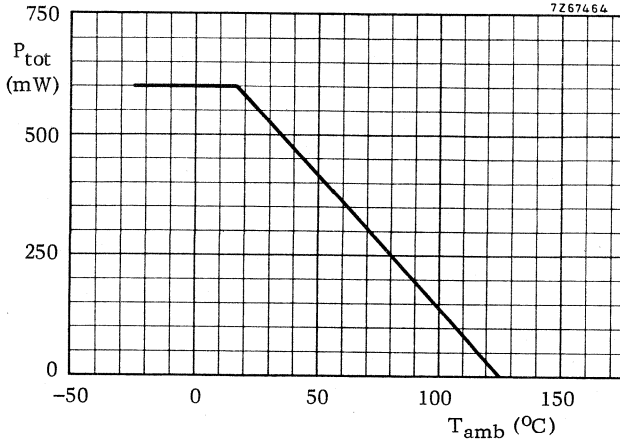
**KEYED AND NOISE
GATED A.G.C. DETECTOR**

NOISE SEPARATOR



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

<u>Supply voltage</u>	V_P	max.	16	V ¹⁾
<u>Power dissipation</u>	P_{tot}	max.	600	mW



Temperatures

Storage temperature	T_{stg}	-25 to +125	°C
Ambient temperature	T_{amb}	-25 to +125	°C

¹⁾ Permissible while tubes are heating up.

CHARACTERISTICS

Supply voltage range	V_P		10 to 14	V
Measured in circuit on page 6 at $T_{amb} = 25^\circ C$; $V_P = 12$ V				
<u>Video amplifier</u>				
Input resistance (detector load)	R_{10-16}	typ.	2,7	k Ω
Input capacitance	C_{10-16}	<	1	pF
Bandwidth (3 dB)	B	>	5	MHz
Voltage gain	G_V	typ.	9,5	dB
Video input voltage (peak-to-peak value)	$V_{10-16(p-p)}$	typ.	2	V ¹⁾
Video output voltage (peak-to-peak value)	$V_{12-16(p-p)}$	typ.	5,2	V ²⁾
Tolerances on video output voltage:				
I. C. processing spreads	$\pm\Delta V_{12-16}$	<	550	mV
Temperature drift	$-\Delta V_{12-16}$	<	20	mV/ $^\circ C$ ³⁾
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{12-16}$	<	270	mV ⁴⁾
Black level at the output	V_{12-16}	typ.	5	V ⁵⁾
Tolerances on the black level at the output				
I. C. processing spreads	$\pm\Delta V_{12-16}$	<	300	mV
Temperature drift	ΔV_{12-16}	<	7	mV/ $^\circ C$ ³⁾
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{12-16}$	<	250	mV ⁴⁾⁶⁾
Variation black level at the output due to supply voltage variations	$\frac{\Delta V_{12-16}}{\Delta V_P}$	typ.	0,7	
Available video output current (peak value)	I_{12M}	typ.	14	mA ⁷⁾

- 1) Negative going video signal (no pre-bias needed for the detector).
- 2) Video signal with negative going sync pulse.
- 3) Because the integrated circuit reaches 95% of its final working temperature in 100 seconds, the temperature variations to be considered are those caused by the slower rise in cabinet temperature and by changes in room temperature.
- 4) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled. The video signal increases and the black level decreases with increasing antenna signal.
- 5) Only valid if the video signal is in accordance with the CCIR standard.
- 6) To this must be added 0,7 ΔV_P , if operation of the a. g. c. causes a change in V_P .
- 7) The total load on pin 12 must be such that under nominal conditions $I_{12M} \leq 14$ mA.

CHARACTERISTICS (continued)

Video blanking

Input voltage (peak-to-peak value)	$V_{11-16(p-p)}$	1 to 5	V
Input resistance	R_{11-16}	typ. 1	k Ω

A.G.C. circuit

Control voltage i.f. amplifier	V_{4-16}	0 to 8	V	1)
Control voltage tuner	V_{6-16}	0 to 7	V	1)
Signal expansion for full control of i.f. amplifier and tuner		< 15	%	1)
Keying input pulse (peak-to-peak value)	$V_{3-16(p-p)}$	1 to 5	V	2)
Input resistance	R_{3-16}	typ. 1	k Ω	

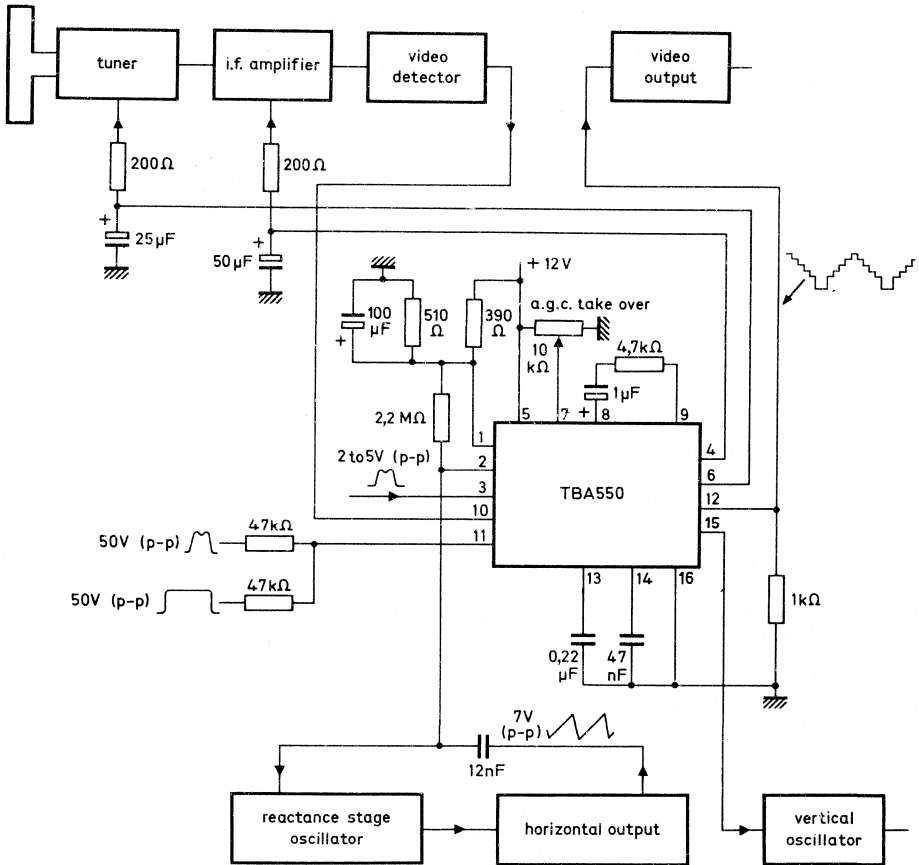
Synchronisation circuit

Sync separator		see note 3		
Control voltage line oscillator	$\pm V_{2-1}$	typ. 3	V	4)
Output voltage vertical sync pulse separator (peak-to-peak value)	$V_{15-16(p-p)}$	> 10	V	
Output impedance	R_{15-16}	typ. 2	k Ω	

- 1) These figures are obtained with a load impedance of 2 k Ω for the i.f. control point (R_{4-16}) and 1 k Ω for the tuner control point (R_{6-16}). With these impedances the signal expansion for i.f. control and tuner control will be about the same. An increase of these impedances will reduce the signal expansion. Lower values will reduce the available control voltage and increase the dissipation of the integrated circuit. Therefore, the minimum values must be restricted to 1, 5 k Ω for the i.f. control point and 750 Ω for the tuner control point.
- 2) The TBA550 may be operated unkeyed but then pin 3 must be connected to the positive supply line via a resistor of suitable value (e.g. 10 k Ω). However, the following consequences should be borne in mind:
 - The decoupling capacitors at the i.f. and tuner control points must be larger to prevent ripple voltages due to the vertical sync pulses. In consequence the a.g.c. will not follow fast signal fluctuations (airplane flutter).
 - Since the horizontal phase detector is designed to be keyed, unkeyed operation will result in the phase detector not operating as a frequency detector when the horizontal oscillator is out of sync. This considerably decreases the catching range.
- 3) The sync pulse is sliced about 30% below top sync level.
- 4) Required reference voltage $V_2(p-p)$ (sawtooth or differentiated line fly-back pulse) = 7 V. For an oscillator-reactance stage with a control sensitivity of 400 Hz/V this gives a holding range of about ± 1000 Hz.
Because the phase detector is keyed a catching range of ± 700 Hz is obtained without affecting the noise immunity.

TBA550 TBA550Q

APPLICATION INFORMATION



7255290.2

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TBA560C is a monolithic integrated circuit used in the decoding system of colour television receivers. The circuit consists of a luminance and a chrominance amplifier. The luminance amplifier input is matched to the luminance delay line and performs the following functions:

d.c. contrast control * brightness control * black level clamping * blanking.

The chrominance amplifier comprises:

gain-controlled amplifier * chrominance gain control tracked with contrast control * separate d.c. saturation control * PAL delay line driver * burst gate * colour killer. Compared with the TBA560B the TBA560C produces a higher gain of the burst signal and consequently a smaller ratio of the chrominance output signal to the burst output signal.

QUICK REFERENCE DATA

Supply voltage	V_{11-16}	nom.	12	V
Supply current	I_{11}	nom.	30	mA
Luminance signal input current	$I_3(p-p)$	typ.	1,5	mA
Chrominance input signal	$V_{1-15}(p-p)$	$\left\{ \begin{array}{l} > \\ < \end{array} \right.$	4 80	mV mV
Luminance output signal at nominal contrast setting	$V_{5-16}(p-p)$	typ.	3	V ¹⁾
Chrominance output signal at nominal contrast and saturation setting	$V_{9-16}(p-p)$	typ.	1	V ¹⁾
Contrast control range		\geq	20	dB
Saturation control range		\geq	20	dB
Burst output (closed a. c. c. loop)	$V_{7-16}(p-p)$	typ.	1	V

¹⁾ Nominal setting: maximum contrast and/or saturation minus 6 dB

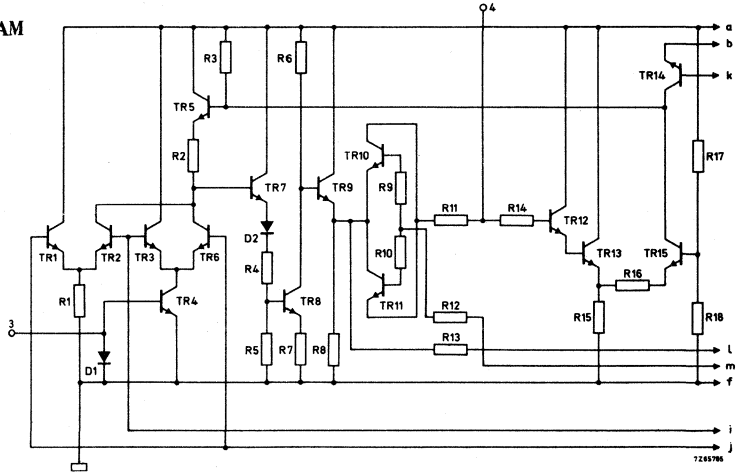
PACKAGE OUTLINES (see general section)

TBA560C : 16-lead DIL; plastic.

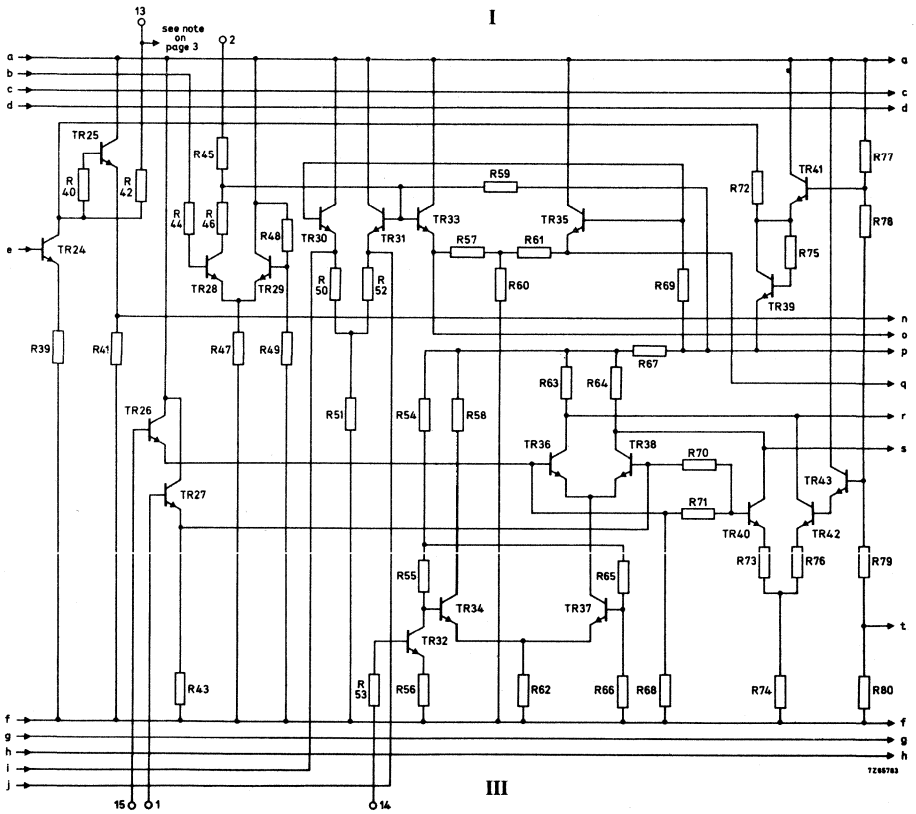
TBA560CQ: 16-lead QIL; plastic.

TBA560C TBA560CQ

CIRCUIT DIAGRAM

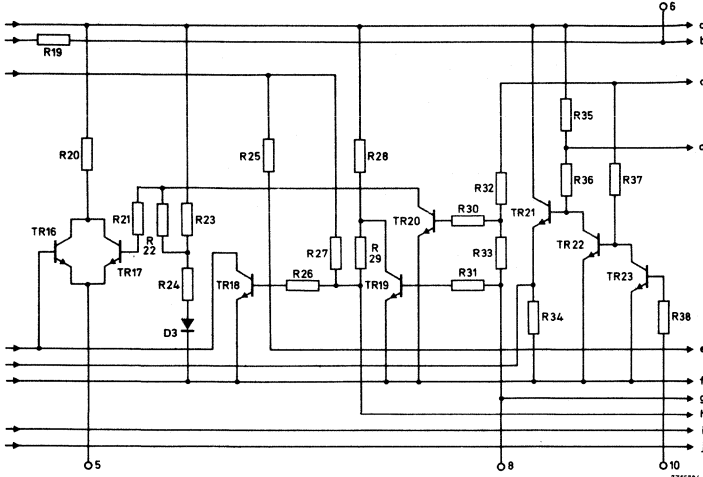


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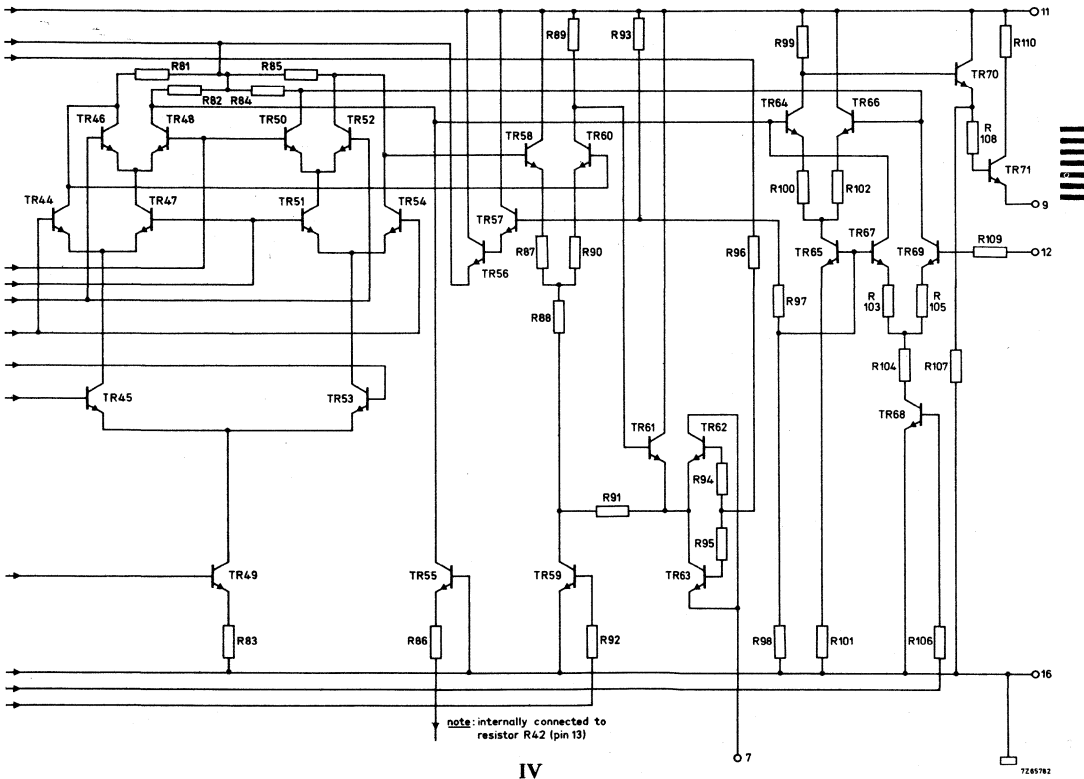


III

Note: the circuits are interconnected in the numerical sequence I, II, III, IV



II



IV

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{11-16} max. 13 V ¹⁾

Power dissipation

Total power dissipation P_{tot} max. 510 mW ¹⁾

Temperatures

Storage temperature T_{stg} -25 to +125 °C

Operating ambient temperature T_{amb} 0 to +60 °C

Voltages with respect to pin 16

V_{1-16}	0 to +5 V	V_{10-16}	min. -5 V
V_{2-16}	0 to +12 V ²⁾	V_{12-16}	-5 to +6 V
V_{4-16}	0 to +6 V	V_{13-16}	-3 to +6,5 V ²⁾
V_{6-16}	0 to +3 V	V_{14-16}	min. -5 V
V_{8-16}	-5 to +5 V	V_{15-16}	0 to +5 V

Currents (positive when flowing into the integrated circuit)

I_1	0 to +1 mA	I_7	-3 to +2 mA
I_3	-1 to +3 mA	I_9	-10 to 0 mA
I_5	-5 to 0 mA	I_{10}	max. +3 mA
I_6	-1 to +1 mA	I_{14}	max. +1 mA
		I_{15}	0 to +1 mA

1) Permissible while tubes are heating up: V_{11-16} max. 16 V and P_{tot} max. 700 mW.

2) V_{2-16} and V_{13-16} must always be lower than V_{11-16} .

CHARACTERISTICS measured in the circuit on page 6

<u>Supply voltage</u>	V_{11-16}	typ.	12	V
			10 to 13	V
Required input signals at $V_{11-16} = 12\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$				
<u>Chrominance input signal</u>				
peak-to-peak value	$V_{1-15(p-p)}$		4 to 80	mV
<u>Luminance input current</u>				
black-to-white value	I_3	typ.	1,5	mA
<u>Contrast control voltage range</u>				
for 20 dB of control	V_{2-16}		see graph on page 11	
<u>Brightness control voltage</u>				
	V_{6-16}		see graph on page 11 ¹⁾	
<u>Saturation control voltage range</u>				
for 20 dB of control	V_{13-16}		see graph on page 11	
<u>Burst keying pulse (positive)</u>				
peak-to-peak value	$I_{10(p-p)}$		0,05 to 1	mA
<u>Fly-back blanking pulses (negative)</u>				
peak-to-peak value				
for 0 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	-0,5	V
for 1,5 V blanking level at pin 5	$V_{8-16(p-p)}$	typ.	-2,5	V
<u>Colour killer</u>				
	V_{13-16}	<	1	V
<u>Automatic chrominance control starting</u>				
	V_{14-16}	typ.	1,2	V ²⁾

¹⁾ When V_{6-16} is increased above 1,7 V the black level of the output signal remains at 2,7 V

²⁾ A negative going potential provides a 26 dB a.c.c. range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of min. 500 mV.

TBA560C TBA560CQ

CHARACTERISTICS (continued)

Obtainable output signals

Luminance output voltage at nominal

contrast (peak-to-peak value) $V_{5-16(p-p)}$ typ. 3 V ¹⁾

Burst signal (peak-to-peak value) $V_{7-16(p-p)}$ typ. 1 V ²⁾

Chrominance signal at nominal

contrast and saturation (peak-to-peak value) $V_{9-16(p-p)}$ typ. 1 V ¹⁾

3 dB bandwidth of chrominance and

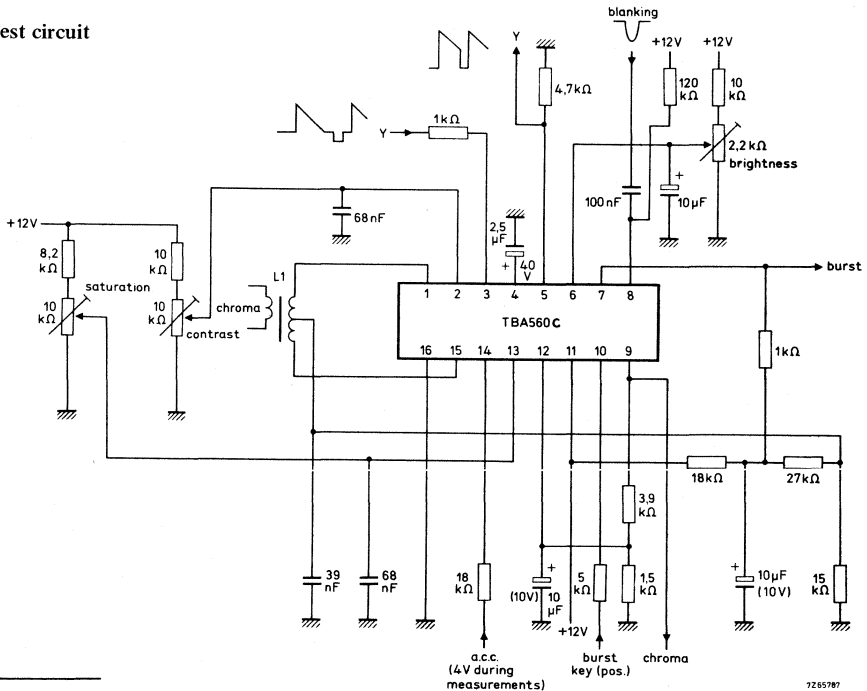
luminance amplifier B typ. 5 MHz

Change of ratio luminance to

chrominance signals at 10 dB

contrast control < 2 dB

Test circuit

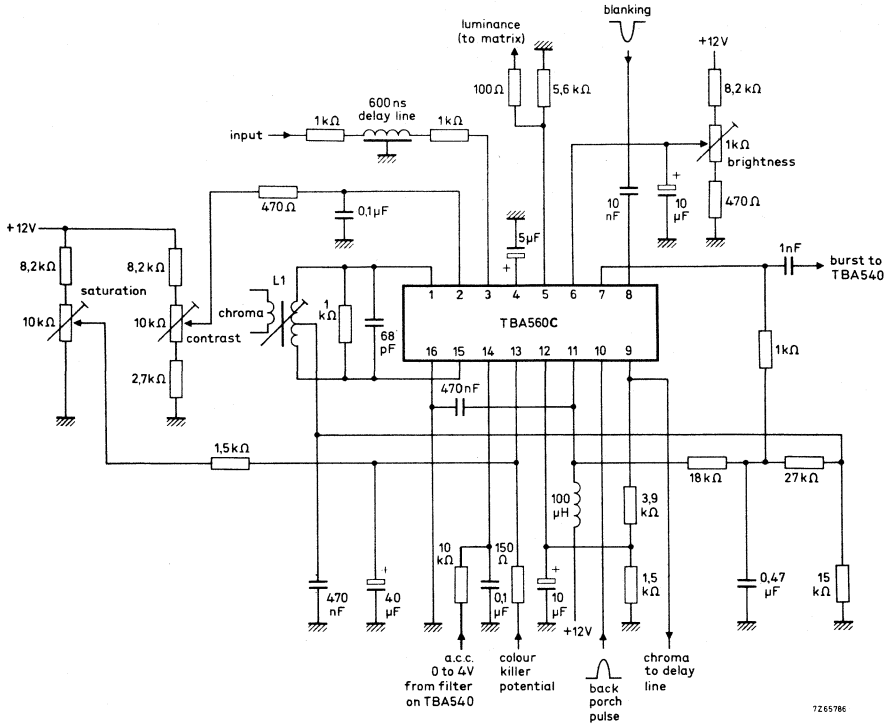


1) Nominal setting: maximum contrast and/or saturation minus 6 dB.

2) Burst signal is kept constant at 1 V peak-to-peak by automatic gain control.

7265787

APPLICATION INFORMATION



Application diagram for operation in combination with the TBA540.

APPLICATION INFORMATION (continued)

Pinning

- | | |
|---------------------------------|---|
| 1. Balanced chroma signal input | 9. Chroma signal output |
| 2. Contrast control | 10. Burst gate and clamping pulse input |
| 3. Luminance signal input | 11. Supply voltage (12 V) |
| 4. Black level clamp capacitor | 12. D.C. feedback for chroma channel |
| 5. Luminance signal output | 13. Chroma saturation control |
| 6. Brightness control | 14. A.C.C. input |
| 7. Burst output | 15. Chroma signal input |
| 8. Fly-back blanking input | 16. Earth (negative supply) |

The function is quoted against the corresponding pin number

1. Balanced chroma signal input (in conjunction with pin 15)

This is derived from the chroma signal bandpass filter, designed to provide the push-pull input. An input signal amplitude of at least 4 mV peak-to-peak is required on pins 1 and 15. Both pins require a d.c. potential of approximately +3,0 V. This is derived as a common-mode signal from a network connected to pin 7 (burst output). In this way d.c. feedback is provided over the burst channel to stabilise its operation.

All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chroma ratio of input signal is 1 : 2.

2. D.C. contrast control

With +3,7 V on this pin, the gain in the luminance channel is such that a 1,5 mA peak-to-peak input signal to pin 3 gives a luminance output signal amplitude on pin 5 of 3 V black-to-white. A variation of voltage on pin 2 between +6 V and +2 V gives a corresponding gain variation of +6 to > -14 dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals.

3. Luminance signal input

This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and must have about 1,5 mA black-to-white amplitude.

4. Charge storage capacitor for black level clamp (5,0 μ F)

5. Luminance signal output

An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 0 to +3 V. An external emitter load resistor is required, not less than 1 k Ω .

Black level shift at contrast control is max. \pm 20 mV if the luminance input current during black level is about 0,75 mA. When this current has a different value a larger black level shift has to be taken into account. If the input current during black level differs 1 mA from the nominal value of 0,75 mA, the black level shift will be about 100 mV over the complete contrast control range. For smaller differences of the input current the black level shift will be correspondingly smaller.

Black level shift with video signal content occurs only when the input signal is a.c. coupled. The value depends on the drive current amplitude and can be calculated from

APPLICATION INFORMATION (continued)

the figures given above (for maximum contrast; for a lower contrast setting the variation is correspondingly smaller).

Black level shift over an ambient temperature variation of 30 °C is typ. -140 mV.

6. The d.c. level of the luminance output signal may be controlled by the d.c. potential applied to this pin

Over the range of potential +0,9 to +1,7 V the black level of the luminance output signal (pin 5) is increased from 0 to +2,7 V. The output signal black level remains at +2,7 V when the potential on pin 6 is increased above +1,7 V.

7. Burst output

A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here. Also, to achieve good d.c. stability by negative feedback in the burst channel the d.c. potential at this pin is fed back to pins 1 and 15 via the chroma input transformer. When limiting occurs the burst amplitude is min. 2,5 V.

8. Fly-back blanking input waveform

Negative-going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of not greater than -1 V negative excursion are applied the signal level at the luminance output (pin 5) during blanking will be 0 V. However, if the blanking pulses applied to pin 8 have an amplitude of -2 to -3 V the signal level at the luminance output during blanking will be +1,5 V.

9. Chroma signal output

With an 1 V peak-to-peak burst output signal (pin 7) and at nominal contrast and saturation setting (pins 2 and 13) the chroma signal output amplitude is 1 V peak-to-peak. An external d.c. network is required which provides negative feedback in the chroma channel via pin 12.

10. Burst gating and clamping pulse input

A positive pulse of minimum 50 µA is required on this pin to provide gating in the burst channel and luminance channel black-level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync pulse or picture line periods during normal operation of the receiver.

11. +12 V L.T power supply

Correct operation occurs within the range 10 to 13 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 550 mW at 60 °C ambient temperature.

12. D.C. feedback for chroma channel (see pin 9)

13. Chroma saturation control

A control range of +6 to > +14 dB is provided over a range of d.c. potential on pin 13 from +2,7 to +6,2 V. Colour killing is also done at this terminal by reducing the d.c. potential to less than +1 V, e.g., from the TBA540 colour killer output terminal. The kill factor is min. 40 dB.

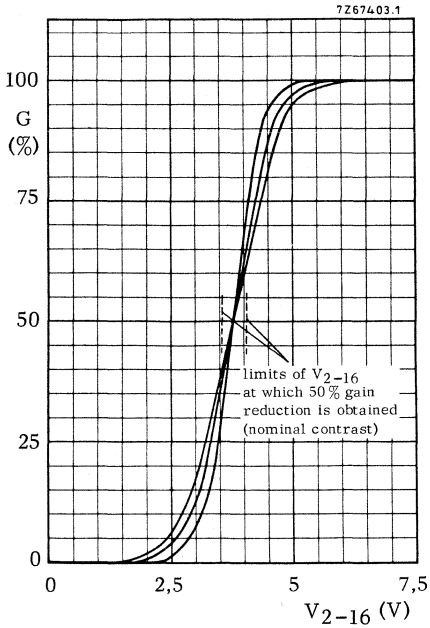
APPLICATION INFORMATION (continued)

14. A.C.C. input

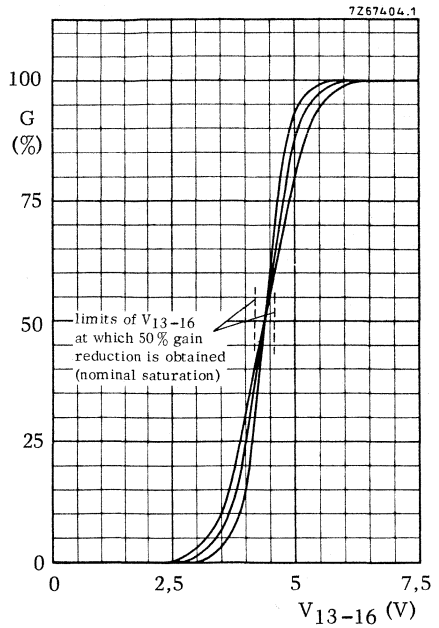
A negative-going potential gives a 26 dB range of a.c.c. starting at +1, 2 V and giving maximum gain reduction at an input voltage of min. 500 mV.

15. Chroma signal input (see pin 1)

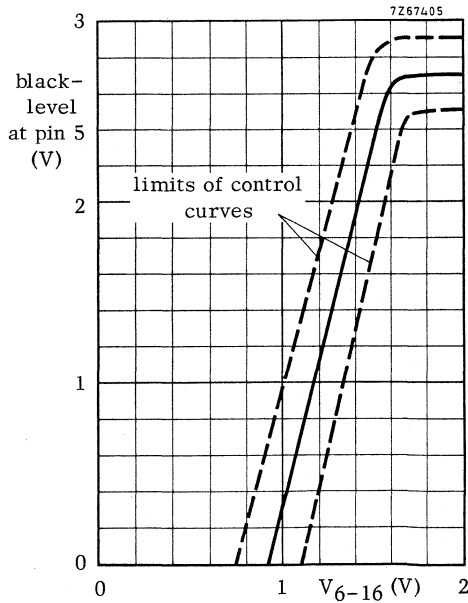
16. Negative supply (earth)



Contrast control of luminance amplifier



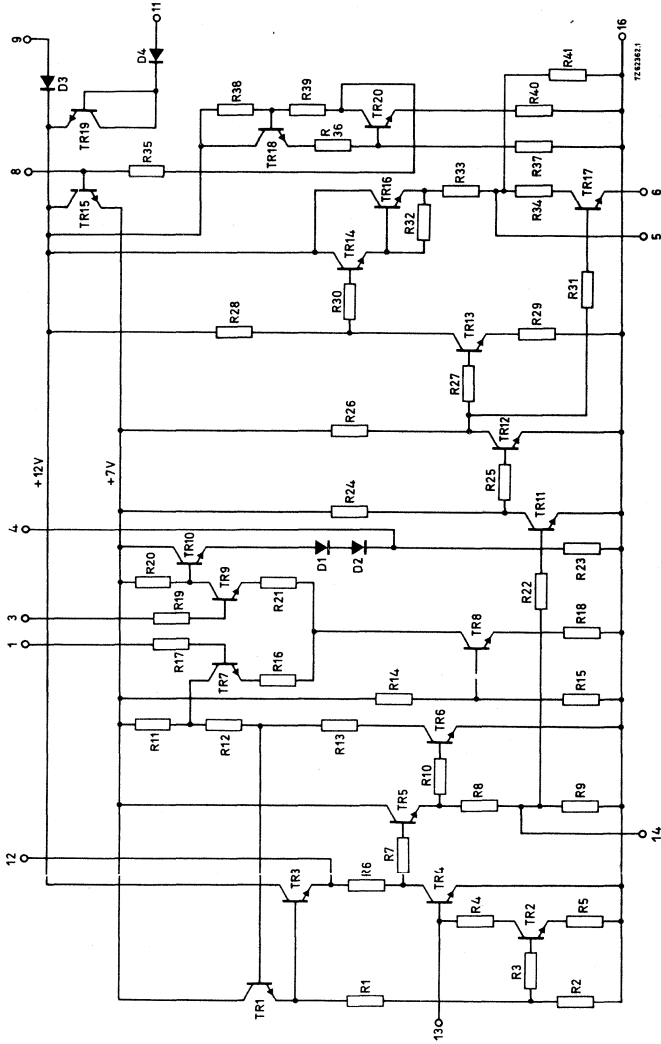
Saturation of chrominance amplifier



Control of black level at output luminance amplifier

**TBA720A
TBA720AQ**

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages

Supply voltage	V_{11-16}	max.	16 V
Starting voltage	V_{9-16}	max.	15 V

Currents

Output current	I_5	max.	60 mA
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Power dissipation

Total power dissipation when mounted on a printed-wiring board	P_{tot}	max.	280 mW
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Temperatures

Storage temperature	T_{stg}	-55 to +125 °C
Operating ambient temperature	T_{amb}	0 to +60 °C

CHARACTERISTICS Measured in the test set-up on page 4

Supply voltage	V_{11-16}	typ.	12 V 10 to 13 V
Starting voltage	V_{9-16}	>	8 V ¹⁾

CHARACTERISTICS at $T_{amb} = 25$ °C; $V_{11-16} = 12$ V

Supply current ²⁾	I_{11}	typ.	10,5 mA 7,5 to 13,5 mA
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Required input signals

D.C. control voltage for nominal frequency at pin No. 1 and pin No. 3	$V_{1-16} = V_{3-16}$		2,4 to 5,3 V
Sensitivity of reactance stage	V_{1-3}	typ.	2 kHz/V
Duty cycle regulation at pin No. 14	I_{14}	typ.	0 μ A +400 to -400 μ A

Delivered output signals

Output voltage at pin No. 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	8 V
Output current	I_5	<	60 mA
Duty cycle; without regulation	δ	{ typ.	40 % 35 to 45 %
with regulation	δ		20 to 60 %
Rise time at pin No. 5 leading edge of output pulse	t_r	typ.	200 ns

¹⁾ Maximum starting voltage should not exceed the value of the supply voltage minus 1 volt.

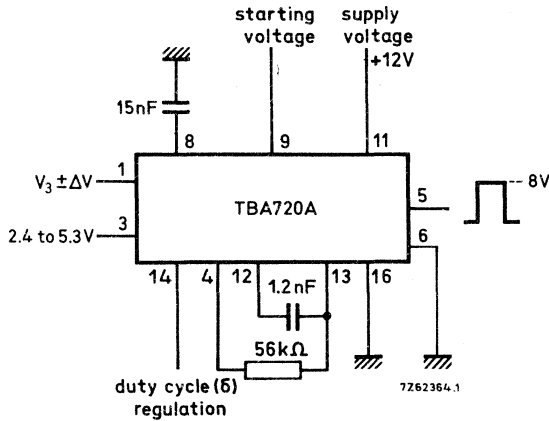
²⁾ No load connected to the output. When the output is loaded, the extra current is: $\delta \times I$, in which δ = duty cycle of output pulse and I = current flowing during output pulse.

TBA720A TBA720AQ

CHARACTERISTICS (continued)

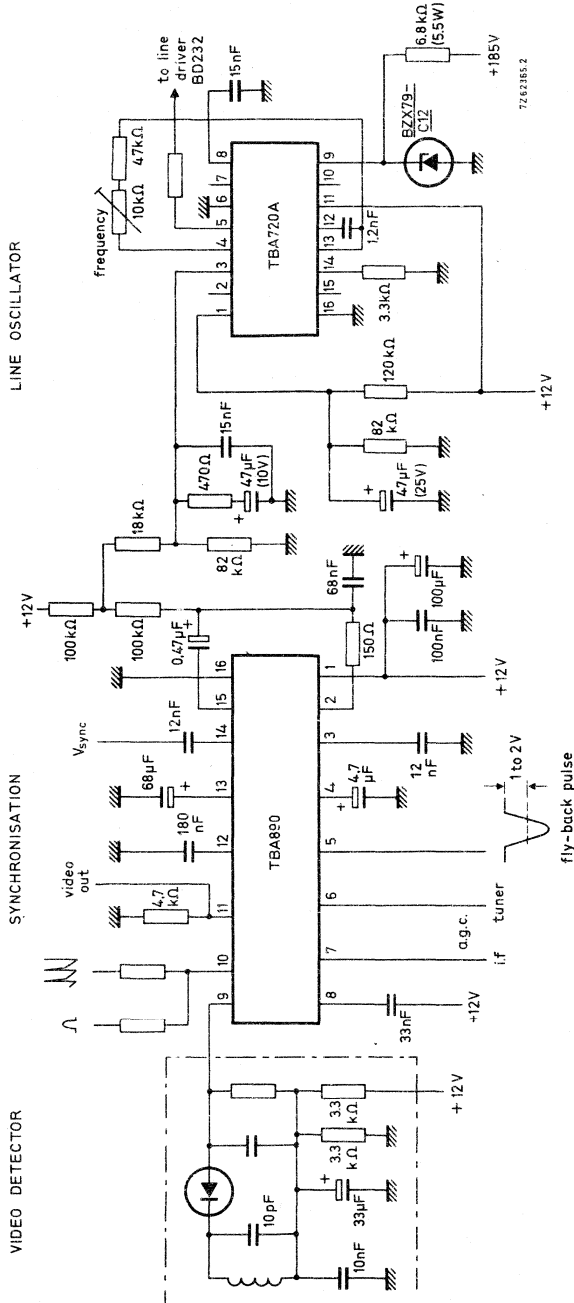
Relative frequency deviation for $\Delta V_{11} = 1\text{ V}$	2 ‰
Relative frequency deviation for change of ambient temperature 25 to 55 °C	3 ‰
Allowable hum-ripple on supply line (peak-to-peak value)	$\Delta V_{11-16}(\text{p-p})$ typ. 100 mV

Test set-up



APPLICATION INFORMATION

The TBA720A with the TBA900 or TBA890 in a receiver with transistorized line deflection.



APPLICATION INFORMATION (continued)

Notes

1. The TBA720A is intended to drive a line deflection circuit equipped with transistors.
2. The duty cycle δ can be adjusted by connecting a resistor between pin 14 and ground or the supply.
3. The oscillation frequency can be set between 10 kHz and 25 kHz by connecting a resistor between pins 4 and 13, and a capacitor between pins 12 and 13.
4. At a nominal oscillation frequency of 15,625 kHz, the frequency deviation is limited to $\pm 1,3$ kHz to safeguard the line timebase output circuits.
5. Besides the oscillator, the TBA720A incorporates a reactance stage and a supply voltage take-over switch for starting purposes (pin 9). The latter can be used to advantage if the 12 V supply is derived from the line flyback pulse.
6. Pins 2, 7, 10 and 15 should not be connected.

LIMITER-AMPLIFIER

The TBA750A is a limiter-amplifier with f.m. detector, d.c. volume control and a.f. preamplifier. It is intended for 4,5 MHz, 5,5 MHz or 10,7 MHz.

The limiter-amplifier is a four-stage differential amplifier that gives very good noise and interference suppression.

The detector is of the balanced type. The d.c. volume control stage has excellent control characteristics with a control range of more than 80 dB.

The a.f. preamplifier can drive a triode-pentode output stage or a class-A push-pull transistor output stage.

QUICK REFERENCE DATA

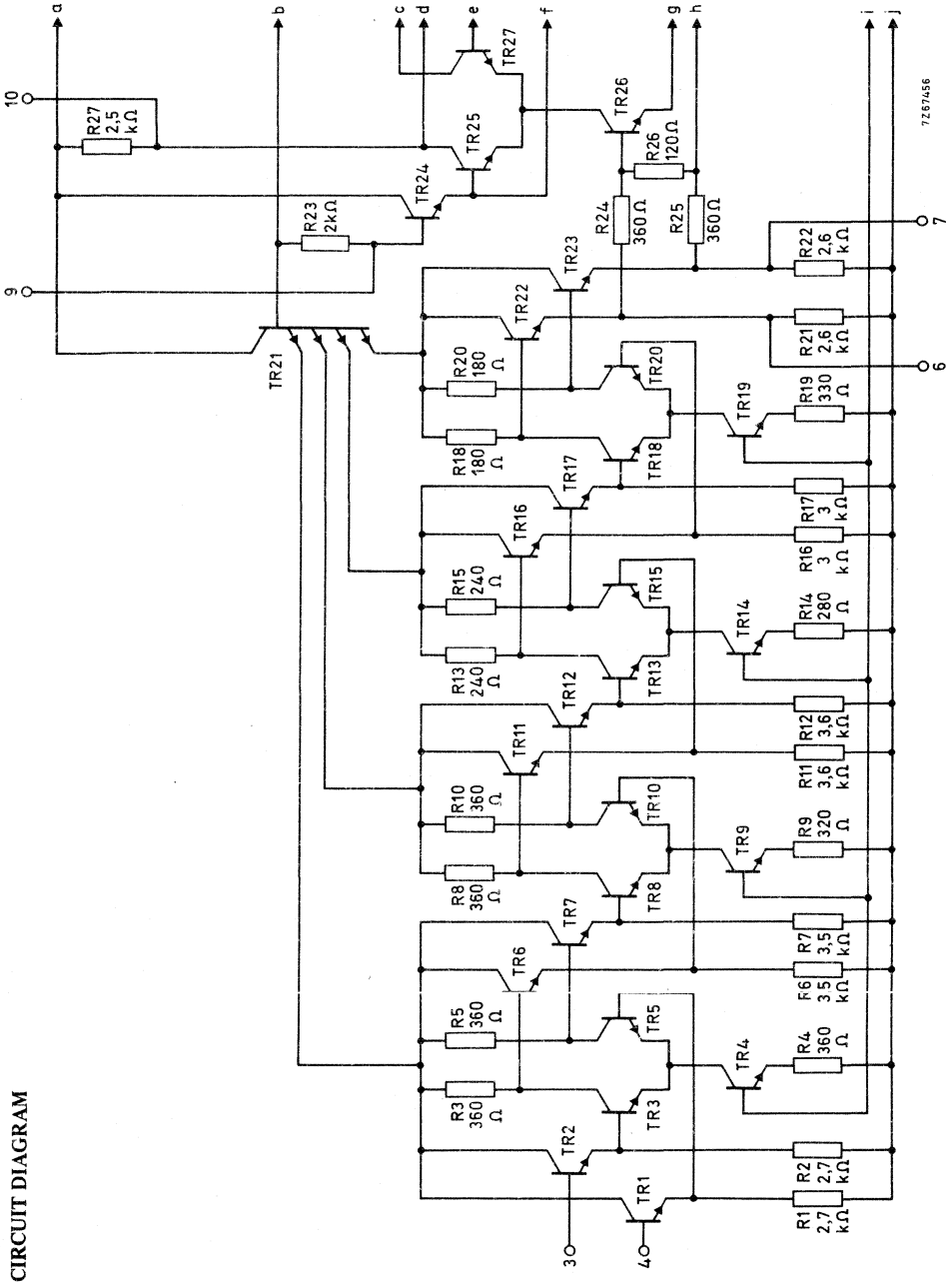
Supply voltage	V_{2-5}	typ.	12	V
Total current drain	I_{tot}	typ.	34	mA
Frequency	f_o		5,5	MHz
Input voltage at start of limiting	$V_{i\ lim}$	typ.	130	μV
A.M. rejection at $V_i = 1\ mV$	α	typ.	45	dB
A.F. output voltage at $\Delta f = \pm 15\ kHz$ at pin 16	$V_{o(rms)}$	typ.	2,7	V
D.C. volume control range		>	80	dB

PACKAGES OUTLINES (see general section)

TBA750A : 16-lead DIL; plastic.

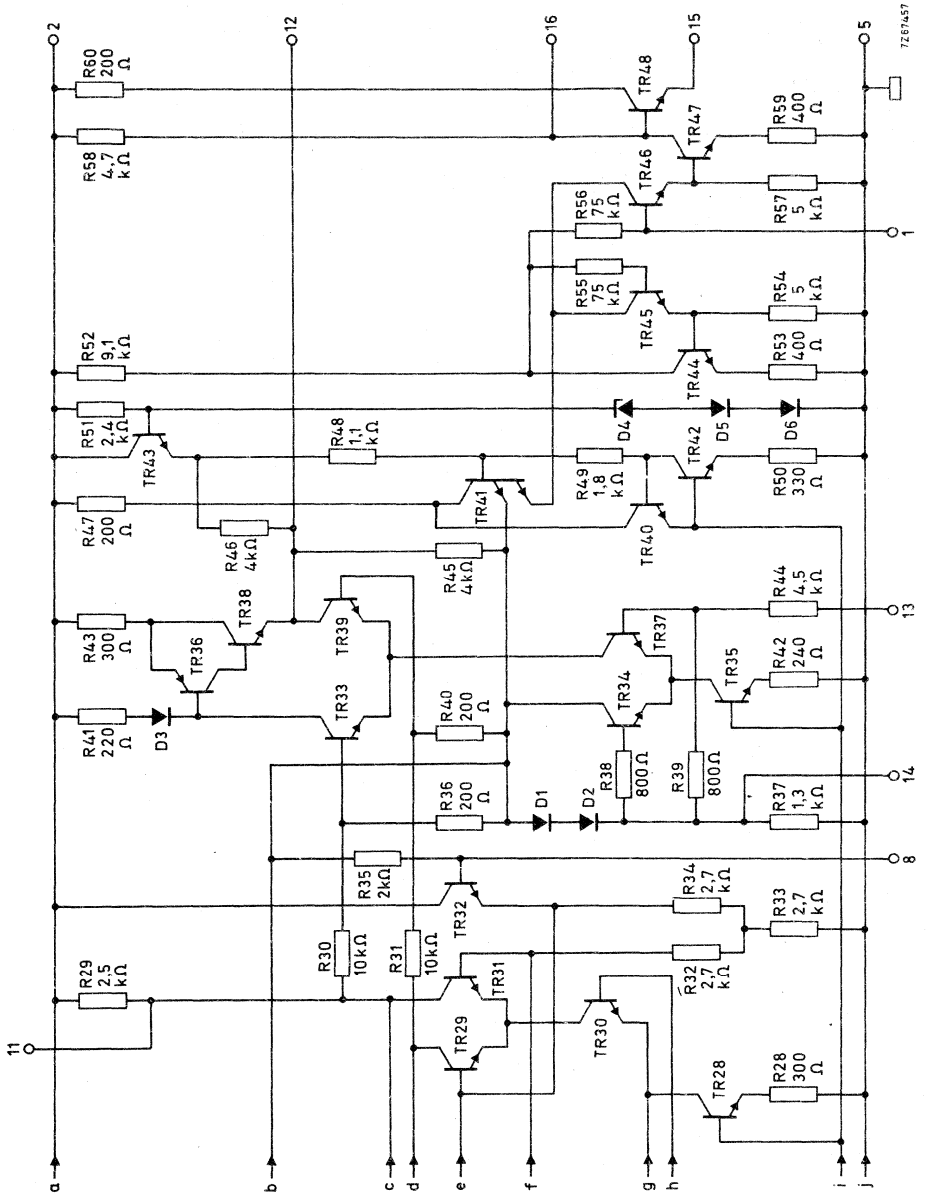
TBA750AQ: 16-lead QIL; plastic.

**TBA750A
TBA750AQ**



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CIRCUIT DIAGRAM

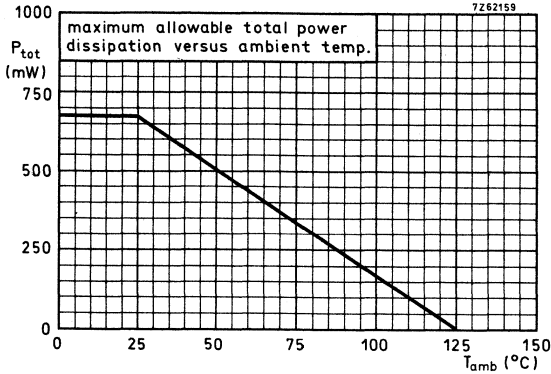


TBA750A
TBA750AQ

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage V_{2-5} max. 16 V ¹⁾

Power dissipation



Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} -25 to +55 °C

CHARACTERISTICS measured in the test circuit on page 5.

Supply voltage range

(See graph R_S versus supply voltage on page 6)

V_{2-5} 10 to 25 V

Total current drain

I_2 25 to 45 mA ²⁾

Input limiting voltage at $V_O = -3$ dB

V_i lim(rms) typ. 130 μ V

I. F. output voltage at pin 6 and 7

(peak-to-peak value)

V_{6-5} (p-p) } typ. 380 mV
 V_{7-5} (p-p) }

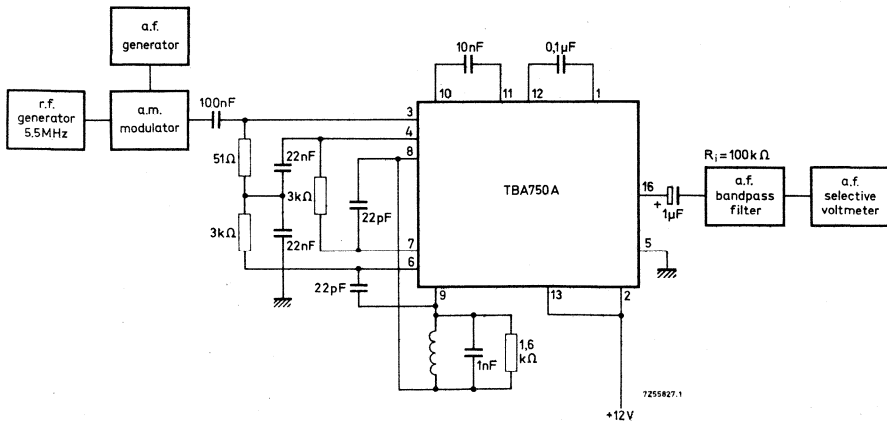
¹⁾ Allowable only if the dissipation in the IC is limited by means of a series resistor in the supply (see upper graph on page 6).

²⁾ Pin 15 not connected.

CHARACTERISTICS (continued)

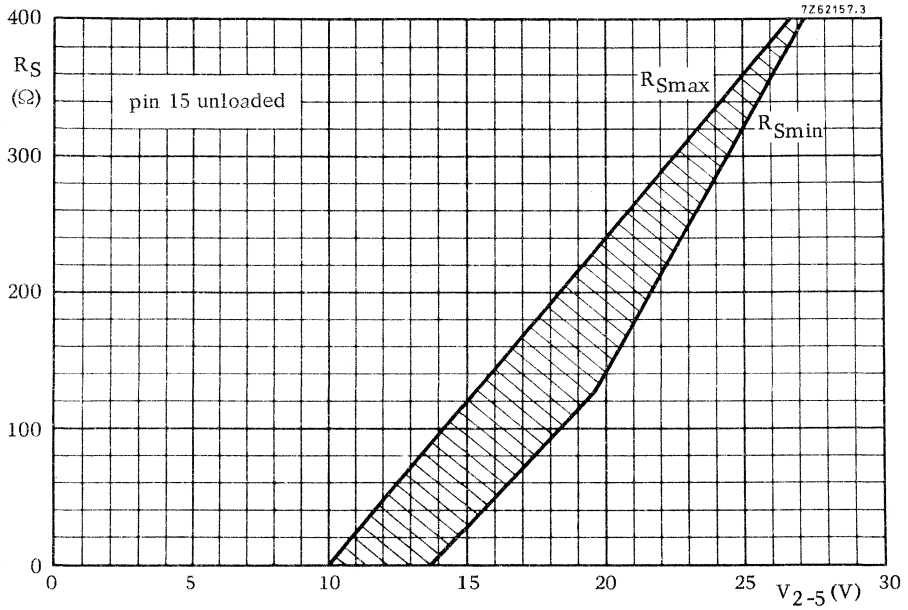
<u>A. M. rejection</u> at $V_i = 1 \text{ mV}$	α	typ.	45	dB
$V_i = 10 \text{ mV}$	α	typ.	50	dB
$V_i = 100 \text{ mV}$	α	typ.	55	dB
<u>D. C. volume control range</u>		>	80	dB ¹⁾
<u>A. F. preamplifier voltage gain</u> (pin 1 to pin 16)	G_v	typ.	10	
<u>Input resistance</u> at pin 1	R_i	\geq	35	k Ω
<u>A. F. output voltages</u> $\Delta f = \pm 15 \text{ kHz}; f_m = 1 \text{ kHz}$	$V_{10-5} \text{ (rms)}$ $V_{11-5} \text{ (rms)}$	typ.	65	mV
	$V_{12-5} \text{ (rms)}$ $V_{16-5} \text{ (rms)}$			
<u>Total harmonic distortion</u> at pin 12; $\Delta f = 15 \text{ kHz}$	d_{tot}	typ.	3	%
at pin 1 with respect to pin 16; $V_o(\text{rms}) = 3 \text{ V}$	d_{tot}	typ.	2,6	%

Test circuit for f. m. : $f_o = 5,5 \text{ MHz}; \Delta f = \pm 15 \text{ kHz}; f_m = 70 \text{ Hz}$
for a. m. : $m = 0,3; f_m = 1 \text{ kHz}$

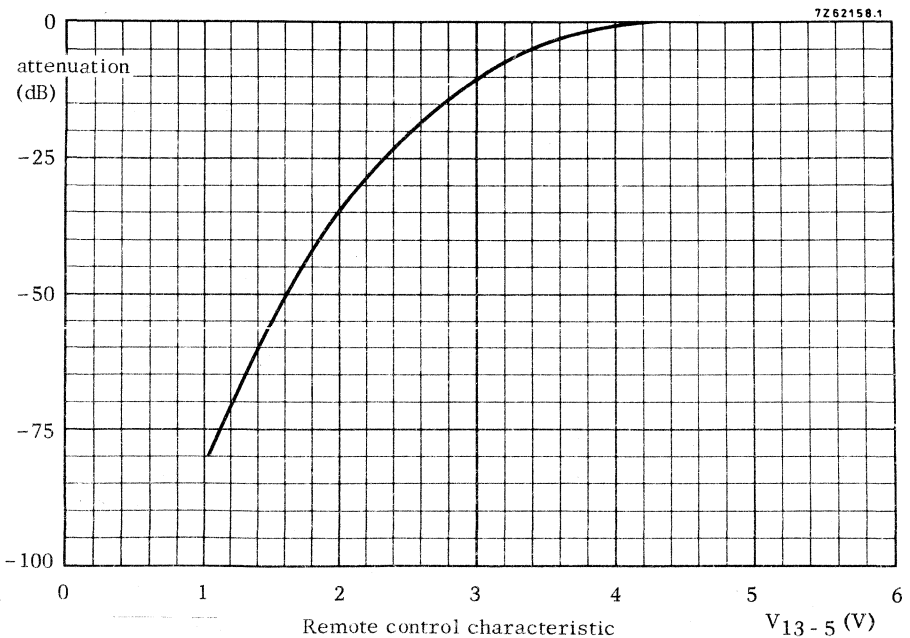


¹⁾ See lower graph on page 6.

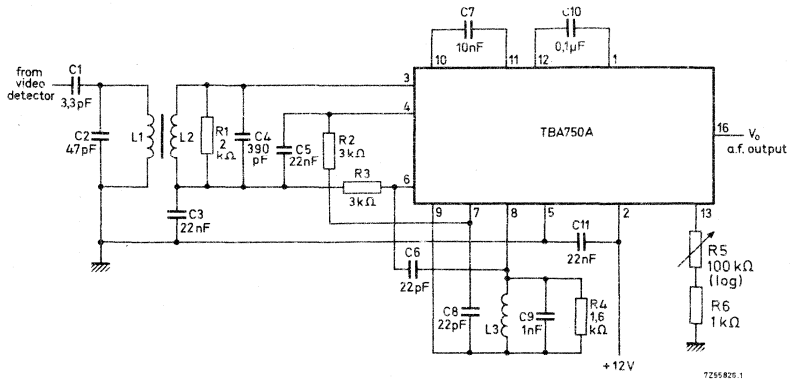
CHARACTERISTICS (continued)



Maximum and minimum values for the power supply series resistance (R_S)



APPLICATION INFORMATION at $f = 5,5 \text{ MHz}$



$L1 = 18 \mu\text{H}; Q_{L1} = 36$

$L2 = 2,2 \mu\text{H}; Q_{L2} = 21$

$L3 = 0,84 \mu\text{H}; Q_{L3} = 22$

Note: Q_{L1} , Q_{L2} and Q_{L3} are the loaded Q-factors.

The transfer ratio of the input bandpass filter: $\frac{V_2}{V_1} = 0,54$

The peak-to-peak bandwidth of the detector S-curve is 300 kHz.

TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA890 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.

It combines the following functions:

- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator.
- automatic horizontal phase detector
- vertical sync pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.

The control stages in the i.f. amplifier and the tuner have to be equipped with n-p-n transistors. The equivalent circuit for tuners equipped with a p-n-p transistor is the TBA900. The circuit is developed for signals with negative modulation.

QUICK REFERENCE DATA

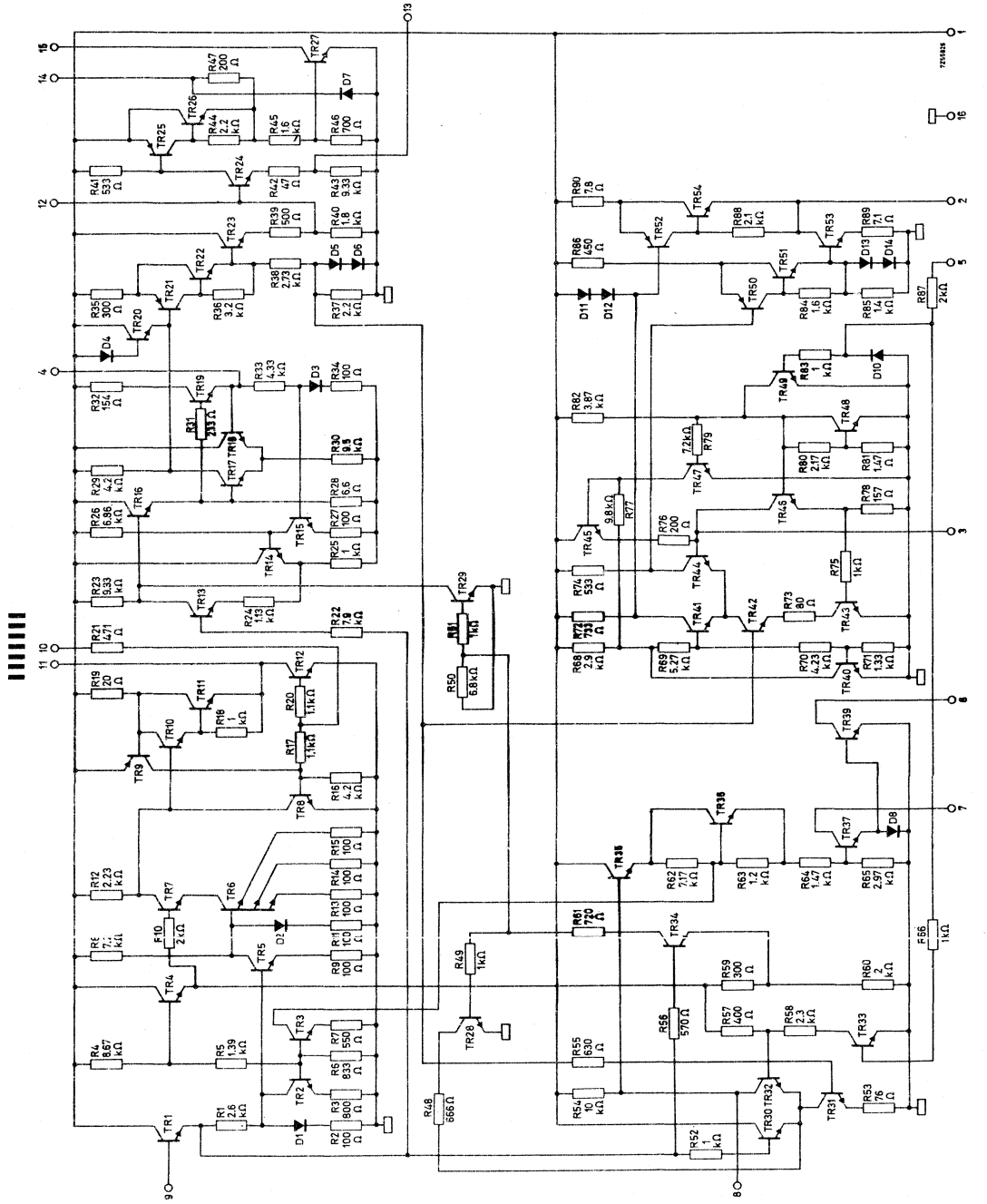
Supply voltage	V_P	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7	V
Voltage gain of the video amplifier	G_V	typ.	7	dB
A.G.C. voltage for i.f. part	V_{7-16}		1,0 to 12	V
A.G.C. voltage for tuner	V_{6-16}		0,3 to 12	V
Output voltage range horizontal phase detector	V_{2-16}		2 to 10	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{14-16(p-p)}$	typ.	11	V

PACKAGE OUTLINES (see general section)

TBA890 : 16-lead DIL; plastic.

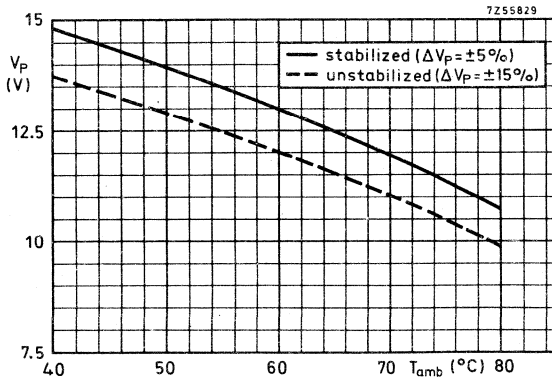
TBA890Q: 16-lead QIL; plastic.

TBA890 TBA890Q



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

<u>Supply voltage</u>	V_P	max.	20	V ¹⁾
<u>Power dissipation</u>	P_{tot}	max.	700	mW
<u>Temperatures</u>				
Storage temperature	T_{stg}	-55 to	+125	°C
Operating ambient temperature	T_{amb}	-25 to	+80	°C



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

1) Allowed only while receiver is warming up.

CHARACTERISTICS

Supply voltage range

V_P

See curves on page 3

The following characteristics are measured in the circuit on p. 7 at $T_{amb} = 25^\circ C$;
 $V_P = 12 V$.

Video amplifier

Input resistance	R_{9-16}	>	30	$k\Omega$
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity (m)		>	0.9	
Rise time and fall time at the output	$t_R; t_f$	<	50	ns
Voltage gain	G_V	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	$V^1)$
D.C. bias video detector voltage	V_{bias}	typ.	6	$V^2)$
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	$V^1)$
Black level at the output	V_{11-16}	typ.	5	$V^3)$
Available video output current (peak value)	I_{11M}	\leq	30	$mA^4)$

Tolerances on the video output voltages

I. C. processing spreads	$\pm \Delta V_{11-16}$	<	420	$mV^5)$
Temperature drift	$-\Delta V_{11-16}$	typ.	1.8	$mV/^\circ C$
Spreads over a. g. c. expansion (entire range)	$\pm \Delta V_{11-16}$	<	100	$mV^6)$
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.5	

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C. C. I. R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C. C. I. R. standard.

4) The total load on pin 11 must be such that the d. c. output current $I_{11} \leq 15 mA$.

5) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure.

6) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output

I. C. processing spreads	$\pm\Delta V_{11-16}$	< 420	mV ¹⁾
Temperature drift	$-\Delta V_{11-16}$	typ. 1.7	mV/°C
Spreads over a. g. c. expansion (entire range)	$\pm\Delta V_{11-16}$	< 130	mV ²⁾
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_p}$	typ. 0.4	

Video blanking

Input voltage (peak-to-peak value)	$V_{10-16(p-p)}$	1 to 5	V
Input resistance	R_{10-16}	typ. 1	k Ω
Output voltage during blanking	V_{11-16}	< 500	mV

A. G. C. circuit

Range of control voltage i. f. amplifier	V_{7-16}	1 to 12	V ³⁾
Range of control voltage tuner	V_{6-16}	0.3 to 12	V ³⁾
Signal expansion for full control of i. f. amplifier and tuner		typ. 0.5	dB
Current i. f. control point	I_7	< 20	mA
Current tuner control point	I_6	< 20	mA
Current i. f. control point for tuner take-over	I_7	see note 4	
Keying input pulse (peak-to-peak value)	$V_{5-16(p-p)}$	see note 5	
Input resistance	R_{5-16}	typ. 2	k Ω

- 1) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure (pin 9).
- 2) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled.
- 3) Positive going at increasing input signal.
- 4) This value depends on the ratio between the external impedances on pins 6 and 7. With equal impedances the current of the i. f. control point at tuner take-over will be about 16% from its maximum value (minimum control voltage).
- 5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit

Sync. separator		see note 1
Output voltage range of phase detector	V_{2-16}	2 to 10 $V^{2)}$
Control steepness	S_{φ}	typ. 2.5 $V/\mu s^3)$
Phase deviation between front edge sync. pulse and front edge flyback pulse	φ_0	typ. 1.5 μs
Variation φ_0 caused by internal spreads	$\pm\Delta\varphi_0$	typ. 0.3 $\mu s^4)$
Output voltage range as a frequency detector	V_{2-16}	4 to 8 $V^5)$

Vertical synchronization circuit

Output voltage vertical sync. pulse generator	V_{14-16}	typ. 11 V
Output impedance	R_{14-16}	typ. 2 $k\Omega$

1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.

2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example $R_S = 56 \Omega$, $S_{\varphi} = 5 V/\mu s$ and $R_S = 0$, $S_{\varphi} = \geq 25 V/\mu s$.

4) In addition to this figure $\pm 7\%$ of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0 .

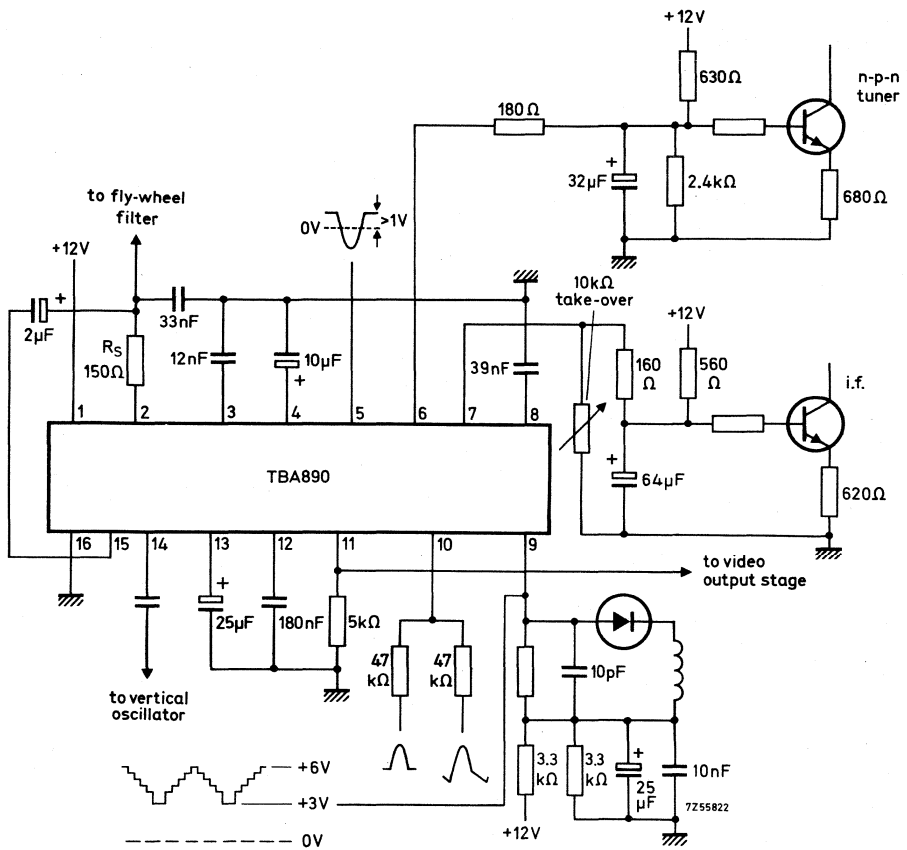
This value of $\pm 7\%$ is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed $\pm 10\%$.

5) Nominal voltage 6 V.

The load impedance on pin 2 of the circuit on page 7 is about 50 $k\Omega$.

When a higher impedance is used (tube equipped reactance stage) values from 2 V to 10 V can be reached.

APPLICATION INFORMATION



TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA900 is a silicon monolithic integrated signal processing circuit for mono-chrome and colour television receivers.

It combines the following functions:

- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator.
- automatic horizontal phase detector
- vertical sync pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.

The control stage in the i.f. amplifier has to be equipped with an n-p-n transistor and the tuner with a p-n-p transistor.

The circuit is developed for signals with negative modulation.

QUICK REFERENCE DATA

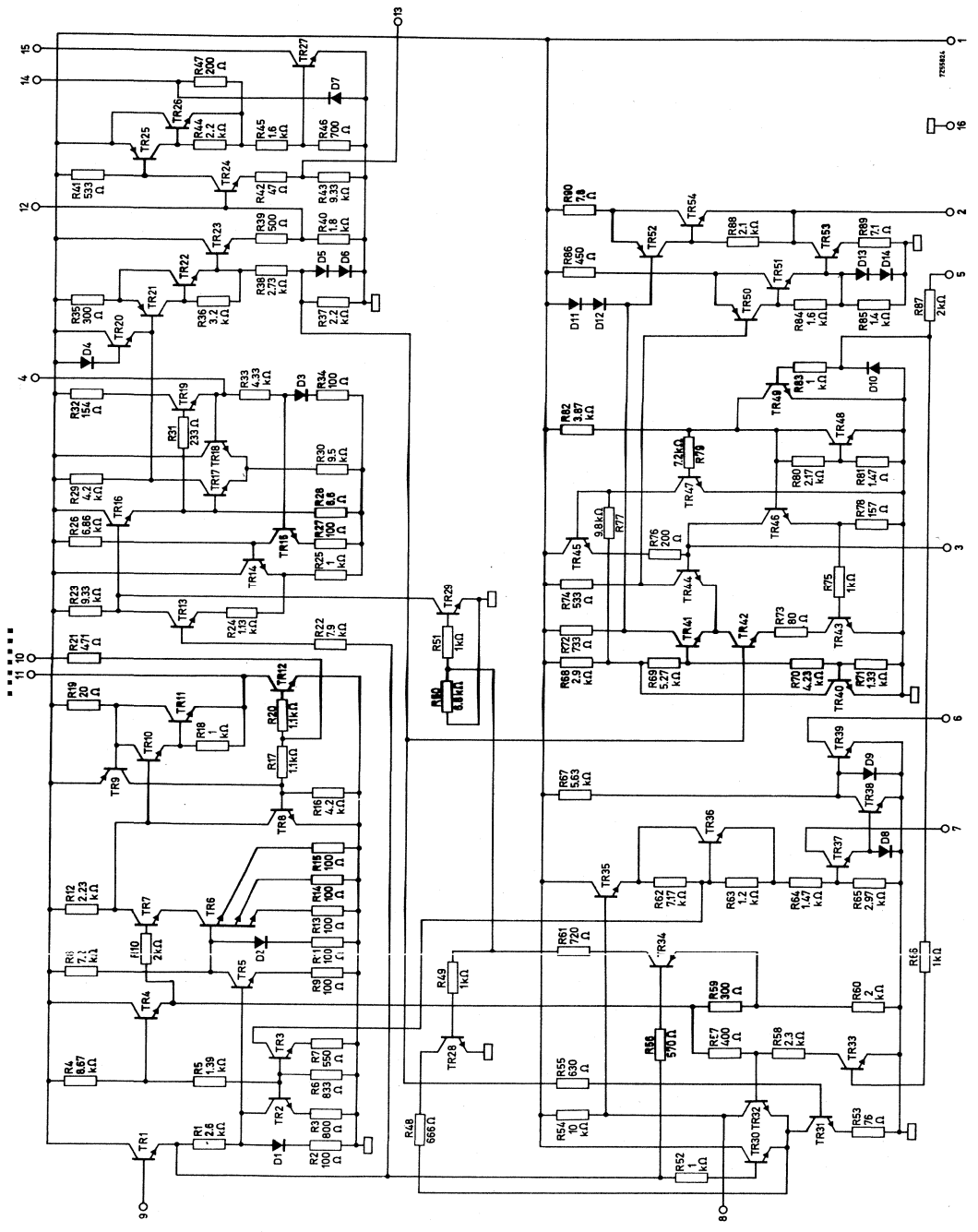
Supply voltage	V_p	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	°C
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7	V
Voltage gain of the video amplifier	G_v	typ.	7	dB
A.G.C. voltage for i.f. part	V_{7-16}		1,0 to 12	V
A.G.C. voltage for tuner	V_{6-16}		0,3 to 12	V
Output voltage range horizontal phase detector	V_{2-16}		2 to 10	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{14-16(p-p)}$	typ.	11	V

PACKAGE OUTLINES (see general section)

TBA900 : 16-lead DIL; plastic.

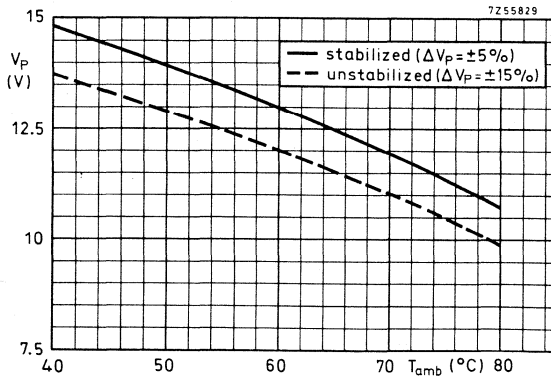
TBA900Q: 16-lead QIL; plastic.

TBA900 TBA900Q



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

<u>Supply voltage</u>	V_P	max.	20	$V^1)$
<u>Power dissipation</u>	P_{tot}	max.	700	mW
<u>Temperatures</u>				
Storage temperature	T_{stg}	-55 to	+125	$^{\circ}C$
Operating ambient temperature	T_{amb}	-25 to	+80	$^{\circ}C$



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

¹⁾ Allowed only while receiver is warming up.

CHARACTERISTICS

Supply voltage range

V_P

See curves on page 3

The following characteristics are measured in the circuit on p. 7 at $T_{amb} = 25\text{ }^\circ\text{C}$;
 $V_P = 12\text{ V}$.

Video amplifier

Input resistance	R_{9-16}	>	30	$k\Omega$
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity (m)		>	0.9	
Rise time and fall time at the output	$t_r; t_f$	<	50	ns
Voltage gain	G_V	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	$V^1)$
D.C. bias video detector voltage	V_{bias}	typ.	6	$V^2)$
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	$V^1)$
Black level at the output	V_{11-16}	typ.	5	$V^3)$
Available video output current (peak value)	I_{11M}	\leq	30	$mA^4)$

Tolerances on the video output voltages

I. C. processing spreads	$\pm\Delta V_{11-16}$	<	420	$mV^5)$
Temperature drift	$-\Delta V_{11-16}$	typ.	1.8	$mV/^\circ\text{C}$
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	100	$mV^6)$
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.5	

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C.C.I.R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15\text{ mA}$.

5) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure.

6) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output

I. C. processing spreads	$\pm\Delta V_{11-16}$	<	420	mV ¹⁾
Temperature drift	$-\Delta V_{11-16}$	typ.	1.7	mV/°C
Spreads over a. g. c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	130	mV ²⁾
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.4	

Video blanking

Input voltage (peak-to-peak value)	$V_{10-16(p-p)}$		1 to 5	V
Input resistance	R_{10-16}	typ.	1	k Ω
Output voltage during blanking	V_{11-16}	<	500	mV

A. G. C. circuit

Range of control voltage i. f. amplifier	V_{7-16}		1 to 12	V ³⁾
Range of control voltage tuner	V_{6-16}		0.3 to 12	V ⁴⁾
Signal expansion for full control of i. f. amplifier and tuner		typ.	0.5	dB
Current i. f. control point	I_7	<	20	mA
Current tuner control point	I_6	<	8	mA
Current i. f. control point for tuner take-over	I_7	typ.	2	mA
Keying input pulse (peak-to-peak value)	$V_{5-16(p-p)}$		see note 5	
Input resistance	R_{5-16}	typ.	2	k Ω

1) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure (pin 9).

2) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) Negative going at increasing input signal.

5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit

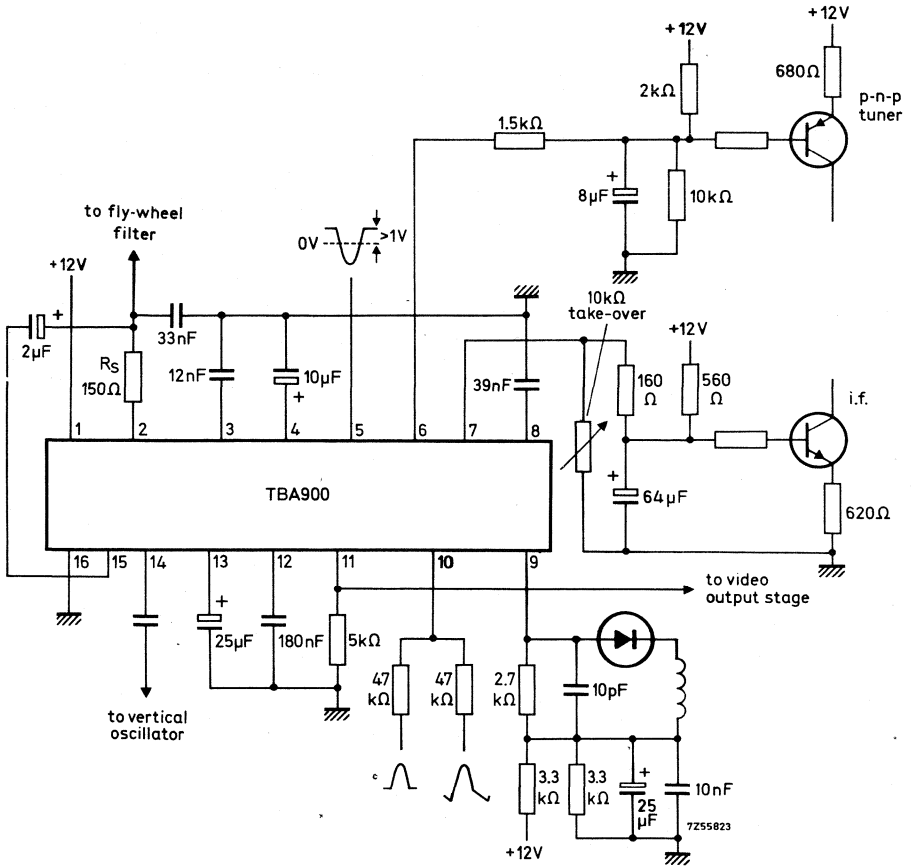
Sync. separator		see note 1
Output voltage range of phase detector	V_{2-16}	2 to 10 $V^2)$
Control steepness	S_ϕ	typ. 2.5 $V/\mu s^3)$
Phase deviation between front edge sync. pulse and front edge flyback pulse	ϕ_0	typ. 1.5 μs
Variation ϕ_0 caused by internal spreads	$\pm\Delta\phi_0$	typ. 0.3 $\mu s^4)$
Output voltage range as a frequency detector	V_{2-16}	4 to 8 $V^5)$

Vertical synchronization circuit

Output voltage vertical sync. pulse generator	V_{14-16}	typ. 11 V
Output impedance	R_{14-16}	typ. 2 $k\Omega$

- 1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.
- 2) Nominal voltage 6 V.
- 3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example $R_S = 56 \Omega$, $S_\phi = 5 V/\mu s$ and $R_S = 0$, $S_\phi = \geq 25 V/\mu s$.
- 4) In addition to this figure $\pm 7\%$ of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of ϕ_0 .
This value of $\pm 7\%$ is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed $\pm 10\%$.
- 5) Nominal voltage 6 V.
The load impedance on pin 2 of the circuit on page 7 is about 50 $k\Omega$.
When a higher impedance is used (tube equipped reactance stage) values from 2V to 10 V can be reached.

APPLICATION INFORMATION



HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor -thyristor -or tube equipped output stages.

It combines the following functions:

- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loopgain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

QUICK REFERENCE DATA

Supply voltage	V_{1-16}	nom.	12	V
Ambient temperature	T_{amb}		25	°C

<u>Input signals</u>				
Video input voltage (positive-going sync) top sync to white value	$V_{8-16(p-p)}$	typ.	3	V
			1 to 7	V
Noise gate input current (peak value)	I_{9M}	>	30	μA
Input resistance of noise gate	R_{9-16}	typ.	200	Ω
Flyback signal input voltage (peak value)	V_{5-16M}	typ.	±1	V
Flyback signal input current (peak value)	I_{5M}	typ.	1	mA
<u>Output signals</u>				
Line driver output voltage (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	10	V
Line driver output current (average value)	$I_{2(AV)}$	max.	20	mA
Line driver output current (peak value)	I_{2M}	max.	200	mA
Composite sync output voltage (peak value)	V_{7-16M}	typ.	10	V

PACKAGE OUTLINES (see general section)

TBA920 : 16-lead D1L; plastic.

TBA920Q: 16-lead Q1L; plastic.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Supply voltage	V_{1-16}	max.	13,2	V
Pin No. 3 voltage	V_{3-16}		0 to 13,2	V
Pin No. 8 voltage	$-V_{8-16}$	max.	12	V
Pin No. 10 voltage	V_{10-16}		-0,5 to +5	V

Currents

Pin No. 2 current (average value)	$I_{2(AV)}$	max.	20	mA
	I_{2M}	max.	200	mA
Pin.No. 5 current (peak value)	I_{5M}	max.	10	mA
Pin.No. 7 current (peak value)	I_{7M}	max.	10	mA
Pin No. 8 current (peak value)	I_{8M}	max.	10	mA
Pin No. 9 current (peak value)	I_{9M}	max.	10	mA

Power dissipation

Total power dissipation	P_{tot}	max.	600	mW ¹⁾
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Temperatures

Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		-20 to +60	°C

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C

Measured in circuit on page 6 (CCIR standard).

<u>Current consumption</u> at $I_2 = 0$	I_1	typ.	36	mA
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Required input signals

Video signal

Input voltage (positive going sync) peak-to-peak value	$V_{i(p-p)}$	typ.	3	V
			1 to 7	V
Input current during sync pulse (peak value)	I_{8M}	typ.	100	µA

Noise gating (pin 9)

Input voltage (peak value)	V_{9-16M}	>	0,7	V
Input current (peak value)	I_{9M}	>	30	µA
		<	10	mA
Input resistance	R_{9-16}	typ.	200	Ω

¹⁾ 800 mW permissible while tubes are heating up.

CHARACTERISTICS (continued)

Flyback pulse (pin 5)

Input voltage (peak value)	V _{5-16M}	typ.	±1 V
Input current (peak value)	I _{5M}	> typ.	50 μA 1 mA
Input resistance	R ₅₋₁₆	typ.	400 Ω
Pulse duration at 15625 Hz	t ₅	>	10 μs

Delivered output signals

Composite sync pulses (positive; pin 7)

Output voltage (peak-to-peak value)	V _{7-16(p-p)}	typ.	10 V
Output resistance			
at leading edge of pulse (emitter follower)	R ₇₋₁₆	≈	50 Ω
at trailing edge	R ₇₋₁₆	typ.	2, 2 kΩ
Additional external load resistance	R _{7-16(ext)}	>	2 kΩ

Driver pulse (pin 2)

Output voltage (peak-to-peak value)	V _{2-16(p-p)}	typ.	10 V
Average output current	I _{2(AV)}	<	20 mA
Peak output current	I _{2M}	<	200 mA
Output resistance (low ohmic)	R ₂₋₁₆	typ. 2,5 or 15	Ω ¹⁾
Output pulse duration when synchronised	t ₂	12 to 32	μs ²⁾
Permissible delay between leading edge of output pulse and flyback pulse at t ₅ = 12 μs	t _{0 tot}	0 to 15	μs
Supply voltage at which output pulses are obtained	V ₁₋₁₆	>	4 V

¹⁾ Depends on switch position and polarity output current. R₂₋₁₆ = 2,5 Ω is valid for V₂₋₁₆ = +10, 5 V and a load between pins 2 and 16 (e. g. an external resistor).

²⁾ The output pulse duration is adjusted by shifting the leading edge (V₃₋₁₆ from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.

For a line output stage with a BU108 high voltage transistor the resulting duration is about 22 μs, and in such a way that the line output transistor is switched on again about 8 μs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

CHARACTERISTICS (continued)

Oscillator

Frequency; free running ($R_{15-16} = 3,3 \text{ k}\Omega$)	f_o		15 625	Hz	1)
Spread of frequency at nominal values of peripheral components	$\frac{\Delta f_o}{f_o}$	<	± 5	%	2)
Frequency change when decreasing the supply down to minimum 4 V	$\left \frac{\Delta f_o}{f_o} \right $	<	10	%	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$	typ.	16,5	Hz/ μA	
Adjustment range of network in circuit on page 6	$\frac{\Delta f_o}{f_o}$	typ.	± 10	%	
Influence of supply voltage on frequency at $V_P = 12 \text{ V}$	$\frac{\delta f_o}{f_o} / \frac{\delta V_P}{V_{Pnom}}$	<	5	%	

Control loop 1 (between sync pulse and oscillator)

Control voltage range	V_{12-16}		0,8 to 5,5	V	
Control current (peak values)					
at $V_{10-16} > 4,5 \text{ V}$; $V_{6-16} > 1,5 \text{ V}$	I_{12M}	typ.	± 2	mA	
at $V_{10-16} < 2 \text{ V}$; $V_{6-16} > 1,5 \text{ V}$	I_{12M}	typ.	± 6	mA	
Loopgain of APC system					
a. Time coincidence between sync pulse and flyback pulse or $V_{10-16} > 4,5 \text{ V}$	$\frac{\Delta f}{\Delta t}$	typ.	1	kHz/ μs	
b. No time coincidence or $V_{10-16} < 2 \text{ V}$	$\frac{\Delta f}{\Delta t}$	typ.	3	kHz/ μs	
Catching and holding range	Δf	typ.	± 1	kHz	3)

1) The oscillator frequency can be changed for other t.v. standards by an appropriate value of C_{14-16} .

2) Exclusive external components tolerances.

3) Adjustable with R_{12-15} .

CHARACTERISTICS (continued)

Pull-in time for $\Delta f/f_0 = \pm 3\%$ ($\Delta f = 470$ Hz)	t	≈	20	ms	1)
Switch-over from large control sensitivity to small control sensitivity after catching	t	≈	20	ms	1)

Control loop II (between flyback pulse and oscillator)

Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	t _{d tot}		0 to 15	μs	
Static control error	$\frac{\Delta t}{\Delta t_d}$	<	0,5	%	2)
Output current during flyback pulse (peak value)	I _{4M}	typ.	±0,7	mA	

Overall phase relation

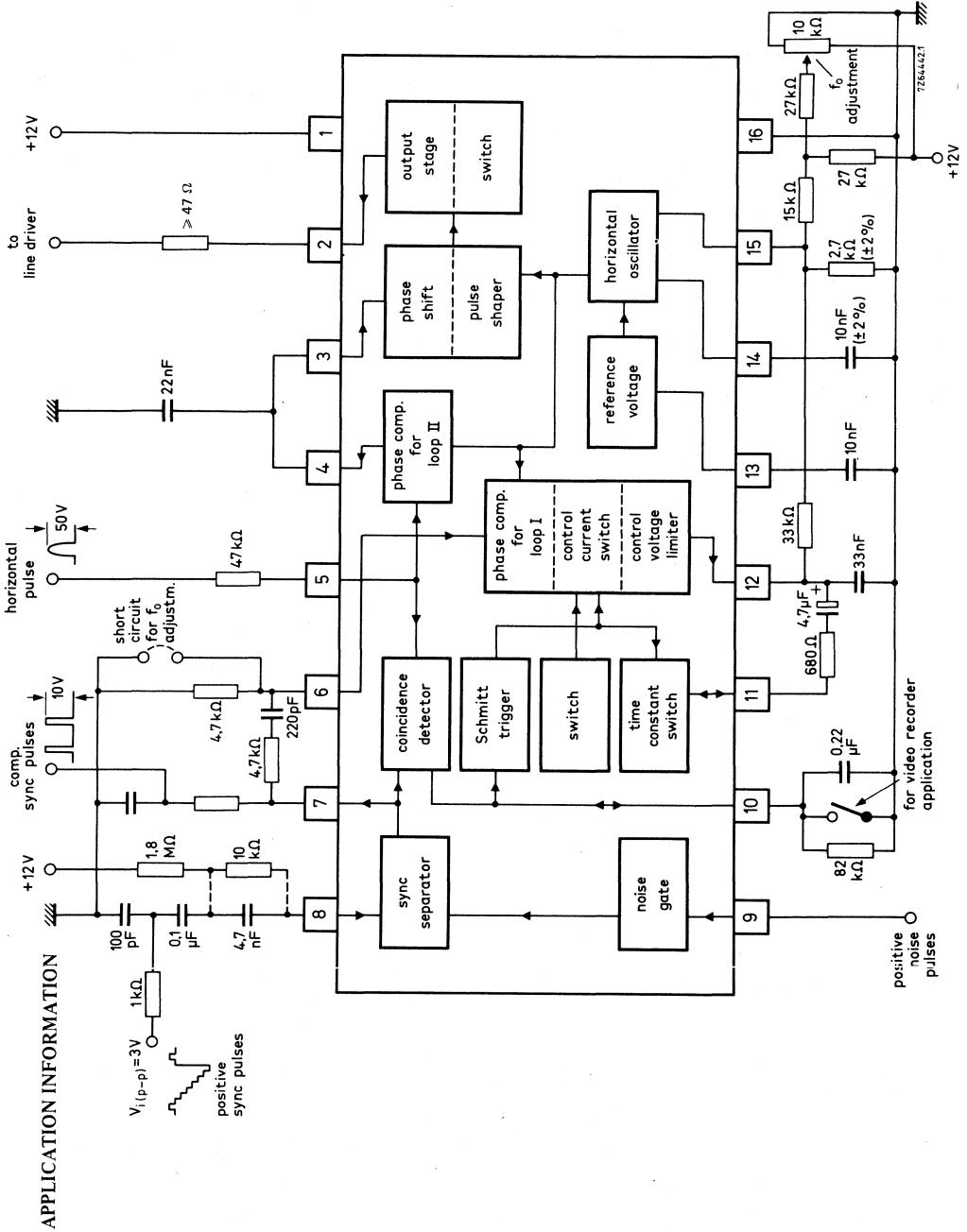
Phase relation between leading edge of sync pulse and middle of flyback pulse	t	typ.	4,9	μs	3)
Tolerance of phase relation	Δt	<	1	μs	4)
Voltage for T ₂ = 12 to 32 μs	V ₃₋₁₆		6 to 8	V	
Adjustment sensitivity	$\frac{\Delta T_2}{\Delta V_{3-16}}$	typ.	10	μs/V	
Input current	I ₃	<	2	μA	

External switch-over of parameters (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.

Required switch-over voltage					
at R ₁₁₋₁₆ = 150 Ω	V ₁₀₋₁₆	>	4,5	V	
at R ₁₁₋₁₆ = 2 kΩ	V ₁₀₋₁₆	<	2	V	
Required switch-over current					
at R ₁₁₋₁₆ = 150 Ω; V ₁₀₋₁₆ = 4,5 V	I ₁₀	typ.	80	μA	5)
at R ₁₁₋₁₆ = 2 kΩ; V ₁₀₋₁₆ = 2 V	I ₁₀	typ.	120	μA	

- 1) See application information circuit on page 6.
- 2) The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
- 3) This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at C₅₋₁₆ = 560 pF.
- 4) The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d. c. voltage to pin 3.
- 5) With sync pulses at pin 7 and 8; without RC network at pin 10.

TBA920 TBA920Q



HORIZONTAL COMBINATION

The TBA920S is identical to the TBA920, except for the following data :

Oscillator

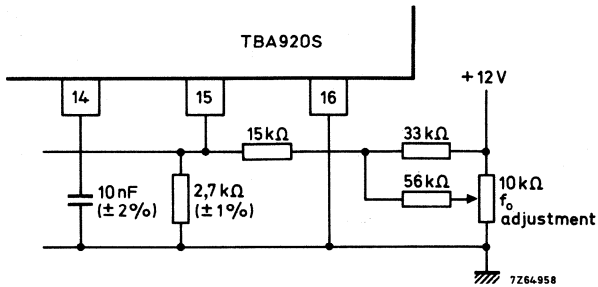
Spread of frequency at

$$R_{15-16} = 3,3 \text{ k}\Omega; C_{14-16} = 10 \text{ nF}$$

$$\frac{\Delta f_0}{f_0} < 1,5 \%$$

Adjustment range of frequency
(in network below)

$$\frac{\Delta f_0}{f_0} \text{ typ. } \pm 5 \%$$



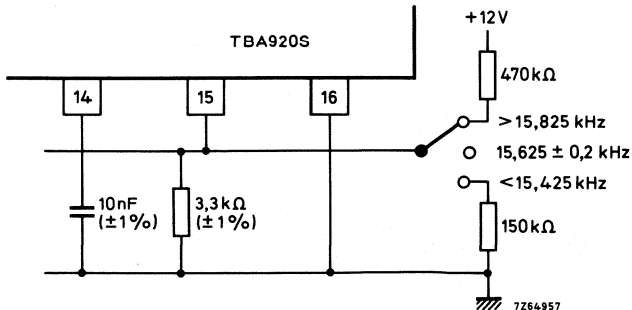
Note: The above network is the only part that differs from the circuit given on page 6 of TBA920 data.

Overall phase relation

Tolerance of phase relation between
leading edge of sync pulse and
middle of flyback pulse

$$|\Delta t| < 0,4 \mu\text{s}$$

Other circuit possibilities for oscillator frequency adjustment



COLOUR DEMODULATOR

The TBA990 is an integrated colour demodulator circuit for colour television receivers incorporating two active synchronous demodulators for the R-Y and B-Y chrominance signals, a matrix (producing the G-Y colour difference signal), PAL phase switch and flip-flop. It is suitable for d. c. -coupled drive to the picture tube when associated with the matrix integrated circuit (TBA530) and RGB output stages.

Special attention has been given in the design to minimising d. c. level drift with temperature.

QUICK REFERENCE DATA

Supply voltage (stabilised)	V ₆₋₁₆	nom.	12 V
Supply current	I ₆	nom.	17 mA
Gain of R-Y demodulator	G ₁₃₋₄	typ.	3, 8
Gain of B-Y demodulator	G ₁₀₋₇	typ.	6, 7
Impedance of chrominance inputs	$\left. \begin{array}{l} Z_{13-16} \\ Z_{10-16} \end{array} \right\}$	>	800 Ω in parallel with 10 pF
Impedance of colour-difference signal outputs	Z ₄₋₁₆	typ.	3 k Ω
	Z ₅₋₁₆	typ.	3 k Ω
	Z ₇₋₁₆	typ.	3 k Ω

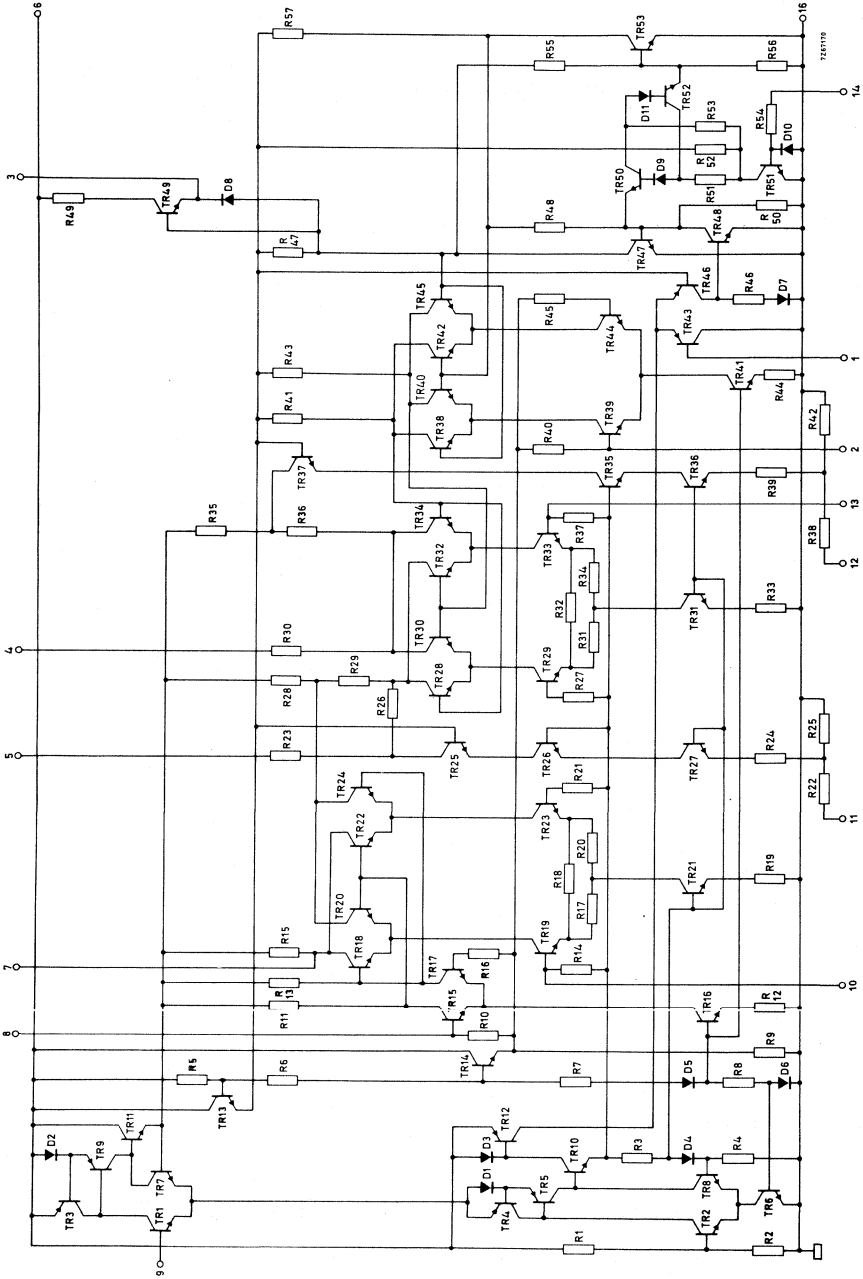
PACKAGE OUTLINES (see general section)

TBA990 : 16-lead DIL; plastic.

TBA990Q: 16-lead QIL; plastic.

TBA990
TBA990Q

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

<u>Supply voltage</u>	V ₆₋₁₆	max.	13,2 V
<u>Total power dissipation</u>	P _{tot}	max.	300 mW

Temperatures

Storage temperature	T _{stg}	-55 to +125 °C
Operating ambient temperature	T _{amb}	-20 to +60 °C

CHARACTERISTICS at V₆₋₁₆ = 12 V (stabilised); T_{amb} = 25 °C

Gain of chrominance (R-Y) signal

V _{i(p-p)} = 50 mV; f = 4,4 MHz (see note 1)	G ₁₃₋₄	typ.	3,8
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Ratio of gain of blue channel to

red channel defined at equal chroma signal inputs (see also pin 4 on page 6)	$\frac{G_{10-7}}{G_{13-4}}$	typ.	1,78
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Matrix for generation G-Y signal

-0,51 (R-Y) -0,19 (B-Y)

Colour difference d.c. output voltage (see note 2)

V ₄₋₁₆	typ.	7,5 V
V ₇₋₁₆	typ.	7,5 V
V ₅₋₁₆	typ.	7,5 V

Drift d.c. output voltage

$\Delta T_{amb} = 40 \text{ °C}; V_{11-16} = V_{12-16} = 6 \text{ V}$	<	±50 mV
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Relative change of d.c. output voltages

between channels at $\Delta T_{amb} = 40 \text{ °C}$	<	20 mV
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Colour difference output signals

peak-to-peak values (see note 3): R-Y	V _{4-16(p-p)}	>	1,6 V
B-Y	V _{7-16(p-p)}	>	2,0 V
G-Y	V _{5-16(p-p)}	>	0,9 V

Impedance of chrominance inputs

V _{i(rms)} = 20 mV (sinusoidal); f = 4,4 MHz	$\left. \begin{array}{l} Z_{10-16} \\ Z_{13-16} \end{array} \right\}$	>	800 Ω in paral- lel with 10 pF
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Impedance of reference signal inputs

Z ₂₋₁₆	typ.	5 kΩ
Z ₈₋₁₆	typ.	5 kΩ

Impedance of colour-difference signal outputs

Z ₄₋₁₆	typ.	3 kΩ
Z ₅₋₁₆	typ.	3 kΩ
Z ₇₋₁₆	typ.	3 kΩ

1. Ratio of peak-to-peak values of input and output signals.
2. These can be adjusted, by the potentiometers shown in circuit on page 5, by ±0,2 V to compensate for spreads in the matrix and output circuitry.
3. Linearity ≥ 0,7 measured in the circuit on page 5.

CHARACTERISTICS (continued)

Square wave output voltage

peak-to-peak value; $f = 7, 8 \text{ kHz}$

$V_{3-16(p-p)}$ typ. 3,5 V

Input voltages

Reference voltages (peak-to-peak)

at reference R-Y

$V_{2-16(p-p)}$ typ. 1 V

at reference B-Y

$V_{8-16(p-p)}$ typ. 1 V

Identification circuit

line pulse input (triggers on negative going edge)

$V_{14-16(p-p)}$ 2 to 5 V

Identification signal

required voltage for "ident on"

$V_{1-16} > 6,5 \text{ V}$

required voltage for "ident off"

$V_{1-16} < 5,5 \text{ V}$

required current for "ident on"

$-I_1 < 0,1 \text{ mA}$

Input current

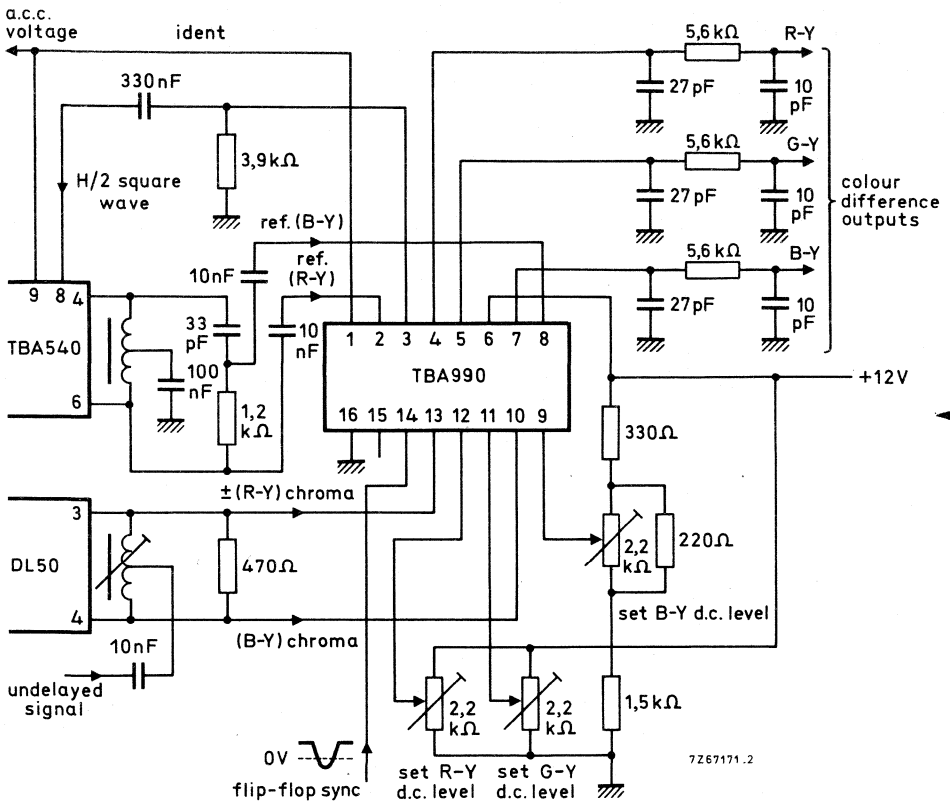
Supply current consumption

I_6 typ. 17 mA

PINNING

- | | |
|--|--|
| 1. Identification bias | 9. B-Y d.c. level setting |
| 2. R-Y sub-carrier reference input | 10. B-Y chrominance input signal |
| 3. P. A. L. square wave output (7,8 kHz) | 11. G-Y d.c. level setting |
| 4. R-Y signal output | 12. R-Y d.c. level setting |
| 5. G-Y signal output | 13. R-Y chrominance input signal |
| 6. Supply voltage (12 V) | 14. Line pulse input (flip-flop syn -
chronising) |
| 7. B-Y signal output | 15. n.c. |
| 8. B-Y sub-carrier reference input | 16. Earth (negative supply) |

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number (see also page 5).

1. Identification bias

The P. A. L. flip-flop is stopped, for identification purposes, when the voltage on pin 1 increases above 6 V. This threshold is internally generated and has a proportional behaviour with the 12 V supply voltage. The threshold level of 6 V is chosen to match the output characteristic of the TBA540 and has a sufficiently high safety margin above the zero chroma signal level of 4 V to eliminate spurious identifying.

2. R-Y subcarrier reference input

A 1 V peak-to-peak signal is required via a d. c. blocking capacitor. Under no circumstances should this signal be less than 0,5 V peak-to-peak. The input resistance at this pin is typically 5 k Ω .

3. P. A. L. Square wave circuit

The amplitude is 3,5 V peak-to-peak from an emitter follower.

4. R-Y signal output (G-Y at pin 5 and B-Y at pin 7)

These outputs require no external d. c. loads except that direct connection must be made via the low pass filter to the appropriate pins on the R.G.B. matrix TBA530.

The signals produced are in the following ratios:

$$\begin{aligned} V_{B-Y} &= 1,78 V_{R-Y} \pm 10 \% \\ \text{(a) } V_{G-Y} &= 0,85 V_{R-Y} \pm 10 \% \\ \text{(b) } V_{G-Y} &= 0,17 V_{R-Y} \pm 10 \% \end{aligned}$$

Condition (a) refers to (B-Y) + (R-Y) addition in the G-Y matrix.

Condition (b) refers to the phase reversed (R-Y) input signal where (G-Y) is obtained by subtraction.

The d. c. levels should each be adjusted, starting with the (B-Y), to +7,5 V at nominal supply voltage. However, in a complete circuit using the TBA530 matrix and feedback integrated circuit these d. c. levels will be adjusted to give the correct setting of the picture tube drive black levels.

The changes in d. c. level with supply voltage are approximately linear and track together.

The unwanted products of demodulation occurring in the colour difference outputs are chiefly 8,86 MHz and harmonics together with a small amount of 4,43 MHz due to possible unbalance in the demodulators. To avoid possible troubles in the receiver because of the radiation of these demodulation products from the R. G. B. drive circuits, filters must be employed in each of the colour-difference outputs from the TBA990. The roll-off should begin at about 1,5 MHz and attention should be given to the parallel resonance of the inductors to ensure that no serious attenuation will occur at less than 1,5 MHz. Also, some advantage may be secured by designing the inductor so that the dip due to its self-resonance occurs at about 4,43 MHz.

APPLICATION INFORMATION

5. G-Y signal output (see pin 4)

6. Positive supply

The maximum allowable voltage on this pin is 13, 2 V.

7. B-Y signal output (see pin 4)

8. B-Y subcarrier reference input

The requirements here are identical with those for pin 2.

9. D.C. level setting for B-Y output signal (see circuit diagram on page 5, and also pin 7)

10. Chrominance B-Y input signal

An input signal of approximately 360 mV peak-to-peak (colour bars) is required at this pin. The input impedance is greater than 800 Ω and the input capacitance is less than 10 pF. The spread in gain of the internal circuitry in the chrominance channel is $\pm 10\%$.

11. D.C. level setting for G-Y output signal (see circuit diagram on page 5, and also pin 5)

12. D.C. level setting for R-Y output signal (see circuit diagram on page 5, and also pin 4)

13. Chrominance R-Y input signal

An input signal of approximately 500 mV peak-to-peak (colour bars) is required at this pin. The input impedance and spread in gain is the same as for pin 9.

14. Line pulse input (flip-flop synchronising)

A waveform derived from the line timebase can be used for synchronising providing that its amplitude lies between 2 V and 5 V peak-to-peak. The trigger point occurs where the negative going edge crosses approximately +0, 6 V.

15. Not connected

This pin should not be used for external connections.

16. Negative supply (earth)

TELEVISION SIGNAL PROCESSING CIRCUIT

The TCA270S is a monolithic integrated circuit combining the following functions:

- synchronous demodulator
- video amplifier with buffer output stages
- noise inverters
- A. G. C. detector with output stages for n-p-n tuner and i. f. amplifier
- A. F. C. demodulator with buffer output stage

Opposite polarity video signals are available from emitter followers, the negative-going signal being matched to integrated circuit type TBA920.

QUICK REFERENCE DATA

Supply voltage	V_{3-16}	nom.	12	V
Ambient temperature	T_{amb}	typ.	25	°C

Frequency	f	typ.	38,9	MHz
Supply current	I_3	typ.	47	mA
Video output voltage (peak value)	V_{9-16M}	typ.	3	V
Bandwidth (3 dB)	B	typ.	5	MHz
Intermodulation products (blue colour bar)				
1, 1 MHz with respect to B-W level		typ.	-60	dB
3, 3 MHz with respect to B-W level		typ.	-67	dB
A. F. C. output control voltage swing (peak-to-peak value)	$V_{11-16(p-p)}$	>	10	V
A. G. C. control current for n-p-n i. f. (pin 4)	I_4	>	10	mA
A. G. C. control current for tuner (pin 5)	I_5	>	10	mA

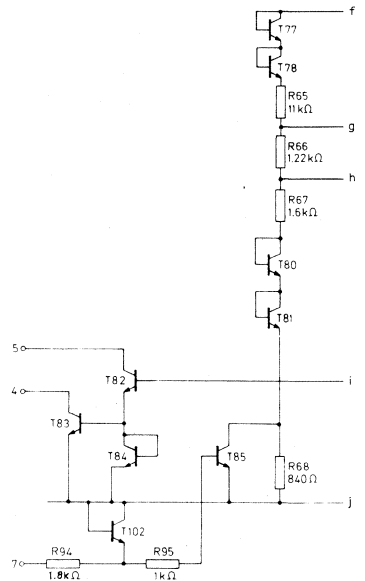
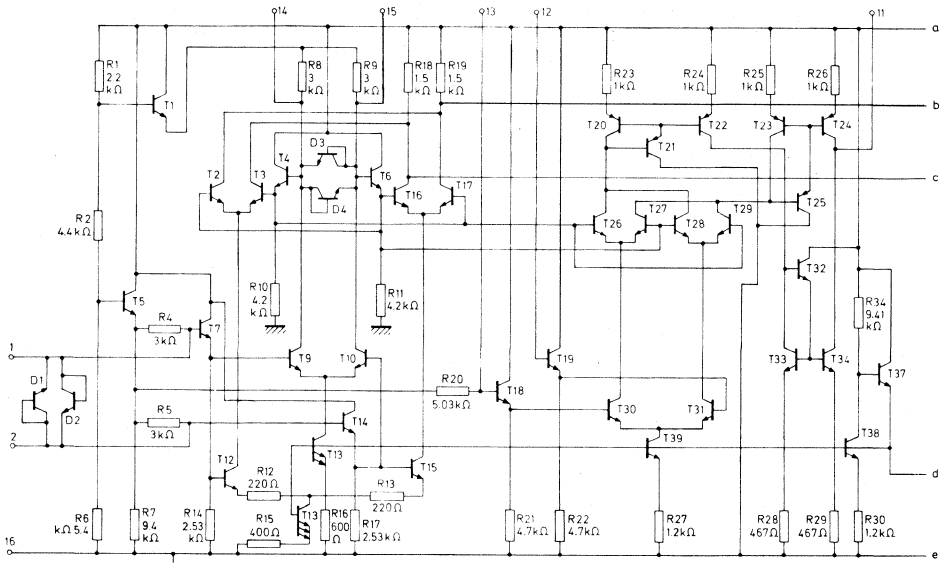
PACKAGE OUTLINES (see general section)

TCA270S : 16-lead DIL; plastic.

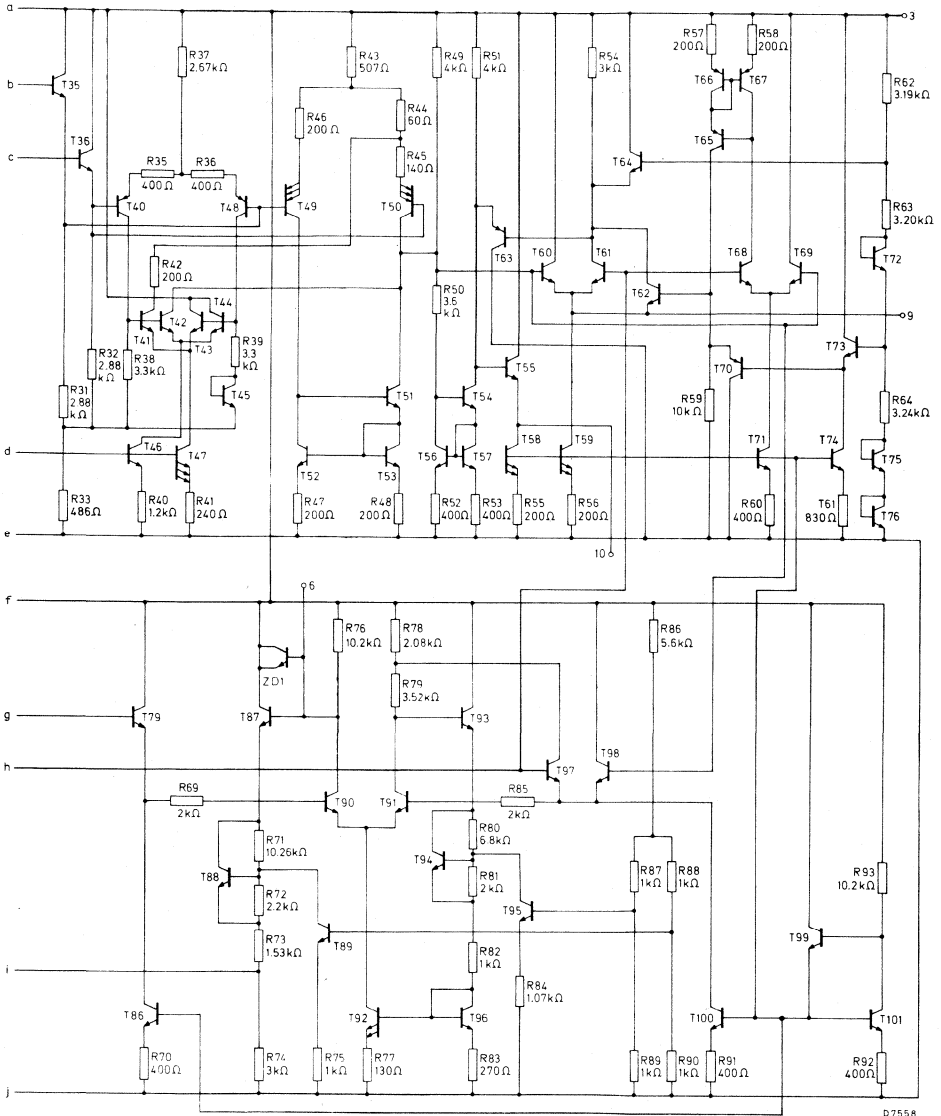
TCA270SQ: 16-lead QIL; plastic.

TCA270S TCA270SQ

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



07558

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

<u>Supply voltage</u> during switch on ($t \leq 10$ s)	V_{3-16}	max.	18	V
<u>Power dissipation</u>	P_{tot}	max.	1	W
<u>Temperatures</u>				
Storage temperature	T_{stg}		-55 to +125	$^{\circ}\text{C}$
Operating ambient temperature	T_{amb}		-25 to +55	$^{\circ}\text{C}$

CHARACTERISTICS

Supply voltage range	V_{3-16}	typ.	12,0	V
			10, 2 to 13, 8	V
Supply current range	I_3	typ.	47	mA
			33 to 62	mA
D.C. output voltage (zero signal; pin 9)	V_{9-16}	typ.	6	V
D.C. output voltage (zero signal; pin 10)	V_{10-16}	typ.	6	V
D.C. output voltage at start of a.g.c. (pin 9)	V_{9-16}	typ.	3	V
Unbalanced r. m. s. input voltage for a. g. c.	$V_{i(rms)}$	typ.	70	mV
			50 to 100	mV
Input resistance at pin 1	R_{1-16}	typ.	3	$k\Omega$
Input resistance at pin 2	R_{2-16}	typ.	3	$k\Omega$
Bandwidth (3 dB) of video output	B	typ.	5	MHz
Differential gain		<	10	% 1)
Differential phase		<	10	$^{\circ}$ 1)
Intermodulation products (blue colour bar)				
1, 1 MHz		typ.	-60	dB
3, 3 MHz		typ.	-67	dB
Carrier frequency rejection at pins 9, 10 and 11		>	40	dB
Twice carrier frequency rejection at pins 9, 10 and 11		>	40	dB

1) CCIR system of modulation, peak of white signal = 10% of carrier.

CHARACTERISTICS (continued)

A. G. C. circuit

Saturation voltage of tuner control at 10 mA (pin 4)	$V_{4-13sat}$	<	0,3	V
Saturation voltage of i. f. control at 10 mA (pin 5)	$V_{5-13sat}$		0,7 to 1,2	V
Breakdown voltage at 1 mA (pins 4 and 5)	$V_{(BR)4-13}$ $V_{(BR)5-13}$	>	14	V
Control current at pins 4 and 5	$I_4; I_5$	>	10	mA
Signal expansion for complete a. g. c.		<	0,5	dB
A. G. C. gating (optional) by negative line flyback pulse; input voltage (peak-to-peak value)	$V_{i(p-p)}$	>	2	V
		<	supply voltage	
input resistance	R_i	typ.	1,8	k Ω
Current ratio of unsaturated outputs (pins 4 and 5) at $I_5 = 1$ mA	$\frac{I_4}{I_5}$	>	6	

A. F. C. circuit

Output control voltage swing (peak-to-peak value)	$V_{11-16(p-p)}$	>	10	V
Change of frequency for complete output voltage swing		<	400	kHz
Change of frequency to maintain peak output voltage		>	± 1	MHz

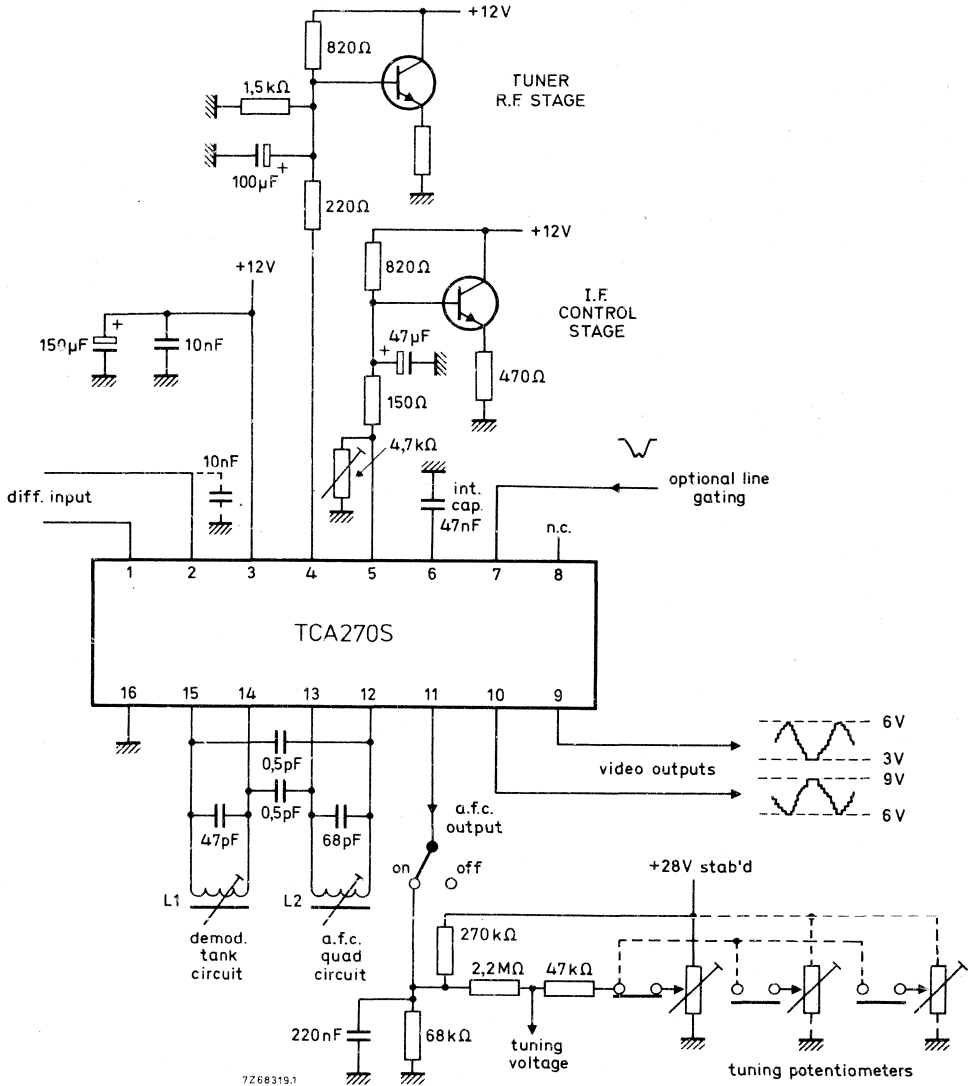
Noise inverters ¹⁾

Negative-going noise pulses in pin 9 inversion threshold		typ.	2,55	V
Positive-going noise pulses in pin 9 inversion threshold		typ.	6,6	V

¹⁾ Noise pulses are inverted to a point near black level.

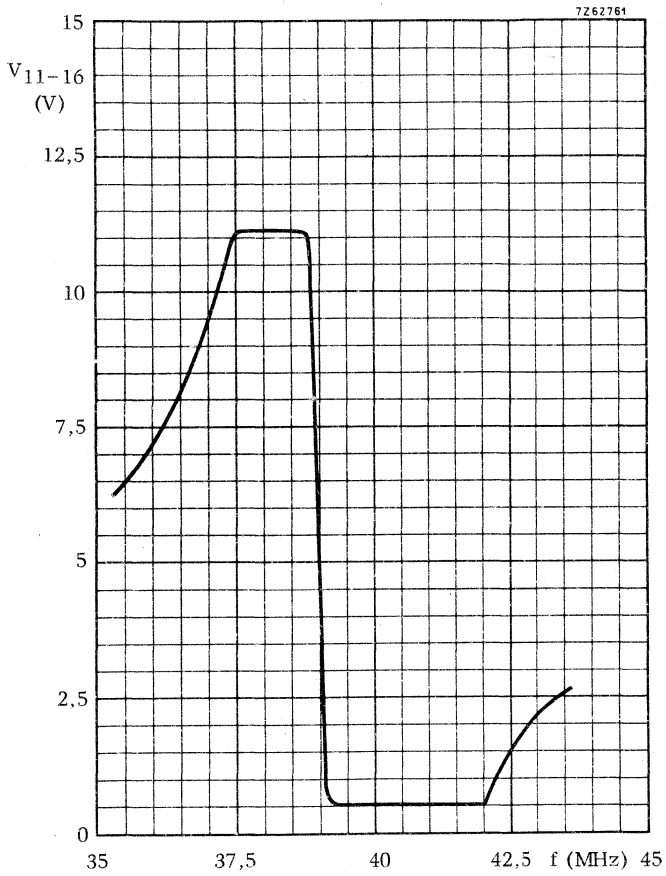
TCA270S TCA270SQ

APPLICATION INFORMATION



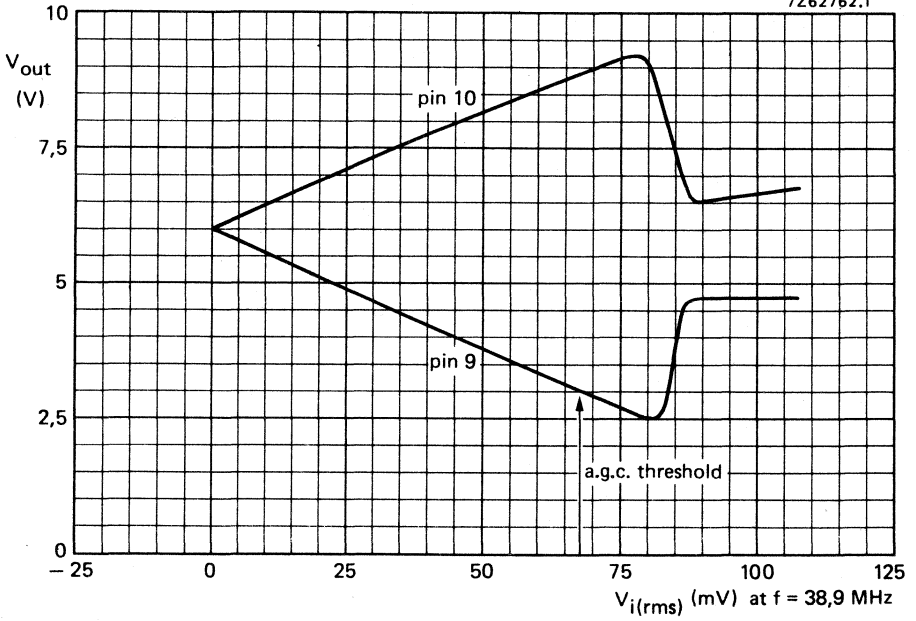
7268319.1

Unloaded Q of L1 and L2 must be > 50.



A.F.C. output voltage versus frequency

7Z62762.1



SYNCHRONOUS DEMODULATOR FOR TV RECEIVERS

The TCA540 is a silicon monolithic integrated synchronous demodulator for television receivers which combines the following functions:

- synchronous demodulator with passive regeneration of the reference carrier
- white spot inverter (inverts white spots, which can occur because of the principle of synchronous demodulation).
- video preamplifier
- a.f.c. circuit

QUICK REFERENCE DATA

Supply voltage	V_{11-14}	nom.	12	V
Supply current	I_{11}	typ.	40	mA

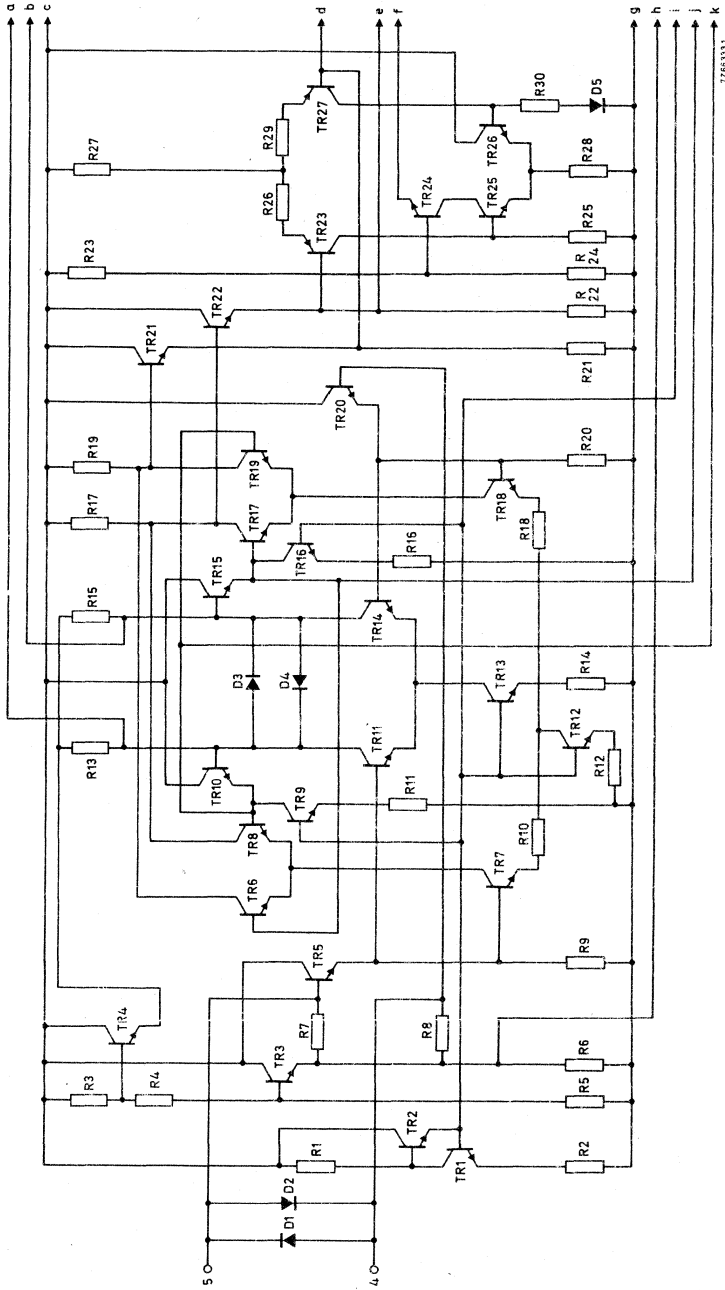
Input voltage (r. m. s. value) for 3 V peak-to-peak output voltage	$V_{4-5(\text{rms})}$	typ.	70	mV
Differential gain (at pin 8)	dG	typ.	2	%
Differential phase (at pin 8)	$d\phi$	typ.	2°	
A. F. C. output voltage	V_{3-14}		1 to 11	V
A. F. C. sensitivity per kHz ($R_L = 50 \text{ k}\Omega$)	V_{3-14}	typ.	40	mV

PACKAGE OUTLINES (see general section)

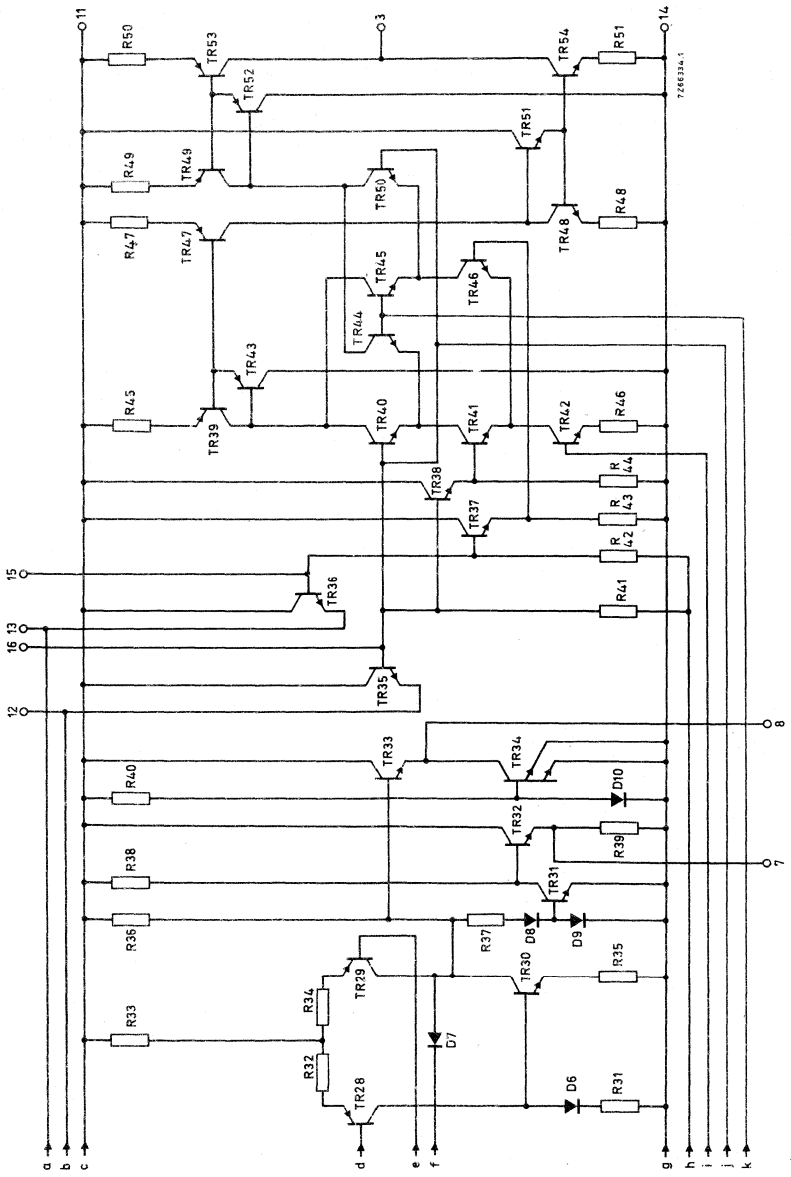
TCA540 : 16-lead DIL; plastic.

TCA540Q: 16-lead QIL; plastic.

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11) V_{11-14} max. 18 V ¹⁾

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} -25 to +55 °C

CHARACTERISTICS

Supply voltage range (pin 11) V_{11-14} 10, 2 to 13, 2 V

Supply current I_{11} typ. 40 mA

The following characteristics are measured at $T_{amb} = 25$ °C; $V_{11-14} = 12$ V;
 $f_o = 38,9$ MHz unless otherwise specified.

Demodulator circuit

Zero signal d. c. outputs V_{7-14} typ. 5, 7 V
 V_{8-14} typ. 6 V

Input voltage (r. m. s. value) for 3 V
peak-to-peak output voltage V_{4-5} typ. 70 mV ²⁾

Input resistance R_{4-5} typ. 6 kΩ

Input capacitance C_{4-5} typ. 4, 7 pF

Bandwidth of video output (3 dB; pin 8) B typ. 5 MHz

Output resistances R_{8-14} typ. 35 Ω
 R_{7-14} typ. 75 Ω

Differential gain (pin 8) D.S.B. dG typ. 2 %
S.S.B. dG typ. 5 %

Differential phase (pin 8) D.S.B. $d\phi$ typ. 2 °
S.S.B. $d\phi$ typ. 3 °

¹⁾ Allowed only while receiver is warming up.

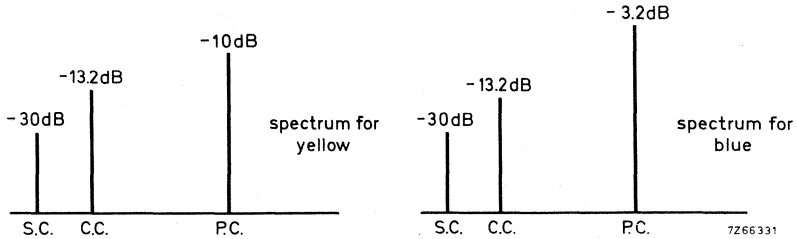
²⁾ Input signal modulated in accordance with the CCIR standard system B.

CHARACTERISTICS (continued)

Intermodulation (see input conditions below)

Blue spectrum (pin 8)	typ.	60	dB
Yellow spectrum (pin 8)	typ.	52	dB

Input conditions for intermodulation measurements (75% saturation):



S.C. : sound carrier attenuation	}	with respect to top sync level
C.C. : chrominance carrier attenuation		
P.C. : picture carrier attenuation		

The sound-chrominance beat suppression is related to the B. W. amplitude with a top sync level of 3 V.

A.F.C. circuit (see figures 1 and 2 on pages 8 and 9)

Output control voltage	V ₃₋₁₄	1 to 11	V
Sensitivity per kHz (R _L = 50 kΩ)	V ₃₋₁₄	typ.	40 mV



PINNING

- | | |
|-----------------------------------|--|
| 1. Not connected | 9. Not connected |
| 2. Not connected | 10. Not connected |
| 3. A. F. C. output | 11. Supply voltage (positive) |
| 4. Balanced i. f. input | 12. Tank coil connection (reference carrier) |
| 5. Balanced i. f. input | 13. Tank coil connection (reference carrier) |
| 6. Not connected | 14. Earth (negative supply) |
| 7. Video output (pos. going sync) | 15. Tank coil connection (a.f.c.) |
| 8. Video output (neg. going sync) | 16. Tank coil connection (a.f.c.) |

APPLICATION INFORMATION

Below some information is given about the external circuit.
The function is quoted against the corresponding pin numbers.

1. Not connected
2. Not connected
3. A. F. C. output

This output is a current source, so for driving the tuner the current must be translated into a voltage and this has been done by means of a network as shown in figure 3 on page 9. The network load is about 50 k Ω .

With this load, a sensitivity is obtained of about 40 mV/kHz.

Since a.f.c. is most important at u.h.f., the control network has been designed for optimum holding range and correction factor in this band, combined with the ELC2000S tuner.

The holding range with this control network is limited to about 6 MHz for u.h.f., so in this case it is not necessary to switch off the a.f.c. during tuning.

The correction factor ranges from 3,3 for v.h.f. to more than 20 in the u.h.f. band. The table below gives examples for some channels in an application using the ELC2000S.

channel	catching range (MHz)	holding range (MHz)	correction factor
4	-0,6 to +0,5	-0,6 to +0,5	3,3
9	-0,8 to +0,8	-0,8 to +0,8	5
28	-2,8 to +0,9	-2,8 to +2,8	18
60	-2,3 to +0,7	-2,3 to +2,3	14

APPLICATION INFORMATION (continued)

4. Balanced i. f. input (in conjunction with pin 5)

A balanced input is provided at pins 4 and 5. The d. c. level is set internally, and the signal should be applied from a floating transformer winding or through coupling capacitors. An unbalanced signal may be applied to either pin, the other has to be decoupled to earth by a capacitor of about 1,5 nF. The input impedance is typically $6\text{ k}\Omega/4, 7\text{ pF}$. The input signal for 3 V peak-to-peak output signal is about 70 mV (rms).

5. Balanced i. f. input (see pin 4).

6. Not connected

7. Video output (positive going sync)

The a. c. performance of this output is the same as that of pin 8. The d. c. level has a spread of $\pm 10\%$.

8. Video output (negative going sync)

This video signal is intended to be used for driving the video output stage in a black-and-white receiver or the luminance channel in a colour receiver. The signal has excellent figures for differential gain and phase so that also chroma and sound take-off is possible at this output.

This output is matched with the TBA890 or TBA900 signal processing integrated circuit (see figure 1 on page 8).

For use with the TBA500 (luminance combination) an external matching network is required (see figure 2 on page 9).

A 5,5 MHz trap can be connected in series with the video output for driving the luminance channel, to avoid sound-chroma beat in the video part of the receiver.

This type of demodulator will cause white peaks in the video signal when interferences are received. For this reason a white spot inverter is used which detects white peaks and reverses them to black level.

The zero signal d. c. level is $6\text{ V} \pm 5\%$.

9. Not connected

10. Not connected

11. Positive supply (12 V)

Correct operation is obtained at voltages between 10,2 V and 13,2 V.

During short periods (e. g. while tubes are warming up) a supply voltage of 18 V is allowed.

12. Reference tuned circuit (in conjunction with pin 13)

A tuned circuit is connected between pins 12 and 13 to provide the carrier filtering. The damping impedance between these two pins is about $6\text{ k}\Omega$. The choice of the L/C ratio of the tuned circuit is a compromise between a good figure for differential gain and intermodulation products. Excellent differential gain/phase performance requires a low tuning capacitance. However, the lowest intermodulation products will be obtained by a large tuning capacitance. A proved practical value of 47 pF gives good results. The unloaded quality factor in this circuit has to be > 50 .

13. Reference tuned circuit (see pin 12)

APPLICATION INFORMATION (continued)

- 14. Negative supply (earth)
- 15. A.F.C. tuned circuit (in conjunction with pin 16)

This circuit is loosely coupled to the reference tuned circuit of the demodulator by means of the collector-base capacitances of TR35 and TR36 (see circuit diagrams on pages 2 and 3). The unloaded quality factor of this tuned circuit has to be >70 . The temperature stability is important for the a. f. c. reference tuned circuit. Using a miniature coil-former with powder iron core a good compensation is obtained with a NP0 temperature coefficient capacitor.

The drift of the a. f. c. is typical $+1 \text{ kHz}/^{\circ}\text{C}$.

- 16. A.F.C. tuned circuit (see pin 15)

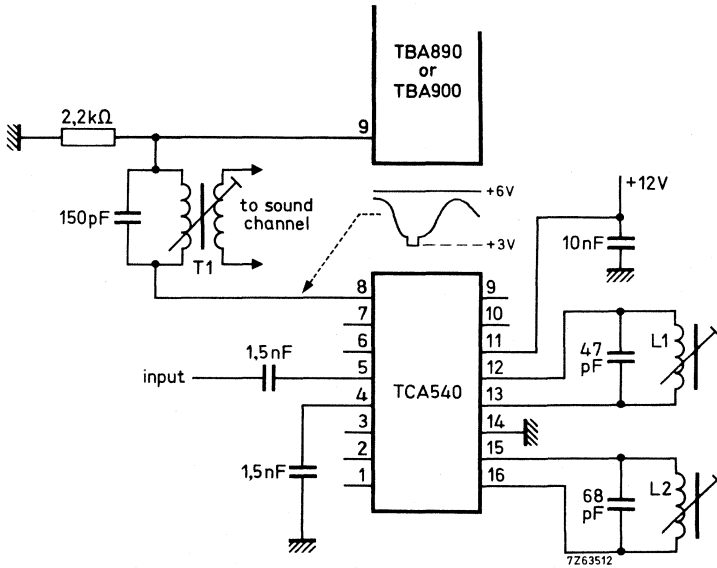
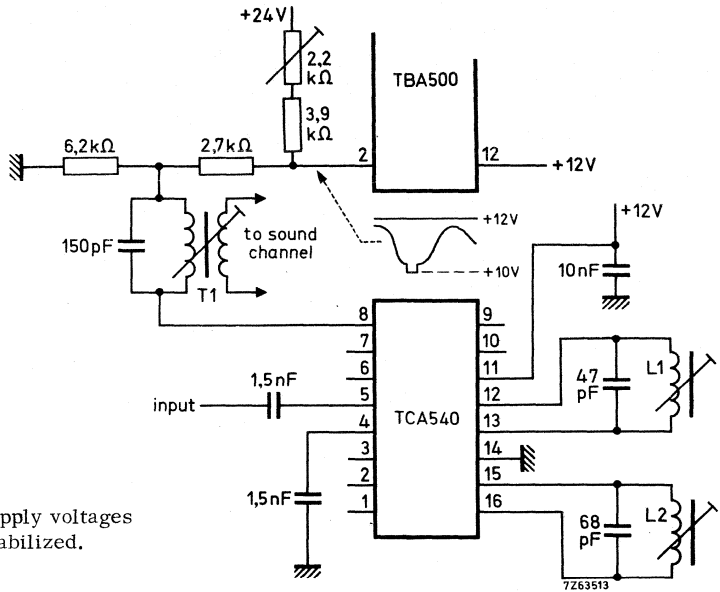


Fig. 1 Interface connections of the TCA540 with the TBA890 or TBA900

APPLICATION INFORMATION (continued)



Note: The two supply voltages must be stabilized.

Fig. 2 Interface connection of the TCA540 with the TBA500

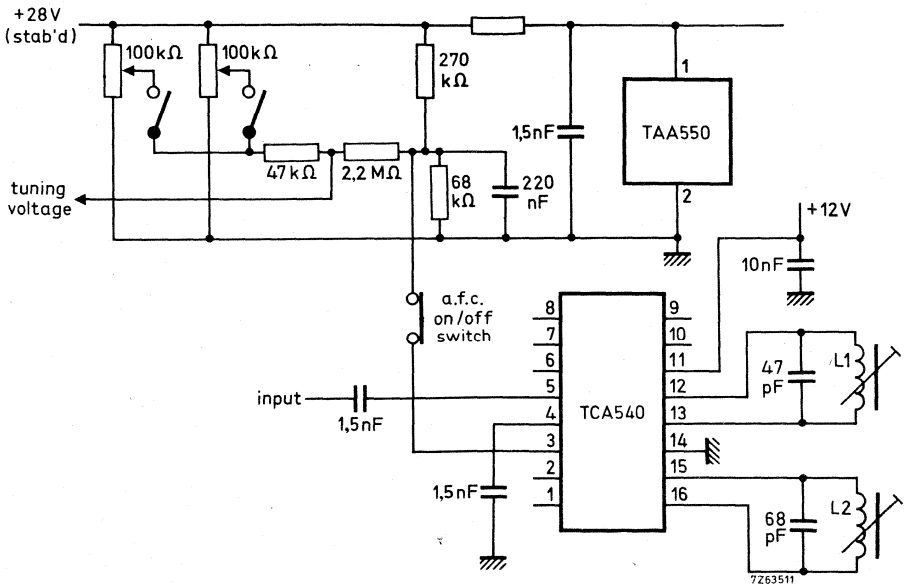


Fig. 3 A.F.C. with TCA540

CHROMINANCE AMPLIFIER FOR SECAM OR PAL/SECAM DECODERS

The TCA640 is an integrated chrominance amplifier for either a SECAM decoder or a double standard PAL/SECAM decoder.

Switching of the standard is performed internally, controlled by an external applied d. c. signal.

In addition to the chrominance amplifier the circuit also incorporates a 7, 8 kHz flip-flop and an identification circuit for SECAM.

For PAL identification the circuit included in the TBA540 should be used.

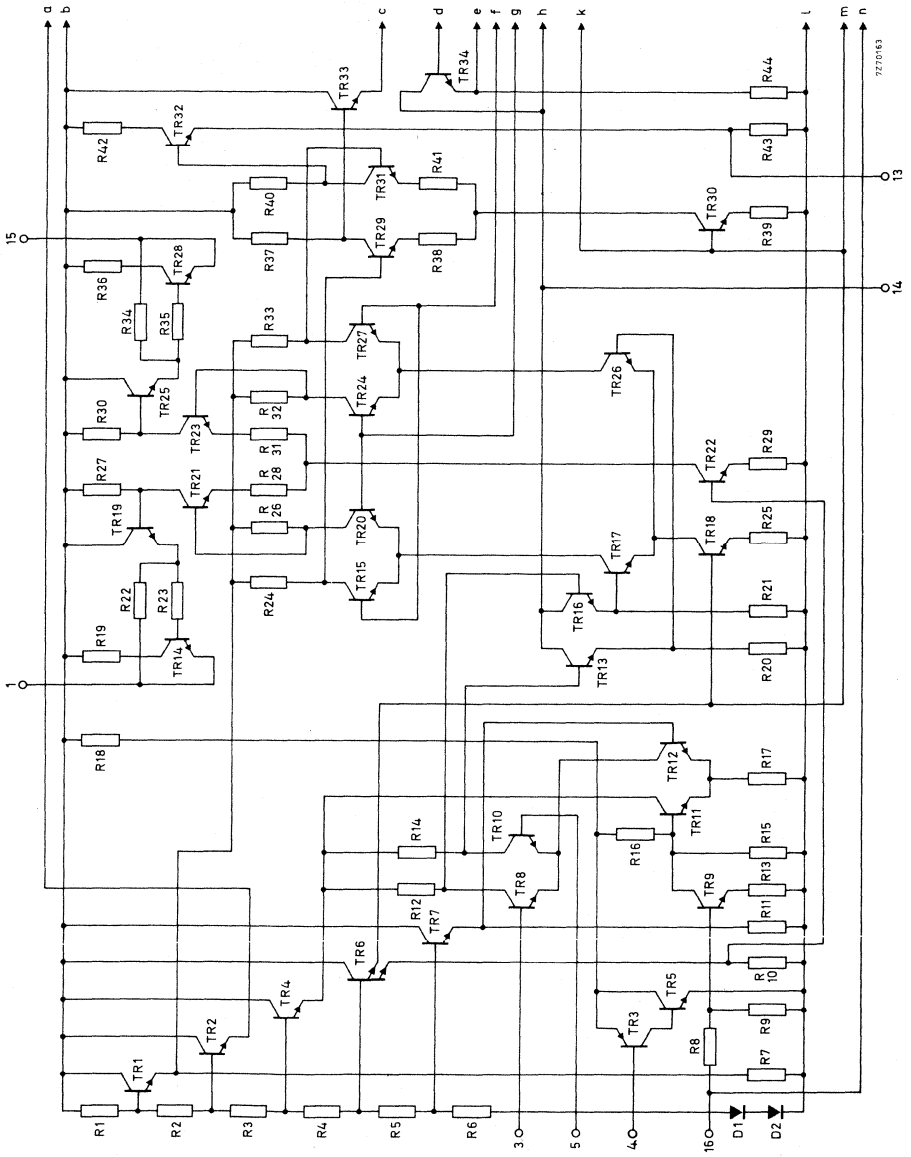
Furthermore, the TCA640 incorporates a blanking circuit, a burst gating circuit and a colour killer detector.

QUICK REFERENCE DATA			
Supply voltage	V_{14-2}	nom.	12 V
Supply current	I_{14}	nom.	37 mA

		PAL	SECAM
Chrominance input signals (peak-to-peak value)	$V_{3-5(p-p)}$	>	4
		<	80
Chrominance output signals (peak-to-peak value)	$V_{15-2(p-p)}$ $V_{1-2(p-p)}$	} typ.	500
			2000 mV
Burst output (closed a. c. c. loop) (peak-to-peak value)	$V_{13-2(p-p)}$	typ.	1
System switching signal	V_{4-2}	typ.	12
Burst blanking of chrominance signal		>	40
Chrominance blanking at field identification		>	-
Square-wave output (7, 8 kHz) (peak-to-peak value)	$V_{12-2(p-p)}$	typ.	3

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V₁₄₋₂ max. 13,2 V

Power dissipation

Total power dissipation P_{tot} max. 625 mW

Temperatures

Storage temperature T_{stg} -25 to +125 °C

Operating ambient temperature T_{amb} -25 to +65 °C ¹⁾

CHARACTERISTICS measured in the circuit on page 6

Supply voltage V₁₄₋₂ typ. 12 V
10,2 to 13,2 V

Required input signals at V₁₄₋₂ = 12 V and T_{amb} = 25 °C

Chrominance input signal

→ peak-to-peak value V₃₋₅(p-p) { PAL 4 to 80 mV
SECAM 7 ²⁾ to 400 mV

Automatic chrominance control starting V₁₆₋₂ PAL typ. 1,2 V ³⁾

Flyback pulses for blanking and

burst/identification lines-keying See note 4

Line flyback pulses (positive)

peak-to-peak value V₆₋₂(p-p) 4,5 to 12 V

Field identification pulses (positive)

peak-to-peak value V₇₋₂(p-p) 4 to 12 V

System switch signal

V₄₋₂ { PAL 7 to V₁₄₋₂ V
SECAM 0 to 1 V

Colour killer threshold

V₁₆₋₂ PAL typ. 2,5 V ⁵⁾

¹⁾ When a stabilized power supply of ≤12 V is applied, T_{amb} is max. 75 °C.

²⁾ Start of limiting.

³⁾ A negative-going potential provides a 26 dB a. c. c. range.

⁴⁾ The line flyback pulses also provide the clock pulses for the flip-flop.

⁵⁾ The colour killer is operative above the quoted input voltage.

CHARACTERISTICS (continued)

Obtainable output signals

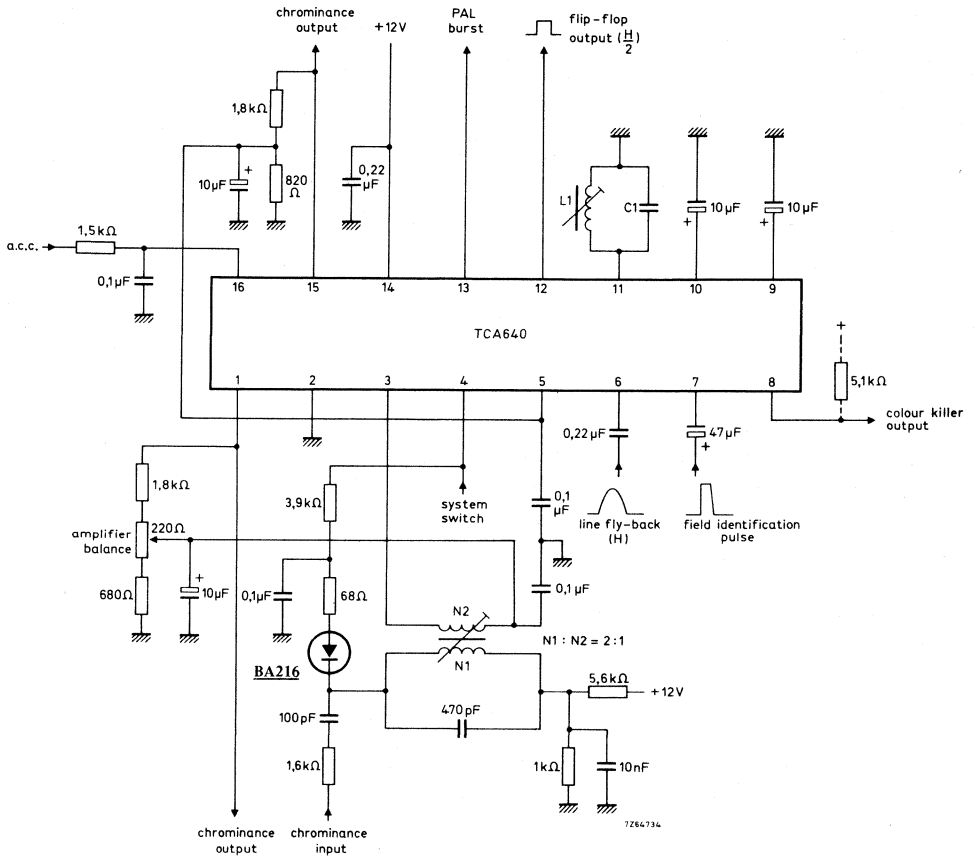
Chrominance output signals

peak-to-peak value	$V_{15-2(p-p)}$ $V_{1-2(p-p)}$	$\left. \begin{array}{l} \text{PAL} \\ \text{SECAM} \end{array} \right\}$	425 to 575 1, 8 to 2, 3	mV V
<u>Phase difference between output pins</u>	$\Delta\phi_{15-1}$	PAL	170° to 190°	1)
<u>Burst signal</u> (peak-to-peak value)	$V_{13-2(p-p)}$	PAL	typ. 1	2)
<u>Identification signal</u>				
peak-to-peak value	$I_{11(p-p)}$	SECAM	1, 4 to 2, 4	mA
<u>Output resistance</u>	R_{11-2}		2 to 2, 9	k Ω
<u>Flip-flop signal</u>				
peak-to-peak value	$V_{12-2(p-p)}$		2, 5 to 3, 5	V
<u>Colour killer</u>	killed	$\left\{ \begin{array}{l} V_{8-2} \\ I_g \end{array} \right.$	<	0, 5 V
			<	10 mA
	unkilled	$\left\{ \begin{array}{l} V_{8-2} \\ I_g \end{array} \right.$	<	V_{14-2} V
			<	10 μ A
<u>Bandwidth of chrominance amplifier (-1 dB)</u>				
at a carrier frequency of 4,2 MHz			>	± 1 MHz
<u>Blanking</u>				
burst rejection		PAL	>	40 dB
rejection identification lines with field identification		SECAM	>	40 dB

1) Over the a. c. c. control range the phase difference varies less than 2, 5°.

2) The burst is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Pinning

- | | |
|-------------------------------------|---|
| 1. Chrominance output | 9. Identification integrating |
| 2. Earth (negative supply) | 10. capacitor (SECAM) |
| 3. Chrominance input | 11. Identification tank circuit (SECAM) |
| 4. System switch input | 12. Flip-flop output |
| 5. Chrominance input | 13. Burst output (PAL) |
| 6. Line fly-back pulse input | 14. Supply voltage (12 V) |
| 7. Field identification pulse input | 15. Chrominance output |
| 8. Colour killer output | 16. A.C.C. input |

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance output (in conjunction with pin 15)

A balanced output is available at pins 1 and 15.

At SECAM reception a limited signal of 2 V peak-to-peak is available, starting from an input voltage of 15 mV peak-to-peak.

At PAL reception the output signal is 500 mV peak-to-peak for a burst signal of 1 V peak-to-peak.

An external d. c. network is required which provides negative feedback to pin 3. The same holds for the feedback from pin 15 to pin 5.

The figures for input and output signals are based on a 100% saturated colour bar signal.

2. Negative supply (earth)3. Chrominance input (in conjunction with pin 5)

The input signal is derived from a bandpass filter which provides the required "bell" shape bandpass for the SECAM signal and a flat bandpass for the PAL signal.

The input signal can be supplied either in a balanced mode or single ended. Both inputs (pins 3 and 5) require a d. c. potential of about 2.5 V obtained from a resistive divider connected to output pins 1 and 15. The figures for the input signals are based on a 100% saturated colour bar signal and a burst-to-chrominance ratio of 1:3 of the input signal (PAL).

4. System switch input

Between 7 V and the supply voltage, the gain of the chrominance amplifier is controlled by the a. c. c. voltage at pin 16.

The chrominance amplifier then provides linear amplification required for the PAL signal. Between 0 V and 1 V the chrominance amplifier operates as a limiter for the SECAM signal.

5. Chrominance input (see pin 3)6. Line fly-back pulse input (in conjunction with pin 11)

Positive going pulses provide

- blanking of the chrominance signal at the outputs (pins 1 and 15).

- burst gating for both PAL and SECAM.

The carrier signal present during the second half of the back porch of the SECAM signal is gated. It provides line identification when the circuit L_1C_1 (see circuit on page 6) is tuned to 4.25 MHz (at $C_1 = 470$ pF).

- trigger signal for the flip-flop.

7. Field identification pulse input (in conjunction with pin 11)

Like the line fly-back pulses, positive going identification pulses provide blanking and burst gating.

To operate the TCA640 on the identification lines (SECAM) in the field blanking period the circuit L_1C_1 (see circuit on page 6) should be tuned to 3.9 MHz and the capacitor C_1 should be increased to 1 nF. The field fly-back pulse should be shaped so that its amplitude exceeds 4 V during the identification lines.

APPLICATION INFORMATION (continued)8. Colour killer output

This pin is driven from the collector of an internal switching transistor and requires an external load resistor connected to the supply voltage. The killer is operative when the a. c. c. voltage exceeds the threshold, when the SECAM chrominance signal at the input is below the limiting level or when the flip-flop operates in the wrong phase.

9. Identification integrating capacitor (SECAM)10. Identification integrating capacitor (SECAM)11. Identification detector tank circuit (see pins 6 and 7)12. Flip-flop output

A square wave of 7,8 kHz with an amplitude of 3 V is available at this pin. An external load resistor is not required.

13. Burst output (PAL)

A 1 V peak-to-peak burst (kept constant by the a. c. c. system) is produced here.

14. Supply voltage (12 V)

Correct operation occurs within the range 10,2 to 13,2 V.

The power dissipation must not exceed 625 mW at 65 °C ambient temperature.

15. Chrominance output (see pin 1)16. A. C. C. input

With the system switch input (pin 4) connected for PAL operation, a negative going potential gives a 26 dB range of a. c. c. starting at +1,2 V

During SECAM operation, the voltage at the input should not exceed +0,5 V, otherwise the SECAM identification circuit and the colour killer become inoperative.

CHROMINANCE DEMODULATOR FOR SECAM OR PAL/SECAM DECODERS

The TCA650 is an integrated synchronous demodulator for both the SECAM and PAL chrominance signals.

Switching of the standard is performed internally, controlled by an external applied d.c. signal.

In addition to the synchronous demodulator, which delivers colour difference signals, the circuit also incorporates:

- a PAL matrix, used for adding the delayed and non-delayed signals to obtain separately the (R-Y) and (B-Y) components of the chrominance signal.
- a PAL switch, which reverses the phase of the (R-Y) component of the chrominance signal on alternating lines.
- a SECAM switch, which performs the separation of the DR and DB components of the chrominance signal by switching the delayed and non-delayed signals.
- a SECAM limiter.

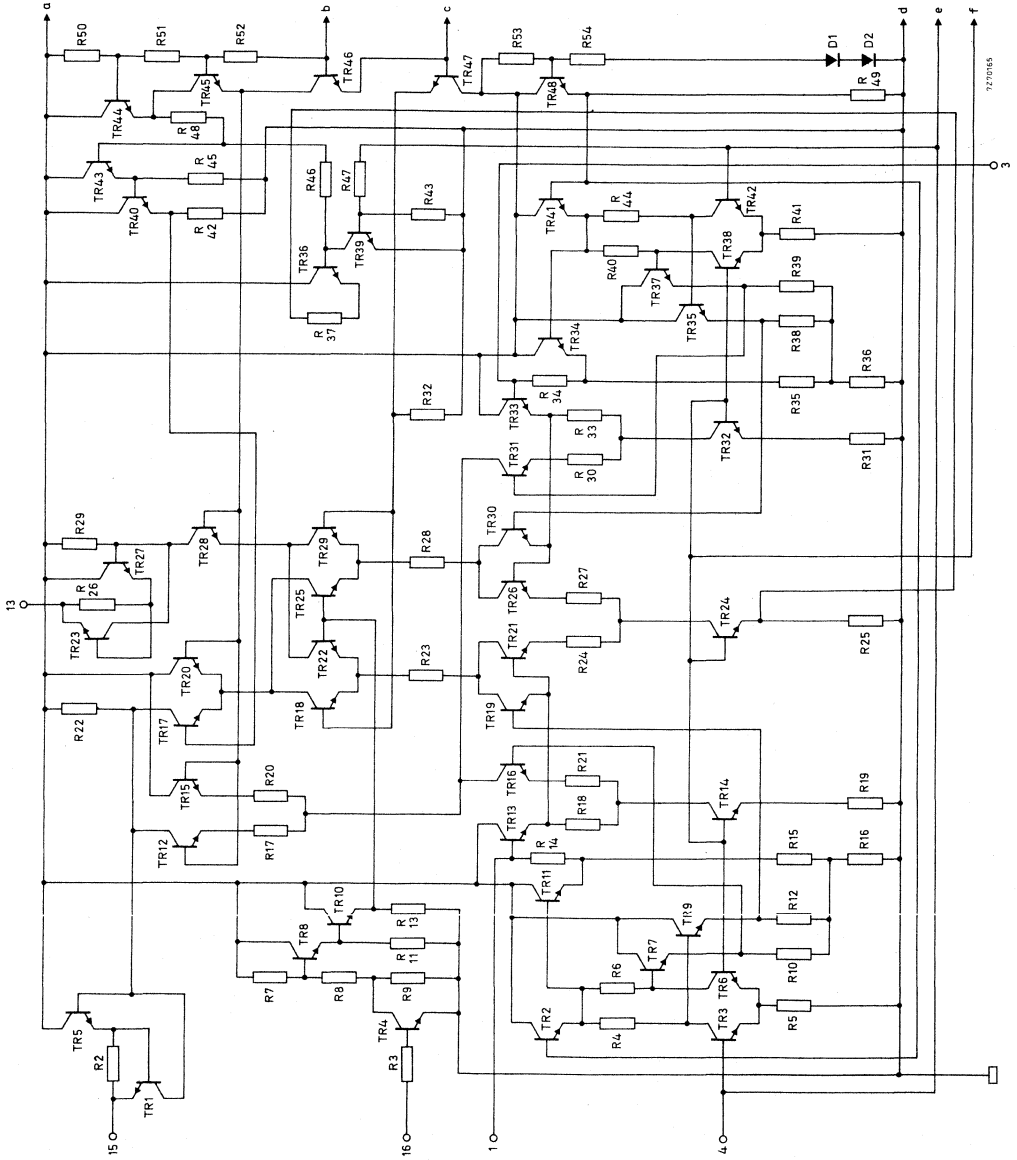
QUICK REFERENCE DATA			
Supply voltage		V ₁₄₋₂ nom.	12 V
Supply current		I ₁₄ nom.	36 mA

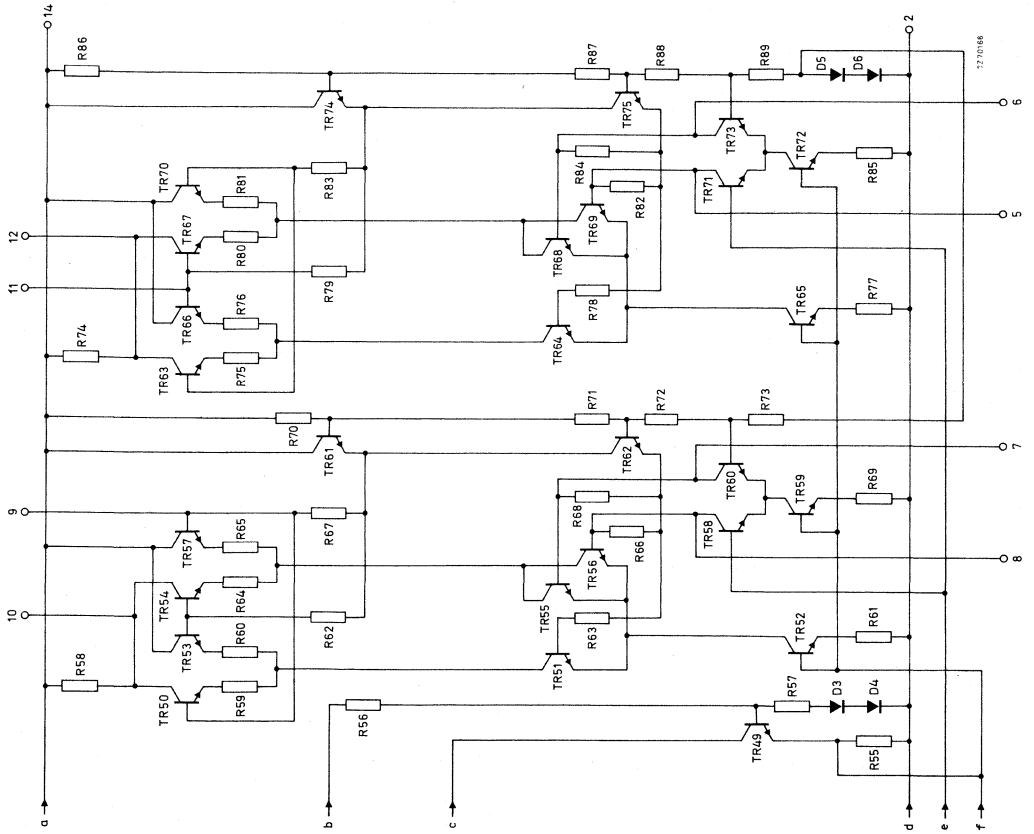
		PAL	SECAM
Chrominance input signals (peak-to-peak value)	V _{1-2(p-p)} } V _{3-2(p-p)} }	typ. 50	200 mV
System switch input	V ₄₋₂	typ. 12	0 V
Colour difference output signals (peak-to-peak value)	(R-Y): V _{12-2(p-p)} (B-Y): V _{10-2(p-p)}	typ.	1, 1 V 1, 47 V
Reference input signals (PAL) (peak-to-peak value)	V _{6-2(p-p)} } V _{7-2(p-p)} }	typ.	1 V
Square-wave input (peak-to-peak value)	V _{16-2(p-p)}	typ.	3 V

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

TCA650





RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{14-2} max. 13,2 V

Power dissipation

Total power dissipation P_{tot} max. 510 mW

Temperatures

Storage temperature T_{stg} -25 to +125 °C

Operating ambient temperature T_{amb} -25 to +65 °C¹⁾

CHARACTERISTICS measured in the circuit on page 6

Supply voltage V_{14-2} typ. 12 V
10,2 to 13,2 V

Required input signals at $V_{14-2} = 12$ V and $T_{amb} = 25$ °C

Chrominance input signal

peak-to-peak value $V_{1-2(p-p)}$ } PAL 35 to 75 mV
 $V_{3-2(p-p)}$ } SECAM 150 to 400 mV

Input impedance

$|Z_{1-2}|$ } 1,2 to 2,6 kΩ
 $|Z_{3-2}|$ }

PAL matrix

Gain from both inputs to pin 13 2,3 to 3,3

Gain from both inputs to pin 15 2,6 to 3,6

Gain difference from line-to-line < 5 %

Phase errors from line-to-line in the
(R-Y) output for zero error in the (B-Y) output < 2,5°

Output impedance $|Z_{13-2}|$ } < 100 Ω
 $|Z_{15-2}|$ }

SECAM permutator

Diaphotie < -46 dB

Output signal (peak-to-peak value) $V_{13-2(p-p)}$ } 1,6²⁾ to 2,2 V
 $V_{15-2(p-p)}$ }

Output impedance $|Z_{13-2}|$ } < 100 Ω
 $|Z_{15-2}|$ }

¹⁾ When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

²⁾ At an input voltage of 0,15 V; at an input voltage > 0,2 V the figure is 1,7 V.

CHARACTERISTICS (continued)Demodulator

Chrominance input signal amplitude

PAL: (B-Y): peak-to-peak value	$V_{9-2(p-p)}$	typ. 0,22	V
(R-Y): peak-to-peak value	$V_{11-2(p-p)}$	typ. 0,28	V

SECAM: peak-to-peak value	$V_{9-2(p-p)}$ } $V_{11-2(p-p)}$ }	1,5 to 3	V
---------------------------	---------------------------------------	----------	---

Input impedance	$ Z_{9-2} $ } $ Z_{11-2} $ }	>	1	k Ω
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Reference input signal amplitude

PAL: peak-to-peak value	$V_{6-2(p-p)}$ } $V_{7-2(p-p)}$ }	0,5 to 1,5	V
-------------------------	--------------------------------------	------------	---

SECAM: peak-to-peak value	$V_{5-2(p-p)}$ } $V_{8-2(p-p)}$ }	0,18 ¹⁾ to 1,5	V
---------------------------	--------------------------------------	---------------------------	---

Input impedance	$ Z_{5-2} $; $ Z_{7-2} $ } $ Z_{6-2} $; $ Z_{8-2} $ }	0,75 to 1,25	k Ω
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Colour difference output signal

(R-Y): peak-to-peak value	$V_{12-2(p-p)}$	0,99 to 1,21	V ²⁾
---------------------------	-----------------	--------------	-----------------

(B-Y): peak-to-peak value	$V_{10-2(p-p)}$	1,32 to 1,62	V ²⁾
---------------------------	-----------------	--------------	-----------------

Output impedance	$ Z_{10-2} $ } $ Z_{12-2} $ }	2,4 to 4,2	k Ω
------------------	----------------------------------	------------	------------

Diaphotie at SECAM operation

Diaphotie of the total circuit at frequencies corresponding to saturated green

$D_R = 4,72$ MHz and $D_B = 4,04$ MHz	<	-40	dB
---------------------------------------	---	-----	----

Square wave input

peak-to-peak value	$V_{16-2(p-p)}$	2,5 to 3,5	V
--------------------	-----------------	------------	---

Input impedance	$ Z_{16-2} $	>	3,8	k Ω
-----------------	--------------	---	-----	------------

System switch input ³⁾

PAL:	7 to V_{14-2}	V
------	-----------------	---

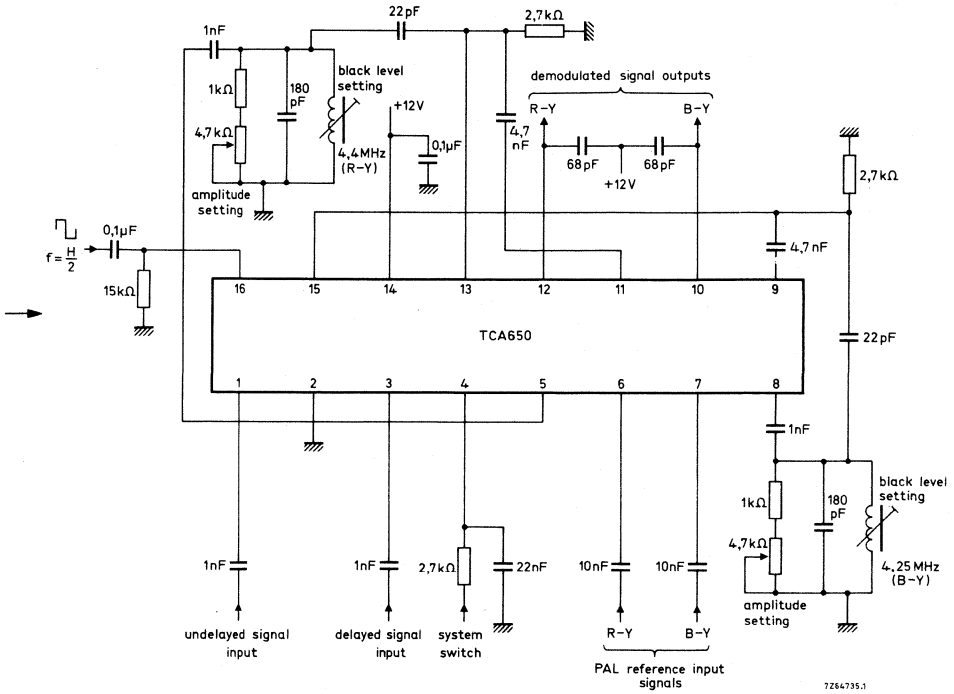
SECAM:	0 to 1	V
--------	--------	---

¹⁾ Limiting starts at the quoted value.

²⁾ The peak-to-peak clipping level for PAL is about 4,7 V for (B-Y) and 3 V for (R-Y). The discriminator characteristic allows a maximum peak-to-peak output signal of 3,6 V for (B-Y) and 2,4 V for (R-Y) (SECAM).

³⁾ The switching signal is applied to pin 4 via a resistor of 2,7 k Ω ($\pm 10\%$).

APPLICATION INFORMATION



Pinning

- | | |
|--|---|
| <ol style="list-style-type: none"> 1. Chrominance input 2. Earth (negative supply) 3. Chrominance input 4. System switch input 5. Reference (R-Y) input SECAM 6. Reference (R-Y) input PAL 7. Reference (B-Y) input PAL 8. Reference (B-Y) input SECAM | <ol style="list-style-type: none"> 9. Chrominance (B-Y), D_B input 10. Colour difference (B-Y) output 11. Chrominance (R-Y), D_R input 12. Colour difference (R-Y) output 13. Chrominance (R-Y), D_R output 14. Supply voltage (12 V) 15. Chrominance (B-Y), D_B output 16. Square wave input |
|--|---|

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance input

The blanked composite chrominance signal from pin 1 of the TCA640 is applied to this input via a resistive divider.

2. Negative supply (earth)3. Chrominance input

The blanked composite chrominance signal from pin 15 of the TCA640 is applied to this input via a delay-line, which has a delay time of 64 μ s.

4. System switch input

The control voltage for switching the standard is applied to this input via a resistor of 2,7 k Ω (\pm 10%). A decoupling capacitor of at least 10 nF is recommended. Between 7 V and the supply voltage the circuit operates in the PAL mode, whereas between 0 V and 1 V the mode SECAM is selected.

5. Reference input for the (R-Y) demodulator

The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 11 via a tank circuit. The tank circuit is tuned such that the level at the (R-Y) output (pin 12) during black ($f_0 = 4,4$ MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 12 can be adjusted by damping the tank circuit.

6. Reference input for the (R-Y) demodulator

A PAL reference signal having (R-Y) phase is applied to this pin.

7. Reference input for the (B-Y) demodulator

A PAL reference signal having (B-Y) phase is applied to this pin.

8. Reference input for the (B-Y) demodulator

The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 15 via a tank circuit. The tank circuit is tuned such that the level at the (B-Y) output (pin 10) during black ($f_0 = 4,25$ MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 10 can be adjusted by damping the tank circuit.

9. Chrominance input to the (B-Y), D_B demodulator

The output signal of pin 15 is applied via a coupling capacitor of 4,7 nF.

10. Output of the (B-Y) demodulator

The output signal of the balance demodulator contains an r.f. ripple of twice the chrominance frequency to be filtered by a π filter. At SECAM the required de-emphasis circuit should be applied.

11. Chrominance input to the (R-Y), D_R demodulator

The output signal of pin 13 is applied via a coupling capacitor of 4,7 nF.

APPLICATION INFORMATION (continued)12. Output of the (R-Y) demodulator

See pin 10.

13. Chrominance (R-Y), D_R output

The (R-Y) component of the chrominance signal (D_R component at SECAM) is present at this pin.

The signal is applied to the input of the (R-Y) demodulator (pin 11) and to the tank circuit for the SECAM reference signal.

The emitter follower output should be loaded with a 2,7 k Ω resistor to obtain an output impedance of <100 Ω .

14. Supply voltage (12 V)

Correct operation occurs within the range 10,2 to 13,2 V.

The power dissipation must not exceed 510 mW at 65 °C ambient temperature.

15. Chrominance (B-Y), D_B output

The (B-Y) component of the chrominance signal (D_B component at SECAM) is present at this pin.

The signal is applied to the input of the (B-Y) demodulator (pin 9) and to the tank circuit for the SECAM reference signal.

The emitter follower output should be loaded with a 2,7 k Ω resistor to obtain an output impedance of <100 Ω .

16. Square wave input

A square wave with an amplitude of 3 V drives the PAL switch or the SECAM permutator.

The square wave is available at pin 12 of the TCA640.

CONTRAST, SATURATION AND BRIGHTNESS CONTROL CIRCUIT FOR COLOUR DIFFERENCE AND LUMINANCE SIGNALS

The TCA660B is an integrated circuit performing the control functions of contrast, saturation and brightness in colour television receivers.

Contrast is controlled by three tracking electronic potentiometers; one for the luminance signal and the other two for the (R-Y) and (B-Y) colour difference signals.

In addition two tracking electronic potentiometers provide the saturation control of the colour difference signals.

Brightness is controlled by varying the black level of the luminance signal at the output. An inverting amplifier is also included for matrixing the (G-Y) signal from the (R-Y) and (B-Y) colour difference signals.

QUICK REFERENCE DATA

Supply voltage	V_{13-4}	nom.	12	V	
Supply current	I_{13}	nom.	35	mA	

Luminance input current (black-to-white positive video signal)	I_{16}	typ.	0,7	mA	
Luminance output voltage (black-to-white positive video signal; peak-to-peak value)	$V_{1-4(p-p)}$	typ.	3	V	1)
Black level (nominal value)	V_{1-4}	typ.	4,2	V	
Brightness control (around nominal black level)	V_{1-4}		+1 to -2	V	
Gain of the (R-Y) and (B-Y) amplifier		typ.	5	dB	1) 2) ←
Gain of the (G-Y) amplifier		typ.	1		
Contrast control range			+3 to -20	dB	3)
Saturation control range			+6 to -20	dB	3)

1) At nominal contrast setting (max. contrast -3 dB)

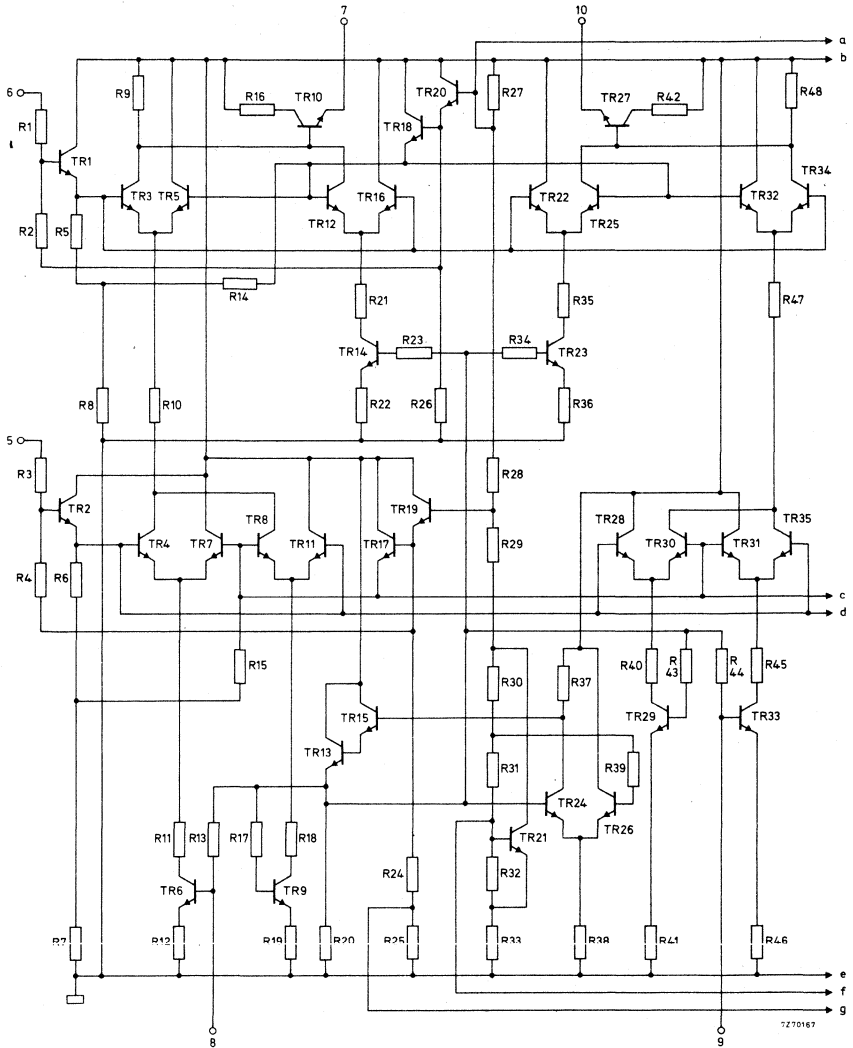
2) At nominal saturation control setting (max. saturation -6 dB)

3) Nominal contrast and nominal saturation are specified as 0 dB.

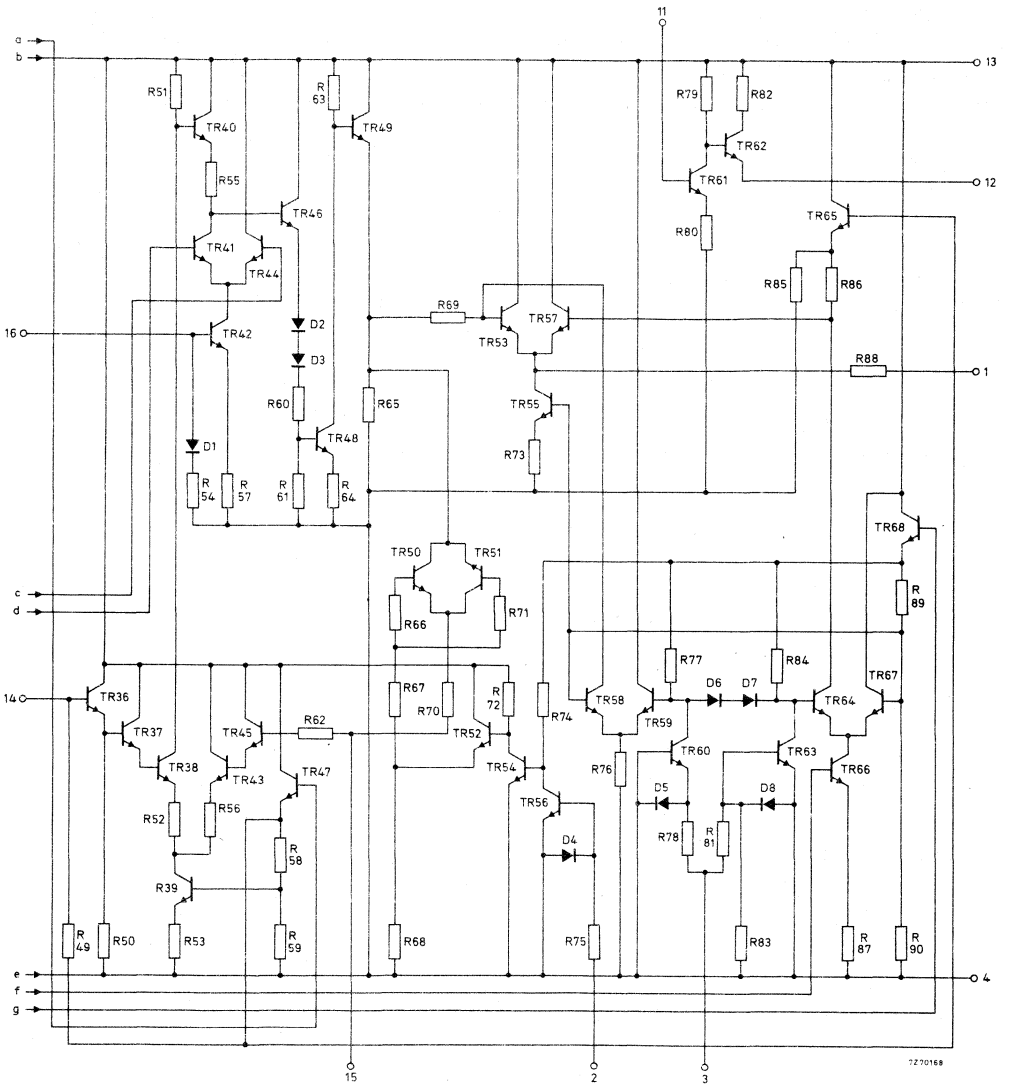
PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage

Supply voltage V_{13-4} max. 13,2 V

Power dissipation

Total power dissipation P_{tot} max. 600 mW

Temperatures

Storage temperature T_{stg} -25 to +125 °C

Operating ambient temperature T_{amb} -25 to +65 °C¹⁾

CHARACTERISTICS measured in the circuit on page 7

Supply voltage V_{13-4} typ. 12 V
10,2 to 13,2 V

Required input signals at $V_{13-4} = 12$ V and $T_{amb} = 25$ °C

Luminance input current

black-to-white positive video signal I_{16} typ. 0,7 mA
0 to 2,5 mA

Input impedance at $I_{16} = 1$ mA $|Z_{16-4}|$ 60 to 90 Ω

Input impedance variation for an

input current variation $\Delta I_{16} = \pm 0,5$ mA $|\Delta Z_{16-4}|$ ∓ 25 Ω

Colour difference input voltage

(R - Y); peak-to-peak value $V_{9-4(p-p)}$ < 0,7 V

(B - Y); peak-to-peak value $V_{8-4(p-p)}$ < 0,9 V

Input voltage variation before clipping

of the output voltage occurs $\left. \begin{array}{l} \Delta V_{8-4} \\ \Delta V_{9-4} \end{array} \right\}$ typ. 0,8 V

Input impedance $\left. \begin{array}{l} |Z_{8-4}| \\ |Z_{9-4}| \end{array} \right\}$ 3,5 to 6,5 kΩ

Blanking pulse (peak value) V_{3-4M} -1,5 to -10 V

Black level reinsertion pulse (peak value) V_{3-4M} +2 to +12 V²⁾

Black level clamp pulse (peak value) V_{2-4M} +1 to +12 V

Luminance output voltage at nominal contrast

black-to-white positive video signal;
peak-to-peak value $V_{1-4(p-p)}$ 2 to 4 V³⁾

1) When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

2) During scan V_{3-4} must be kept lower than 0,7 V (positive and negative) to avoid blanking of the luminance signal.

3) Nominal contrast is specified as maximum contrast -3 dB.

CHARACTERISTICS (continued)

<u>Black level</u> at nominal brightness setting	V_{1-4}	typ.	4,2 V	¹⁾
<u>Black level variation</u> with brightness setting	ΔV_{1-4}		+1 to -2 V	
<u>Contrast control voltage range</u>	V_{5-4}		See graph on page 6	
<u>Black level variation</u> with contrast control	ΔV_{1-4}	<	40 mV	²⁾
<u>Black level variation</u> with video contents	ΔV_{1-4}	<	20 mV	³⁾
<u>Variation between video black level</u> and reinserted black level at $\Delta T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $\Delta V_{13-4} \pm 10\%$	V_{1-4}	<	± 20 mV	
<u>Blanking level</u> with respect to nominal brightness	V_{1-4}		-0,8 to -1,2 V	
<u>Bandwidth</u> (-3 dB) of luminance signal B	B	>	6 MHz	
<u>Colour difference output signal</u> for nominal contrast and saturation ⁴⁾ ⁵⁾				
(R-Y); peak-to-peak value	$V_{10-4}(\text{p-p})$	typ.	1,25 V	⁶⁾ ←
(B-Y); peak-to-peak value	$V_{7-4}(\text{p-p})$	typ.	1,6 V	⁶⁾ ←
<u>D.C. output level</u>	V_{7-4} } V_{10-4} }	typ.	6,1 V	
<u>Output level variation</u> with contrast and saturation control	ΔV_{7-4} } ΔV_{10-4} }	<	500 mV	
<u>Permissible d.c. load impedance</u>	$ Z_{7-4} $ } $ Z_{10-4} $ }	>	4 k Ω	
<u>Saturation control voltage range</u>	V_{6-4}		See graph on page 6	
<u>Saturation control</u> at $V_{6-4} < 0,5 \text{ V}$		<	-50 dB	
<u>Bandwidth</u> (-3 dB) of colour difference signal B		>	2,5 MHz	

1) Nominal brightness setting $V_{14-4} = 5,7 \text{ V}$.

2) Only valid if the input current does not exceed 0,5 mA during black.

3) For a.c. coupling only.

4) Nominal contrast is specified as maximum contrast -3 dB.

5) Nominal saturation is specified as maximum saturation -6 dB.

6) This value is obtained at the specified maximum input voltage.

CHARACTERISTICS (continued)

(G-Y) amplifier

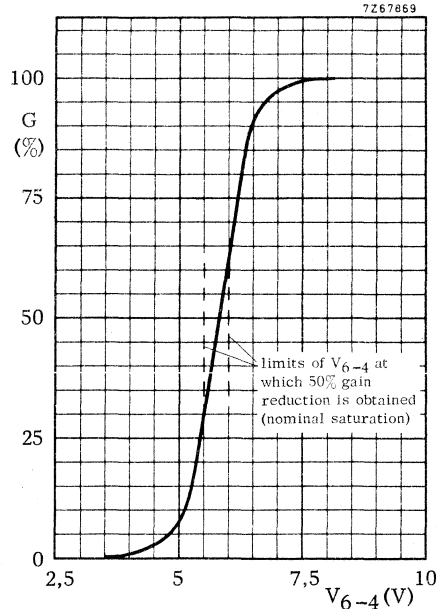
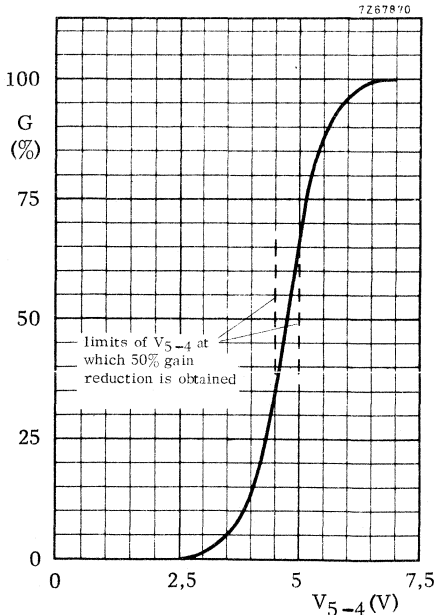
input voltage (peak-to-peak value)	$V_{11-4}(p-p)$	<	1 V
output voltage (peak-to-peak value)	$V_{12-2}(p-p)$	<	1 V
voltage gain	G_{11-12}		-1 to +0,5 dB

Tracking during contrast and saturation control

at a contrast decrease of 20 dB			
change of the ratio	$\frac{(R-Y)}{(B-Y)}$	<	±1 dB
change of the ratio	$\frac{Y}{(B-Y)}$		0 to 4 dB
at a saturation decrease of 20 dB			
change of the ratio	$\frac{(R-Y)}{(B-Y)}$	<	±1 dB

Cross coupling

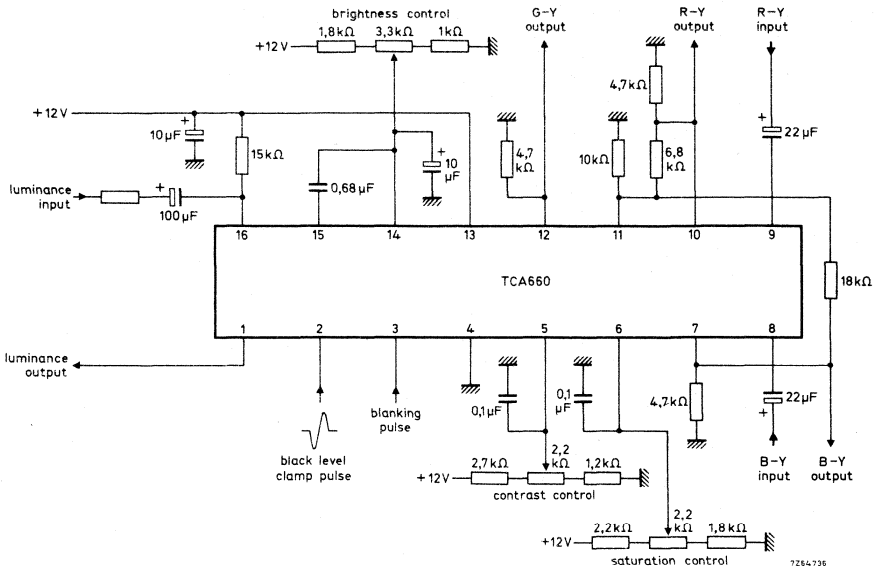
luminance signal to colour difference signal	<	-40 dB
(B-Y) signal to (R-Y) signal	<	-30 dB
colour difference signal to luminance signal	<	-40 dB



Contrast control of luminance amplifier

Saturation control of chrominance amplifier

APPLICATION INFORMATION



Pinning

- | | |
|--|---|
| <ol style="list-style-type: none"> 1. Luminance signal output 2. Black level clamp pulse input 3. Blanking pulse input 4. Earth (negative supply) 5. Contrast control input 6. Saturation control input 7. (B-Y) signal output 8. (B-Y) signal input | <ol style="list-style-type: none"> 9. (R-Y) signal input 10. (R-Y) signal output 11. (G-Y) signal input 12. (G-Y) signal output 13. Supply voltage (12 V) 14. Brightness control input 15. Black level clamp capacitor 16. Luminance signal input |
|--|---|

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Luminance signal output

A positive video signal of 3 V peak-to-peak is available at nominal contrast setting. The black level is clamped internally on the back porch.

By means of the brightness control the black level can be varied between 2,2 V and 5,2 V. The blanking level of the output signal will assume a value of 3,0 to 3,4 V.

2. Black level clamp pulse input

A positive pulse with a peak value between +1 V and +12 V will clamp the black level of the video signal to a nominal level of 4,2 V. The pulse may only be present during the back porch and should have a duration of about 3 μ s.

3. Blanking pulse input

Two modes operation can be selected by the choice of the amplitude of the pulse applied:

- blanking
- black level reinsertion

Blanking of the luminance output signal is obtained when the peak value of the pulse ranges from -1,5 to -10 V. An artificial black level of nominally +4,2 V is inserted in the luminance output signal during the blanking period when the peak value of the pulse ranges from +2 to +12 V.

During scan the amplitude at pin 3 should remain between +0,7 V and -0,7 V to avoid blanking.

4. Negative supply (earth)5. Contrast control input

The contrast curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

6. Saturation control input

The control curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

7. (B-Y) signal output

The amplitude of this signal is controlled by the contrast setting and the saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,6 V peak-to-peak is obtained at an input amplitude of 0,9 V peak-to-peak. The average level is typically 6,1 V.

8. (B-Y) signal input

The signal has to be a.c. coupled to the input.

To cope with the variation of picture contents an input voltage margin of $\pm 0,8$ V is provided, whereas the input signal has a typical value of $\pm 0,45$ V for a saturated colour bar signal.

APPLICATION INFORMATION (continued)9. (R-Y) signal input

The signal has to be a. c. coupled to the input.

To cope with the variation of picture contents an input voltage margin of $\pm 0,8$ V is provided, whereas the input signal has a typical value of $\pm 0,35$ V for a saturated colour bar input.

10. (R-Y) signal output

The amplitude of this signal is controlled by the contrast setting and saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,25 V peak-to-peak is obtained at an input amplitude of 0,7 V peak to peak. The average level is typically 6,1 V.

11. (G-Y) signal input

The (G-Y) signal is obtained by matrixing a part of the (R-Y) and (B-Y) signals in a resistor network. The input may range from 1 to 6,5 V. An average level of typical 5,9 V is required to produce an average output level of 6,1 V. The gain of the inverter stage is typically 1.

12. (G-Y) signal output

An inverted signal with an amplitude of maximum 1V peak-to-peak is available at this pin.

13. Supply voltage (12 V)

Correct operation occurs within the range 10,2 to 13,2 V.

The power dissipation must not exceed 600 mW at 65 °C ambient temperature.

14. Brightness control input

The black level of the luminance output signal tracks the potential applied to this pin. A typical value for setting the brightness control is 5,7 V, for which a black level of 4,2 V is obtained.

It is recommended that a capacitor of at least 10 μ F be connected between this pin and earth.

15. Black level clamp capacitor

The level of the back porch of the luminance output signal is stored in an external capacitor of about 0,68 μ F; the latter to be connected between pins 14 and 15.

16. Luminance signal input

A positive luminance signal of 0,7 mA peak-to-peak between black and white level drives the luminance amplifier.

A black level of about 0,3 mA is recommended. For a. c. coupling a bias resistor to the supply line is required to bias the amplifier properly.

The resistance depends on the signal amplitude e. g.: 15 k Ω is recommended for a input signal of 0,7 mA peak-to-peak.

COLOUR DEMODULATOR

with feed-back clamp

The TCA800 is a monolithic integrated circuit for colour television receivers incorporating the following functions :

- two synchronous demodulators for the (B-Y) and (R-Y) signals
- (G-Y) matrix
- PAL switch bistable
- RGB matrix

The device can drive simple single transistor RGB output stages.

The circuit also incorporates three feedback clamps to stabilize the black level, to eliminate the thermal drift in the demodulators.

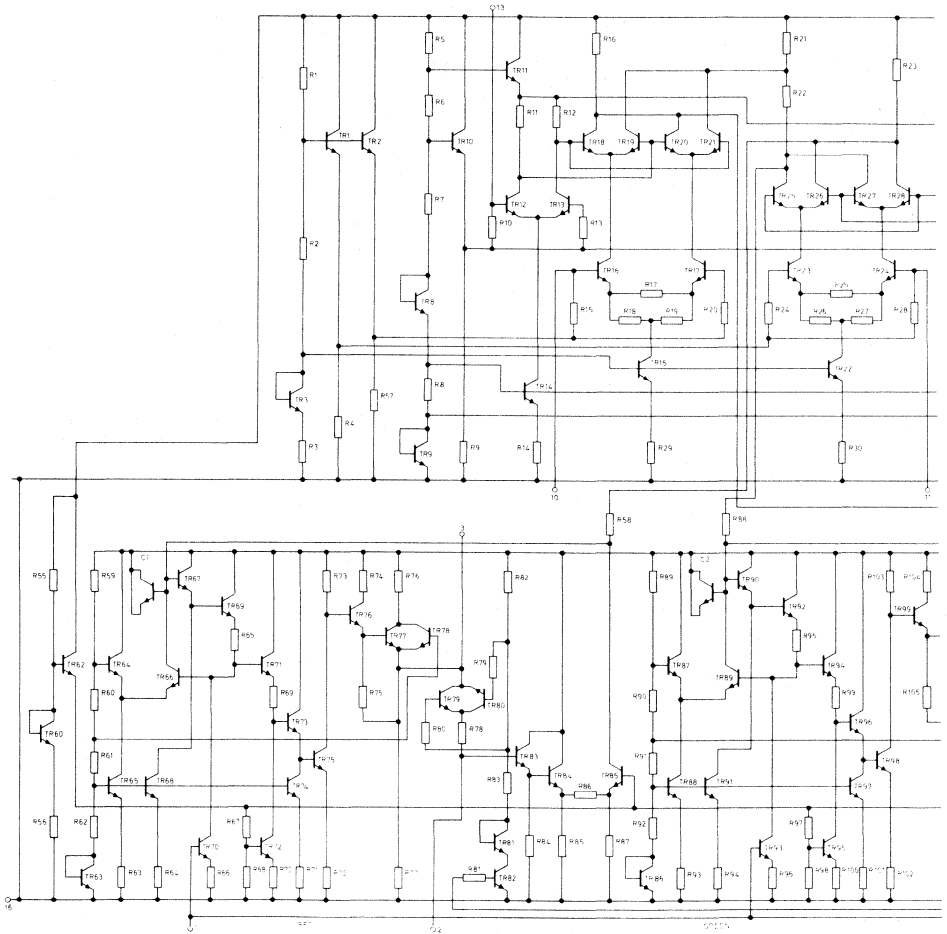
QUICK REFERENCE DATA			
Supply voltage	V_{9-16}	typ.	12 V
Supply current at $I_g = 0.5$ mA	I_g	typ.	47 mA
Voltage gain of chrominance (R-Y) signal channel at $V_{11-16} = 50$ mV; $f = 4.43$ MHz; video gain = 20x	G_{11-3}	typ.	17.5
Voltage gain of luminance (Y) channel $V_{1-16(p-p)} = 1$ V (black to white)	$G_{1-3;5;7}$	typ.	5
Operating ambient temperature range	T_{amb}		-20 to +55 °C



PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{9-16} max. 13,2 V

Temperatures

Storage temperature T_{stg} -20 to +80 °C

Operating ambient temperature T_{amb} -20 to +55 °C

CHARACTERISTICS at $V_{9-16} = 12$ V; $T_{amb} = 25$ °C

Supply voltage range V_{9-16} typ. 12 V
10,8 to 13,2 V

Voltage gain of chrominance (R-Y) signal channel

$V_{11-16} = 50$ mV; $f = 4,43$ MHz; video gain = 20x G_{11-3} typ. 17,5

Voltage gain of luminance (Y) channel

$V_{1-16}(p-p) = 1$ V (black to white) $G_{1-3;5;7}$ typ. 5

Bandwidth (-3 dB) of luminance channel

from Y input to R.G.B. outputs B typ. 10 MHz

Bandwidth (-3 dB) of chrominance channel

from (R-Y), (B-Y) inputs to R.G.B. outputs B typ. 1 MHz

Ratio of demodulated signals (defined with equal

chrominance input signals and measured at the outputs (pins 3, 5 and 7) (see note 1 below)

$$\frac{V_{(B-Y)}}{V_{(R-Y)}} \left\{ \begin{array}{l} \text{typ. } 1,78 \\ 1,60 \text{ to } 1,96 \end{array} \right.$$

$$\frac{V_{(G-Y)}}{V_{(R-Y)}} \left\{ \begin{array}{l} \text{typ. } 0,85 \\ 0,76 \text{ to } 0,94 \end{array} \right.$$

Input signals

Chrominance input impedance

at $f = 4,43$ MHz; $V_{10-11} = 20$ mV (sinusoidal)
defined as resistance (R) and parallel
capacitance (C)

R typ. 1000 Ω
C < 10 pF

1) These values are chosen to minimise visible errors in flesh tones and of the luminance of the green component. The matrix equation for the derivation of the (G-Y) component is given by $(G-Y) = -0,51 (R-Y) - 0,19 (B-Y)$. (This is derived from the basic colour equation $Y = 0,30 R + 0,59 G + 0,11 B$). Measured at the tube cathodes with 100 V peak-to-peak video drive.

CHARACTERISTICS (continued)Luminance (pin 1)

a. Y signal input blanking level (fixed by TBA560C)	V_{1-16}	typ.	1,5 V 1,4 to 1,8 V
b. Y input signal, black level potential (nominal brightness set by brightness control of TBA560C)	V_{1-16}	typ.	1,7 V
c. Y input black to white amplitude (adjusted by contrast control of TBA560C)	V_{1-16}	typ.	1,0 V

Reference

a. Input impedance defined as resistance (R) and parallel capacitance (C) at $f = 4,43$ MHz	R	typ.	5 k Ω
	C	typ.	5 pF
		<	10 pF
b. Reference input voltage (from TBA540) peak-to-peak value	$V_{15-16(p-p)}; V_{13-16(p-p)}$	typ.	1,0 V 0,5 to 2,0 V
c. Phase shift between reference inputs and chrominance input required to give coincidence at the synchronous demodulators		typ.	10 ⁰

Identification (pin 14)

a. Input voltage for ident. "off"	V_{14-16}	>	6 V
b. Input voltage for ident. "on"	V_{14-16}	<	7 V
c. Input current for ident. "off"	I_{14}	<	0,1 mA
d. Tracking of ident. threshold with a supply variation of $\pm 10\%$ (V_T = threshold voltage)	$\frac{\Delta V_T \times V_{9-16}}{V_T \times \Delta V_{9-16}}$	typ.	1,0

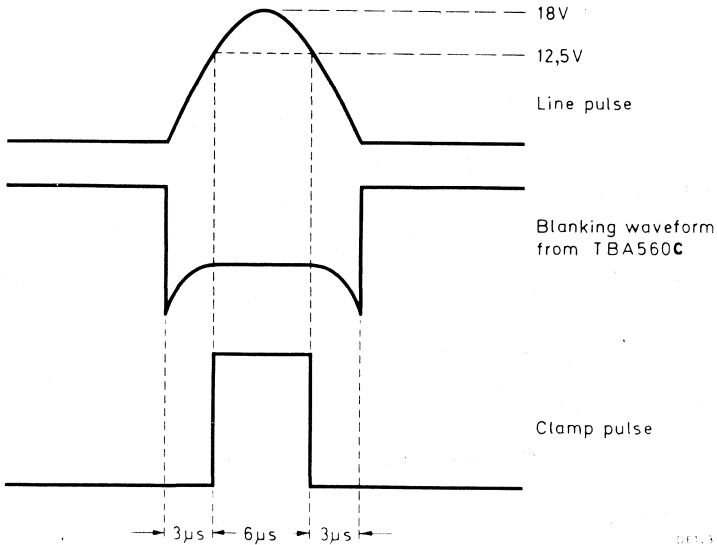
CHARACTERISTICS (continued)

Line pulse

a. Required line pulse input current to clamps and H/2 bistable	I_8	typ.	0,45 mA
			0,3 to 0,6 mA
b. Window level (see note below)	V_{8-16}	typ.	12,5 V
c. Input impedance	R_{8-16}	typ.	1,0 k Ω
			0,6 to 1,4 k Ω

Note

In order to provide a clamp pulse which occurs inside the blanking waveform and free from the edge spikes, it is necessary to window the line pulse at about two thirds of its amplitude



Output signals

R.G.B. outputs (pins 3, 5 and 7)

Blanking level (d. c. value); (nominal blanking at pin 1) $V_{3;5;7-16}$ typ. 2 V

Common mode variation of black level over the temperature range of 40 °C see note below

Note

In order to partially compensate for drift in output stages a negative temperature coefficient to compensate for the variation in the video output transistor has been incorporated.

CHARACTERISTICS (continued)

Blanking to white level output voltage capability of each output amplifier channel (peak-to-peak value)	$V_{3;5;7-16(p-p)}$	6 to 8	V
Difference in clamped blanking level of outputs i. e. R to B to G		<	50 mV
Differential drift of clamped output blanking levels over temperature range of 40 °C		<	25 mV
Residual 4, 43 MHz signal at R.G.B. outputs (peak-to-peak values)	red	<	150 mV
	blue	<	300 mV
<u>H/2 output (pin 12)</u>			
H/2 square wave output amplitude (peak-to-peak value)	$V_{12-16(p-p)}$	>	3,0 V ¹⁾
		typ.	3,5 V

APPLICATION NOTES

- For alternative applications in a simple decoder circuit, it must be possible to trigger the bistable so that it runs in the correct ident. phase means of an a. c. coupled, 2 V peak-to-peak square wave derived from the a. p. c. loop in the reference generator circuit. (The normal input line timebase pulse would still be applied in order to provide clamp pulses).
- Input impedance of output amplifier (BF337) (Expressed as parallel resistance and capacitance):

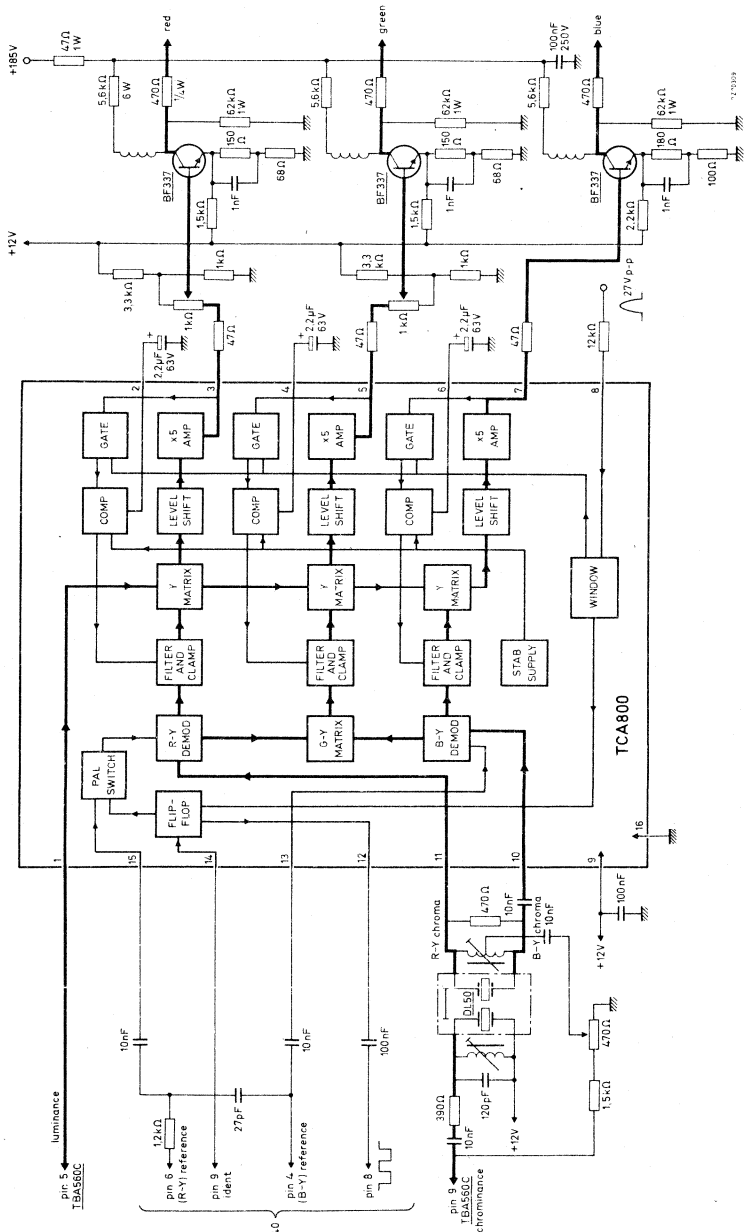
R (typ.) 5 k Ω

C (typ.) 80 pF

The above values are given for suitable design of output stages i. e. emitter follower with 5 mA current capability.

¹⁾ H/2 measured when loaded by TBA540 i. e. 3 k Ω load.

BLOCK DIAGRAM



DOUBLE BALANCED MODULATOR/DEMODULATOR

The TCA820 is a monolithic integrated circuit for use at frequencies up to 650 MHz.
Typical applications are:

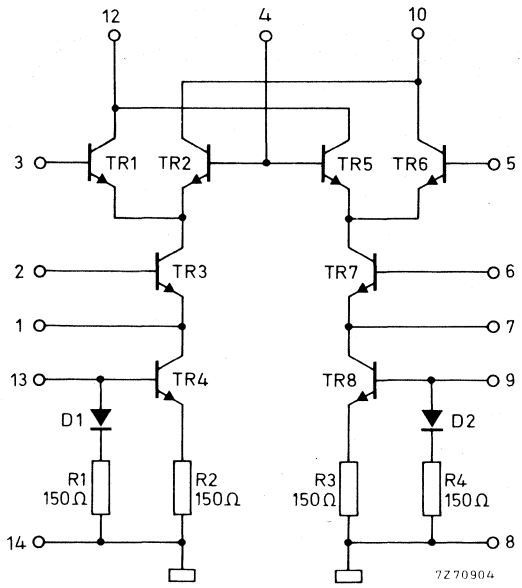
- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities.
The excellent matching and temperature tracking of the transistors in the circuit allow the use of circuit techniques which are not available when using discrete devices.

PACKAGE OUTLINE (see general section)

14-lead; plastic (SOT-43).

CIRCUIT DIAGRAM



Note

Pins 8 and 14 are connected to the substrate.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Voltages

Supply voltage range $V_{10-8}; V_{10-14}; V_{12-8}; V_{12-14}$ 0 to 16 V

Voltages (each transistor)

Collector-substrate voltage (open base and emitter)	V_{CSO}	max.	16	V
Collector-base voltage (open emitter)	V_{CBO}	max.	16	V
Collector-emitter voltage (open base)	V_{CEO}	max.	12	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V

Currents (each transistor)

Emitter current	I_E	max.	10	mA
Base current	I_B	max.	10	mA

RATINGS (continued)Total power dissipation

mounted on a printed-wiring board P_{tot} max. 250 mW

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} 0 to +70 °C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j-a}$ = 220 °C/W

CHARACTERISTICS at $V_{10-8} = V_{10-14} = V_{12-8} = V_{12-14} = 12\text{ V}$; $T_{amb} = 25\text{ °C}$;
measured in test circuit on page 4.

Supply current

$I_{10} + I_{12}$ typ. 2,5 mA
2 to 3 mA

Input signals

carrier signal (r. m. s. value) $V_{3-4(rms)}$; $V_{5-4(rms)}$ typ. 80 mV
< 160 mV

video signal; negative modulated
(peak-to-peak value) $V_{6-2(p-p)}$ typ. 1,0 V
< 1,8 V

Output signal at top sync over 75 Ω

(peak-to-peak value) $V_{10-12(p-p)}$ > 25 mV

Carrier suppression in balanced condition

V_{10-12} > 30 dB
typ. 40 dB

Differential phase

< 8°

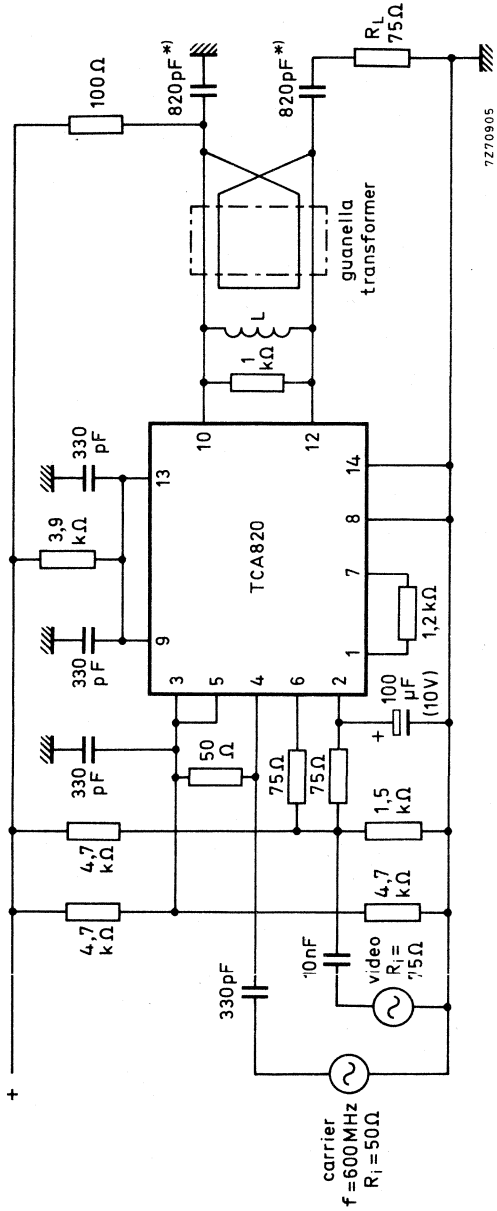
Differential gain

< 16 %

Distortion of video signal

< 5 %

TEST CIRCUIT



7270905

L = aircoil; 3 turns; ϕ 3 mm

*) U.H.F. decoupling capacitor 2212 669 98003

LUMINANCE COMBINATION

The TDA2500 is an integrated luminance circuit for colour television receivers incorporating the following functions:

- luminance amplifier
- linear electronic potentiometer for luminance and chrominance control (contrast control)
- brightness control
- beam current limiter via contrast and brightness
- black level clamp
- matched luminance delay line driver
- emitter follower output for direct drive of the luminance output
- luminance inverter stage (drive for TDA2590)
- blanking or artificial black level insertion

QUICK REFERENCE DATA

Supply voltage	V_{8-16}	typ.	12	V	
Supply current	I_8	typ. see note		mA	
Composite video input voltage (peak-to-peak value)	V_{11-16}	typ.	2,8	V	←
Luminance output (max. contrast; peak-to-peak value)	V_{3-16}	typ.	4,5	V	
Contrast control voltage range	V_{13-16}		2,3 to 4	V	
Inverted video output voltage (peak-to-peak value)	V_{12-16}	typ.	6,8	V	←
Video output voltage for chrominance separation (max. contrast; peak-to-peak value)	V_{10-16}	typ.	4,6	V	←
Brightness control range (black level of luminance signal)	V_{15-16}		0,5 to 2,5	V	
Beam current limiting threshold voltage	V_{14-16}	typ.	0,75	V	←

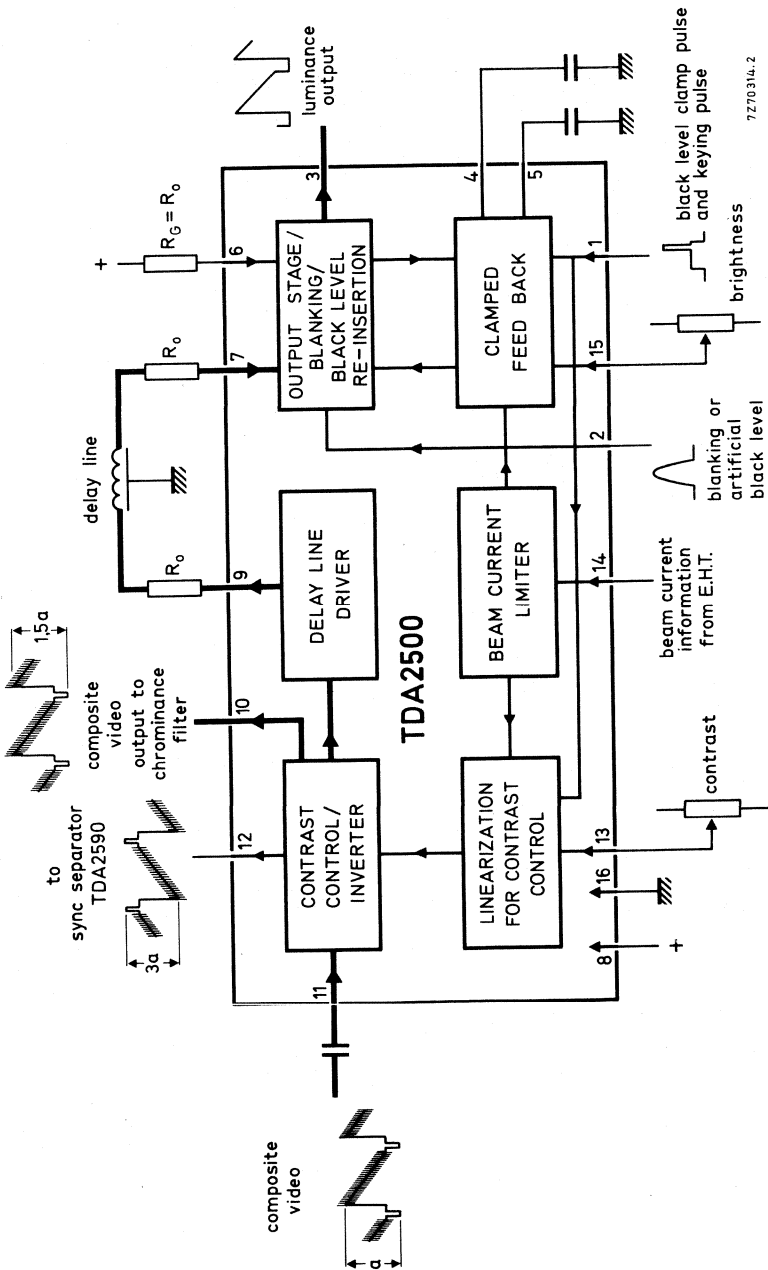
PACKAGE OUTLINES (see general section)

TDA2500 : 16-lead DIL; plastic.

TDA2500Q : 16-lead QIL; plastic.

Note: to be established.

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Supply voltage (pin 8)	V_{8-16}	max.	15 V
Voltage at pin 1	V_{1-16}	max.	15 V
Voltage at pin 13	V_{13-16}	max.	10 V
Voltage at pins 14 and 15	$V_{14-16}; V_{15-16}$	max.	8 V

Currents (positive when flowing into the circuit)

Current at pin 2	$\pm I_2$	max.	2 mA
Current at pin 3; average value peak value	$-I_3(AV)$	max.	15 mA ←
	$-I_3M$	max.	30 mA ←
Current at pin 6	I_6	max.	15 mA
Currents at pins 7, 9, 10 and 12	$I_7, -I_9, -I_{10}, -I_{12}$	max.	10 mA
Current at pin 14	$-I_{14}$	max.	1 mA

Power dissipation

Total power dissipation	P_{tot}	max.	850 mW
-------------------------	-----------	------	--------

Temperatures

Storage temperature	T_{stg}	-20 to +125 °C	←
Operating ambient temperature	T_{amb}	-20 to +60 °C	←

CHARACTERISTICS measured in circuit on page 6

Supply voltage

V_{8-16}	typ.	12 V
		10, 8 to 13, 2 V

The following characteristics are measured at $T_{amb} = 25$ °C; $V_{8-16} = 12$ V; composite video input voltage (peak-to-peak value) $V_{11-16}(p-p) = 1$ V

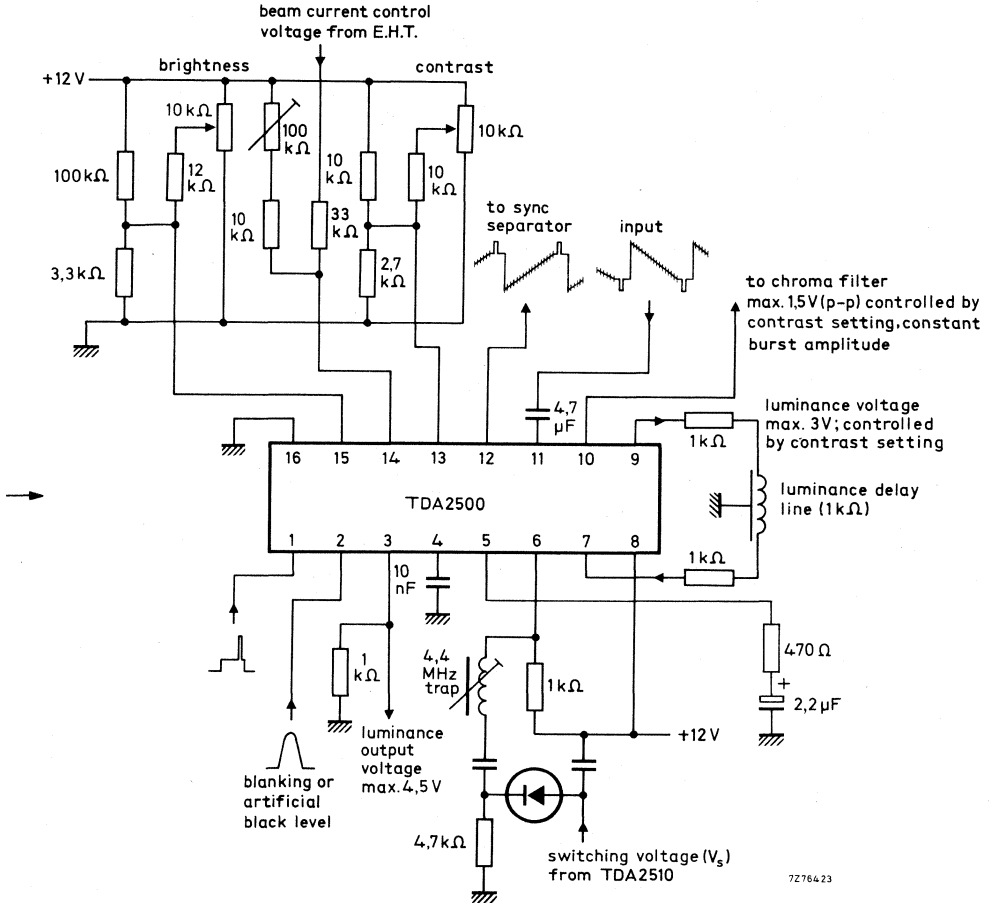
Pre-stages

Delay line driver voltage	V_{9-16}	typ.	3 V ←
Composite video output voltage (max. contrast; peak-to-peak)	$V_{10-16}(p-p)$	typ.	1,5 V
Inverted luminance output voltage (peak-to-peak)	$V_{12-16}(p-p)$	typ.	3 V
Input resistance (pin 11)	R_{11-16}	typ.	12 k Ω
Input capacitance (pin 11)	C_{11-16}	see note on page 1	
Voltage gain between pins 12 and 11	G_{12-11}	typ.	3
Voltage gain at maximum contrast and $V_{1-16} = 0$ between pins 9 and 11	G_{9-11}	typ.	3
	G_{10-11}	typ.	1,5
Voltage gain between pins 10 and 11 at any contrast setting and $V_{1-16} = 2, 3$ to 7 V	G_{10-11}	typ.	1,5 ←

CHARACTERISTICS (continued)

Linearity of V_{9-16} and V_{10-16} at $V_{11-16}(p-p) = 1$ V	m	>	0,9	
→ Frequency response of luminance stage for $f = 0$ to 5 MHz; between pins 9 and 11	d_{9-11}	<	1	dB
between pins 10 and 11	d_{10-11}	<	1	dB
→ Output resistances (emitter follower)	R_{10-16}	typ.	30	Ω
	R_{9-16}	typ.	V_T/I_9	Ω
Contrast control range		typ.	15	dB
Contrast control voltage for maximum contrast	V_{13-16}	typ.	4	V
for -6 dB setting	V_{13-16}	typ.	3	V
for minimum contrast	V_{13-16}	typ.	2,3	V
Contrast control current	I_{13}	typ.	5	μ A
Luminance intermediate stage				
A.C. current gain	$-I_6/I_7$	typ.	3	
Linearity of current gain at $I_7(p-p) = 1$ mA	m	>	0,9	
→ Frequency response of current gain for $f = 0$ to 5 MHz; between pins 6 and 7	d_{6-7}	<	1	dB
Control current at $V_{5-16} = 0$; $V_{7-16} = 0,5$ V	I_7	<	2	mA
→ Control current at $V_{5-16} = 9,5$ V; $I_7 = 0$	I_6	<	4,5	mA
Luminance output stage				
→ Output voltage range (the linearity of the voltage gain $V_{3-16}/V_{6-16} > 0,9$)	V_{3-16}		0,6 to 6	V
→ Frequency response of voltage gain for $f = 0$ to 5 MHz; between pins 3 and 6	d_{3-6}	<	1	dB
Output resistance (pin 3)	emitter follower			
→ Blanking level at luminance output	V_{3-16}	typ.	0,15	V
Clamp level reinsertion at luminance output	V_{3-16}	typ.	1,5	V
Brightness control via clamping circuit				
Brightness control voltage				
at min. brightness	V_{15-16}	typ.	0,5	V
at nom. brightness	V_{15-16}	typ.	1,5	V
at max. brightness	V_{15-16}	typ.	2,5	V
Black level at luminance output				
at min. brightness	V_{3-16}	typ.	0,5	V
at nom. brightness	V_{3-16}	typ.	1,5	V
at max. brightness	V_{3-16}	typ.	2,5	V

APPLICATION INFORMATION



CHROMINANCE COMBINATION

The TDA2510 is an integrated chrominance amplifier circuit for colour television receivers incorporating the following functions:

- chrominance amplifier with a. c. c.
- control voltage amplifier
- burst separator
- colour killer and colour killer voltage detector
- linear electronic potentiometer for saturation control
- Schmitt trigger for colour killer
- chrominance delay line driver stage
- colour burst output stage

QUICK REFERENCE DATA

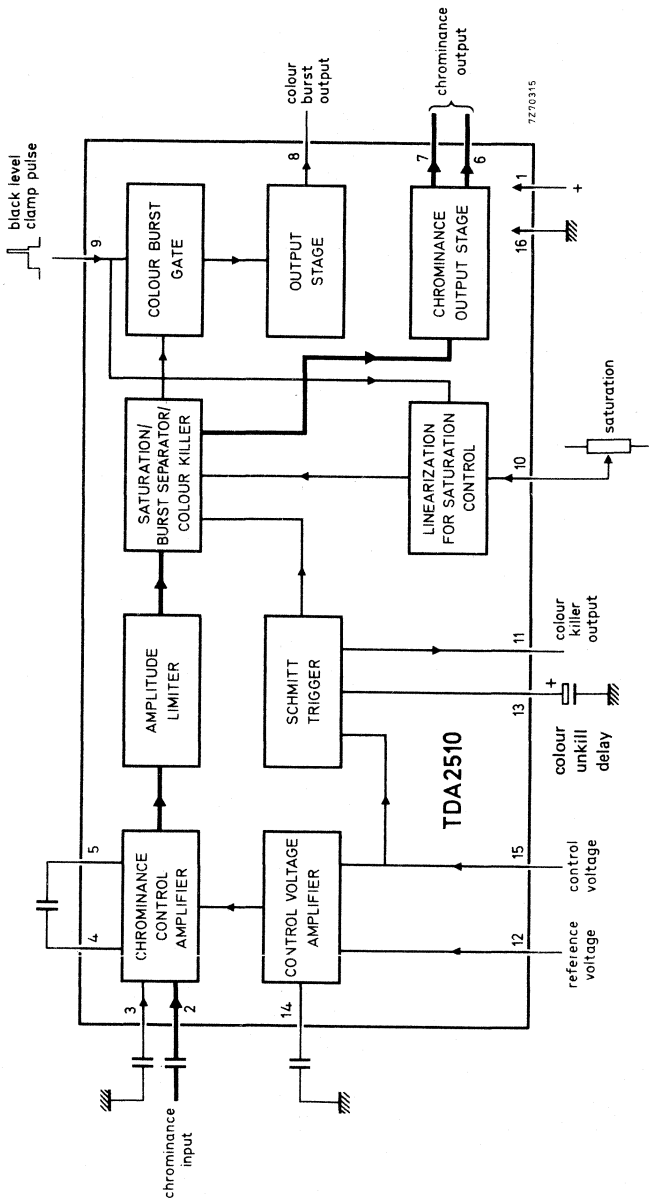
Supply voltage	V_{1-16}	typ. 12 V
Input signal (colour bars) peak-to-peak value	$V_{2-16(p-p)}$	typ. 100 mV
Output signal (colour bars) peak-to-peak value	$V_{7-16(p-p)}$	typ. 0,5 V
Burst signal output peak-to-peak value	$V_{8-16(p-p)}$	typ. 0,5 V

PACKAGE OUTLINES (see general section)

TDA2510 : 16-lead DIL; plastic.

TDA2510Q : 16-lead QIL; plastic.

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage (pin 1) V_{1-16} max. 15 V

Power dissipation

Total power dissipation P_{tot} max. 500 mW

Temperatures

Storage temperature T_{stg} -20 to +125 °C ←

Operating ambient temperature T_{amb} -20 to +60 °C ←

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C

Chrominance input signal

Input voltage (symmetrical or asymmetrical)
colour bars (peak-to-peak value) $V_{2-16(p-p)}$ typ. 100 mV

Input voltage range V_{2-16} 10 to 200 mV ←

Input impedance $|Z_{2-16}|$ > 2 kΩ

Burst signal output (emitter follower)

D.C. voltage V_{8-16} typ. 9 V

Output signal (peak-to-peak value) $V_{8-16(p-p)}$ typ. 0,5 V 1) ←

Limiting level of output signal (peak-to-peak value) $V_{8-16(p-p)}$ typ. 1,5 V ←

Chrominance output signal (without burst)

D.C. voltage V_{6-16} typ. 7 V

Output signal (colour bars)
at nominal saturation (see note 2) and
maximum contrast (peak-to-peak value) $V_{6-16(p-p)}$ typ. 0,5 V

Signal-to-noise ratio S/N > 50 dB

Saturation control range +6 to -50 dB

Phase angle compared to burst output
at nom. saturation $\Delta\phi_B$ < ±5°

Phase angle shift during saturation control
range +6 to -50 dB $\Delta\phi_C$ < ±5° ←

Collector current of output transistor I_7 < 20 mA

1) Kept constant by a.c.c. circuit.

2) Nominal saturation is defined as maximum saturation -6 dB.

CHARACTERISTICS (continued)

Collector voltage of output transistor
at $P_{tot\ max} = 100\ mW$

$V_{7-16} < 20\ V$

Control voltage amplifier input

Reference voltage

V_{12-16} typ. 7 V

Control voltage

V_{12-15} typ. $V_{12-16} - 1,5\ V$

Input impedance

$|Z_{15-16}| > 500\ k\Omega$

Linearization for saturation input

Linear part of control curve

V_{10-16} 1,75 to 4 V

Threshold voltage for 50 dB suppression

$V_{10-16} >$ typ. 1,6 V
1,75 V

Adjustment voltage behaviour for higher
chrominance output voltage

positive-going

Input impedance

$|Z_{9-16}|$ typ. 10 k Ω

Colour killer input at pin 15

Input voltage for : colour on
for : colour off

$V_{15-16} < 5,7\ V$
 $V_{15-16} > 6,0\ V$

Signal suppression at colour off

$> 50\ dB$

Colour killer output

Switching voltage for : colour on
for : colour off

V_{11-16} typ. V_{1-16} V
 $V_{11-16} < 0,5\ V$

Internal resistance

R_i typ. 10 k Ω

Collector current of output transistor

$I_{11} < 10\ mA$

Burst gating and blanking pulse

Burst gating and blanking pulse
(positive or negative)

$\pm V_{9-16}$ 1 to 4 V

Input impedance

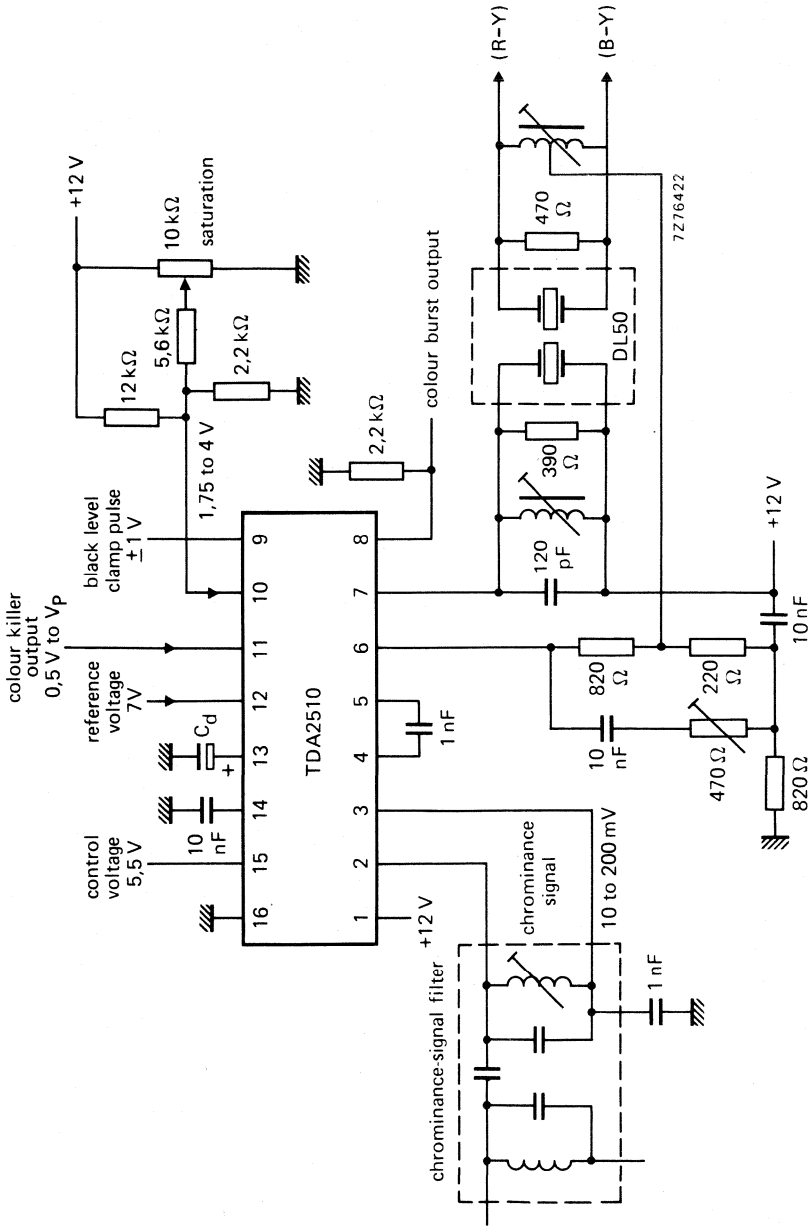
$|Z_{9-16}|$ typ. 1 k Ω

Colour killer

Colour unkill delay; depends on C_d
(see circuit on page 5)

t_d typ. 24 ms/ μF

APPLICATION INFORMATION



COLOUR DEMODULATOR COMBINATION

The TDA2520 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a stage to obtain chrominance signal control (a. c. c.) and an a. c. c. reference level
- a colour killer and identification signal detector
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch
- PAL flip-flop
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier-signals at the outputs.

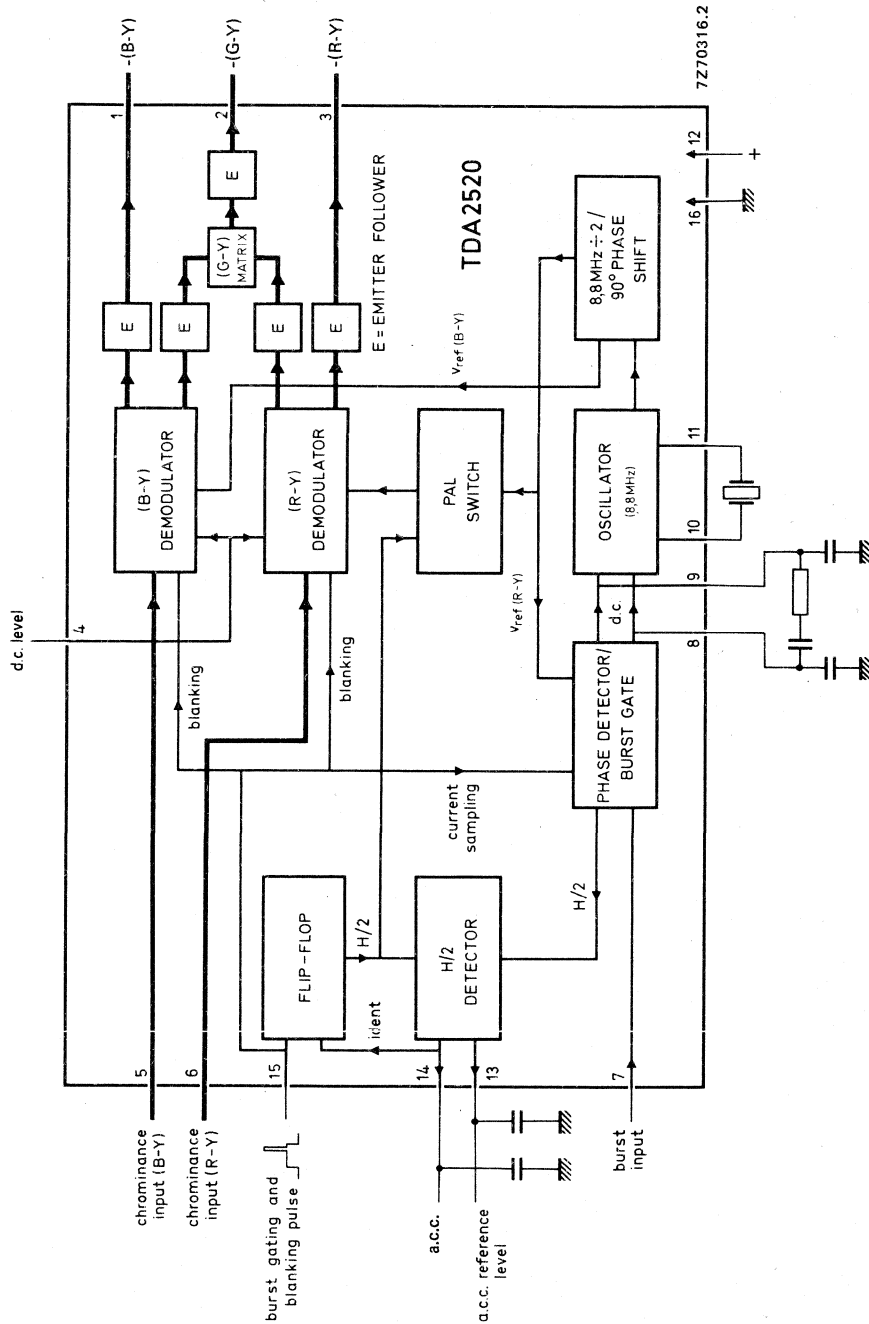
QUICK REFERENCE DATA				
Supply voltage		V_{12-16}	typ.	12 V
Supply current		I_{12}	typ.	40 mA
Colour difference output signals peak-to-peak values				
	-(R-Y)	$V_{3-16(p-p)}$	>	2,4 V
	-(G-Y)	$V_{2-16(p-p)}$	>	1,35 V
	-(B-Y)	$V_{1-16(p-p)}$	>	3 V
Impedance of colour difference signal outputs			typ.	250 Ω

PACKAGE OUTLINES (see general section)

TDA2520 : 16-lead DIL; plastic.

TDA2520Q : 16-lead QIL; plastic.

BLOCK DIAGRAM



7Z70316.2

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{12-16} max. 14 V

Power dissipation

Total power dissipation P_{tot} max. 600 mW

Temperatures

Storage temperature T_{stg} -20 to +125 °C

Operating ambient temperature T_{amb} -20 to +60 °C

CHARACTERISTICS at $V_{12-16} = 12$ V; $T_{amb} = 25$ °C

Demodulator part

Ratio of demodulated signals

B - Y/R - Y: $\frac{V_{1-16}}{V_{3-16}}$ typ. 1,78

G - Y/R - Y: $\frac{V_{2-16}}{V_{3-16}}$ typ. 0,85 ¹⁾

G - Y/R - Y: $\frac{V_{2-16}}{V_{3-16}}$ typ. 0,17 ²⁾

Colour difference output signals ³⁾
peak-to-peak values

-(R - Y)	$V_{3-16(p-p)}$	>	2,4	V
-(G - Y)	$V_{2-16(p-p)}$	>	1,35	V
-(B - Y)	$V_{1-16(p-p)}$	>	3	V

Impedance of colour difference
signal outputs

$ Z_{3-16} $	typ.	250	Ω
$ Z_{2-16} $	typ.	250	Ω
$ Z_{1-16} $	typ.	250	Ω

H/2 ripple at R - Y output (peak-to-peak value) < 10 mV

Blanking and keying pulse

burst keying: active for V_{15-16} > 7,5 V
inactive for V_{15-16} < 6,5 V

blanking: active for V_{15-16} > 2 V
inactive for V_{15-16} < 1 V

¹⁾ The demodulators are driven by a chrominance signal of equal amplitude for the (R - Y) and the (B - Y) components. The phase of the (R - Y) chrominance signal equals the phase of the (R - Y) reference signal.
The same holds for the (B - Y) signals.

²⁾ As under note 1, but the phase of the (R - Y) reference signal reversed.

³⁾ The d. c. level of the colour difference outputs can be adjusted from 6 to 10 V at pin 4.

CHARACTERISTICS (continued)

Reference part

Colour burst (peak-to-peak value)	V ₇₋₁₆ (p-p)	typ.	0,5 V
Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency		<	±5°
Overall holding range with typical crystal	Δf	typ.	±500 Hz
A. C. C. reference output voltage	V ₁₃₋₁₆	typ.	7 V
A. C. C. voltage at 0,5 V peak-to-peak burst at correct phase with zero burst	V ₁₄₋₁₆ V ₁₄₋₁₆	typ. typ.	5,5 V 7,0 V
Oscillator input resistance	R ₁₁₋₁₆	typ.	270 Ω
Oscillator input capacitance	C ₁₁₋₁₆	see note	
Oscillator output resistance	R ₁₀₋₁₆	typ.	200 Ω

Note : to be established.

COLOUR DEMODULATOR COMBINATION

The TDA2522 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a.c.c. detector and amplifier
- a colour killer
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch and PAL flip-flop with internal identification
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier signals at the outputs

QUICK REFERENCE DATA

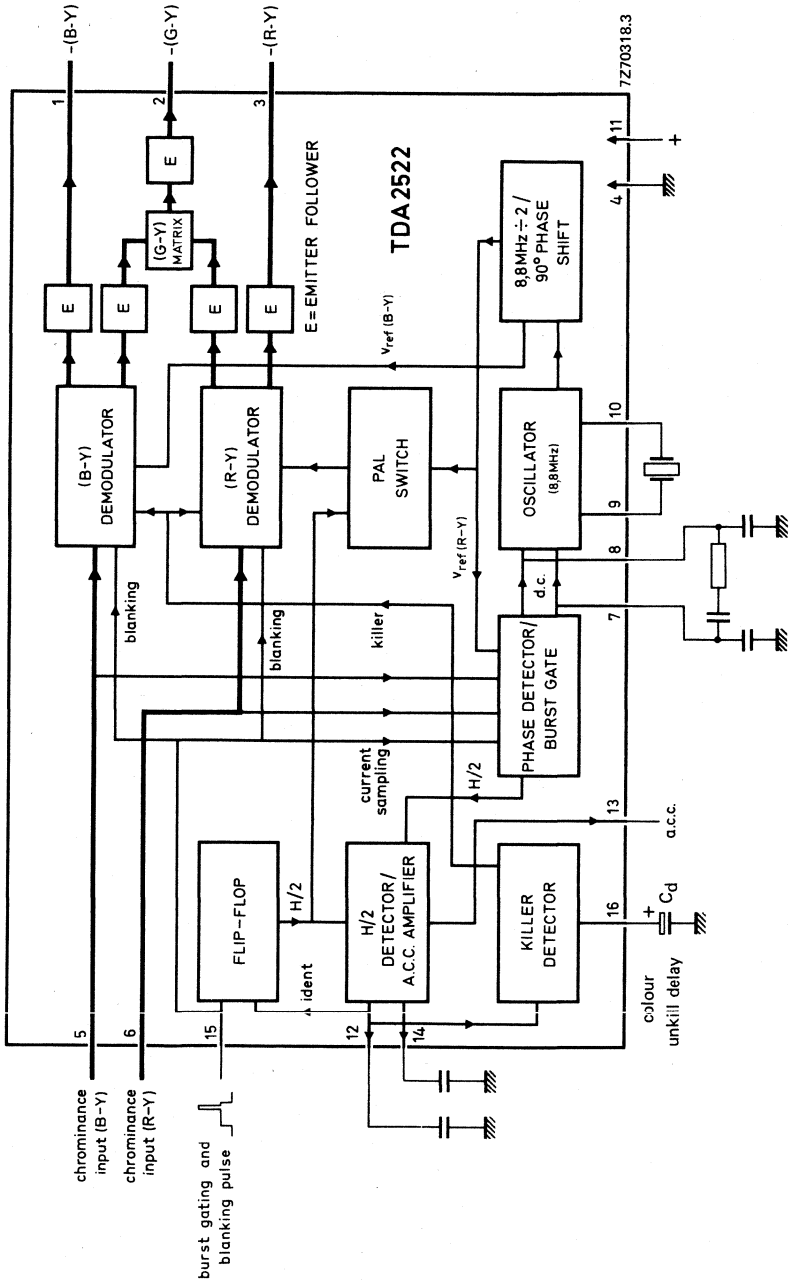
Supply voltage		V_{11-4}	typ.	12	V
Supply current		I_{11}	typ.	40	mA
Colour difference output signals peak-to-peak values; for the following input signals	-(R-Y)	$V_{3-4(p-p)}$	>	2, 4	V
	-(G-Y)	$V_{2-4(p-p)}$	>	1, 35	V
	-(B-Y)	$V_{1-4(p-p)}$	>	3	V
Chrominance input signal (including burst) peak-to-peak value	R-Y	$V_{6-4(p-p)}$		500	mV
	B-Y	$V_{5-4(p-p)}$		350	mV
Impedance of colour difference signal outputs			typ.	250	Ω

PACKAGE OUTLINES (see general section)

TDA2522 : 16-lead DIL; plastic.

TDA2522Q : 16-lead QIL; plastic.

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-4}	max.	14	V
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature	T_{stg}	-20 to +125		°C
Operating ambient temperature	T_{amb}	-20 to +60		°C

CHARACTERISTICS at $V_{11-4} = 12$ V; $T_{amb} = 25$ °C

Demodulator part

Ratio of demodulated signals

B-Y/R-Y:	$\frac{V_{1-4}}{V_{3-4}}$	typ.	1,78	
G-Y/R-Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,85	1)
G-Y/R-Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,17	2)

Colour difference output signals

peak-to-peak values; for the following input signals

-(R-Y)	$V_{3-4}(p-p)$	>	2,4	V
-(G-Y)	$V_{2-4}(p-p)$	>	1,35	V
-(B-Y)	$V_{1-4}(p-p)$	>	3	V

Chrominance input signal (including burst) peak-to-peak value; note 3

R-Y	$V_{6-4}(p-p)$	500	mV
B-Y	$V_{5-4}(p-p)$	350	mV

Impedance of colour difference signal outputs

$ Z_{3-4} $	typ.	250	Ω
$ Z_{2-4} $	typ.	250	Ω
$ Z_{1-4} $	typ.	250	Ω

H/2 ripple at R-Y output (peak-to-peak value)

< 10 mV

Blanking and keying pulse

 burst keying: active for
 inactive for

V_{15-4}	>	7,5	V
V_{15-4}	<	6,5	V

 blanking: active for
 inactive for

V_{15-4}	>	2	V
V_{15-4}	<	1	V

1) The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal.
 The same holds for the (B-Y) signals.

2) As under note 1, but the phase of the (R-Y) reference signal reversed.

3) Colour bar with 75% saturation.

CHARACTERISTICS (continued)

Reference part

Phase difference between reference and burst signals for ± 400 Hz deviation of crystal frequency		<	$\pm 5^\circ$	
Overall holding range with typical crystal	Δf	typ.	± 500	Hz
Burst signal input at keying pulse width of $4 \mu s$ (peak-to-peak value)	V _{5-6(p-p)}	typ.	0,25	V 1)
Oscillator input resistance	R ₁₀₋₄	typ.	270	Ω
Oscillator input capacitance	C ₁₀₋₄	typ.	note 2	pF
Oscillator output resistance	R ₉₋₄	typ.	200	Ω
A.C.C. reference voltage	V ₁₂₋₄	typ.	7	V
A.C.C. voltage at 0,25 V peak-to-peak burst at correct phase :	V ₁₄₋₄	typ.	5,5	V
with zero burst :	V ₁₄₋₄	typ.	7,0	V
A.C.C. amplifier output voltage range at $\pm I_{13} < 200 \mu A$	V ₁₃₋₄		0,5 to 5	V
Colour killer				
Via pin 14				
Colour off	V ₁₄₋₄	>	6	V
Colour on	V ₁₄₋₄	<	5,6	V
Alternatively via pin 16				
Colour off	V ₁₆₋₄	>	7	V
Colour on	V ₁₆₋₄	<	5	V
Colour unkill delay	t _d	typ.	20	ms/ μF 3)

1) The amplitude of the burst is kept constant by a.c.c. action, but depends linearly on the keying pulse width.

2) To be established.

3) The delay depends on the value of C_d.

COLOUR DEMODULATOR COMBINATION

The TDA2523 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a. c. c. detector and amplifier
- a colour killer
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch and PAL flip-flop with internal identification
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier signals at the outputs

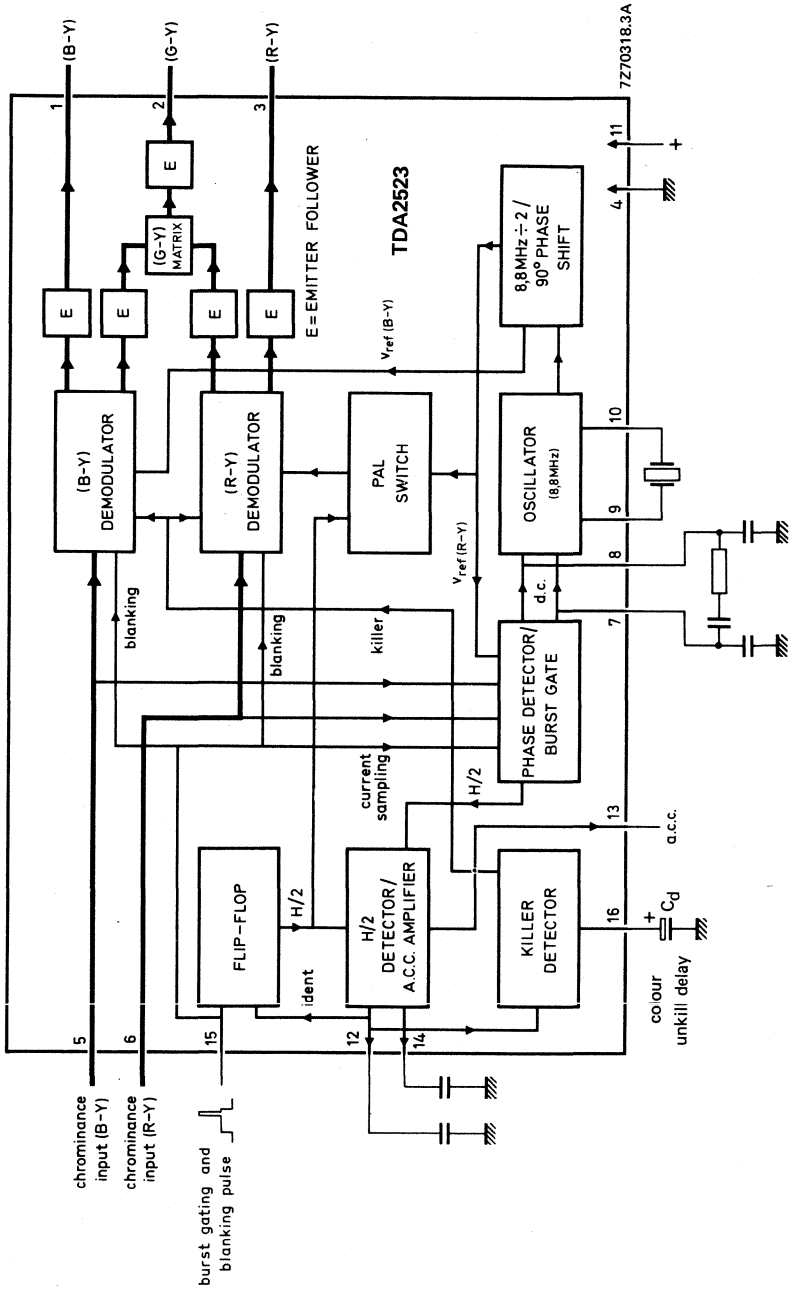
QUICK REFERENCE DATA

Supply voltage		V ₁₁₋₄	typ.	12	V
Supply current		I ₁₁	typ.	40	mA
Colour difference output signals peak-to-peak values; for the following input signals	(R-Y)	V _{3-4(p-p)}	>	2,4	V
	(G-Y)	V _{2-4(p-p)}	>	1,35	V
	(B-Y)	V _{1-4(p-p)}	>	3	V
Chrominance input signal (including burst) peak-to-peak value	R-Y	V _{6-4(p-p)}		500	mV
	B-Y	V _{5-4(p-p)}		350	mV
Impedance of colour difference signal outputs			typ.	250	Ω

PACKAGE OUTLINES (see general section)

TDA2523 : 16-lead DIL; plastic.

TDA2523Q : 16-lead QIL; plastic.



BLOCK DIAGRAM

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-4}	max.	14	V
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature	T_{stg}		-20 to +125	°C
Operating ambient temperature	T_{amb}		-20 to +60	°C

CHARACTERISTICS at $V_{11-4} = 12$ V; $T_{amb} = 25$ °C**Demodulator part**

Ratio of demodulated signals

B - Y/R - Y:	$\frac{V_{1-4}}{V_{3-4}}$	typ.	1,78	
G - Y/R - Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,85	1)
G - Y/R - Y:	$\frac{V_{2-4}}{V_{3-4}}$	typ.	0,17	2)

Colour difference output signals

peak-to-peak values; for the following input signals

(R - Y)	$V_{3-4(p-p)}$	>	2,4	V
(G - Y)	$V_{2-4(p-p)}$	>	1,35	V
(B - Y)	$V_{1-4(p-p)}$	>	3	V

Chrominance input signal (including burst) peak-to-peak value; note 3

R - Y	$V_{6-4(p-p)}$		500	mV
B - Y	$V_{5-4(p-p)}$		350	mV

Impedance of colour difference signal outputs

$ Z_{3-4} $	typ.	250	Ω
$ Z_{2-4} $	typ.	250	Ω
$ Z_{1-4} $	typ.	250	Ω

H/2 ripple at R - Y output (peak-to-peak value)

	<	10	mV
--	---	----	----

Blanking and keying pulse

burst keying: active for
inactive for

V_{15-4}	>	7,5	V
V_{15-4}	<	6,5	V

blanking: active for
inactive for

V_{15-4}	>	2	V
V_{15-4}	<	1	V

1) The demodulators are driven by a chrominance signal of equal amplitude for the (R - Y) and the (B - Y) components. The phase of the (R - Y) chrominance signal equals the phase of the (R - Y) reference signal.

The same holds for the (B - Y) signals.

2) As under note 1, but the phase of the (R - Y) reference signal reversed.

3) Colour bar with 75% saturation.

CHARACTERISTICS (continued)

Reference part

Phase difference between reference and burst signals for ± 400 Hz deviation of crystal frequency		<	$\pm 5^\circ$	
Overall holding range with typical crystal	Δf	typ.	± 500	Hz
Burst signal input at keying pulse width of $4 \mu s$ (peak-to-peak value)	V _{5-6(p-p)}	typ.	0,25	V ¹⁾
Oscillator input resistance	R ₁₀₋₄	typ.	270	Ω
Oscillator input capacitance	C ₁₀₋₄	typ.	note 2	pF
Oscillator output resistance	R ₉₋₄	typ.	200	Ω
A.C.C. reference voltage	V ₁₂₋₄	typ.	7	V
A.C.C. voltage at 0,25 V peak-to-peak burst at correct phase :	V ₁₄₋₄	typ.	5,5	V
with zero burst :	V ₁₄₋₄	typ.	7,0	V
A.C.C. amplifier output voltage range at $\pm I_{13} < 200 \mu A$	V ₁₃₋₄		0,5 to 5	V
Colour killer				
Via pin 14				
Colour off	V ₁₄₋₄	>	6	V
Colour on	V ₁₄₋₄	<	5,6	V
Alternatively via pin 16				
Colour off	V ₁₆₋₄	>	7	V
Colour on	V ₁₆₋₄	<	5	V
Colour unkill delay	t _d	typ.	20	ms/ μF ³⁾

¹⁾ The amplitude of the burst is kept constant by a.c.c. action, but depends linearly on the keying pulse width.

²⁾ To be established.

³⁾ The delay depends on the value of C_d.

RGB MATRIX PREAMPLIFIER

The TDA2530 is an integrated RGB matrix preamplifier for colour television receivers, incorporating a matrix preamplifier for RGB cathode drive of the picture tube with clamping circuits. The three channels have the same layout to ensure identical frequency behaviour.

This integrated circuit has been designed to be driven from the TDA2522 synchronous demodulator and oscillator IC.

QUICK REFERENCE DATA

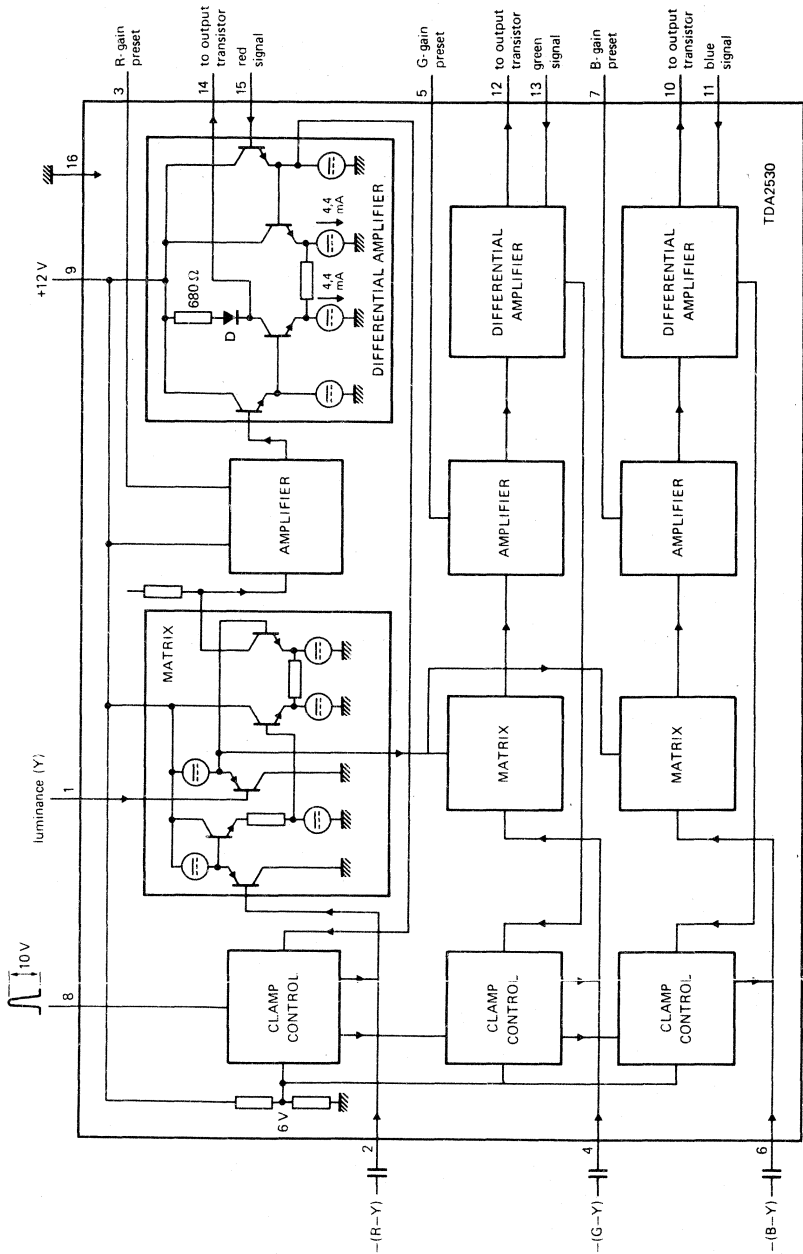
Supply voltage	V ₉₋₁₆	typ.	12 V
Operating ambient temperature range	T _{amb}		-20 to +60 °C
Luminance input resistance	R ₁₋₁₆	>	100 kΩ
Input current of colour difference inputs	I _{2, I₄, I₆}	typ.	2 μA
during clamping	I _{2, I₄, I₆}		-0, 2 to +0, 2 mA
Clamping pulse input current	-I ₈	<	20 μA
Gain of RGB preamplifiers	G	typ.	0 dB
Gain d. c. adjustment range	ΔG	typ.	±3 dB
Gain of error amplifier (conductance)		typ.	20 mA/V
Input current of feedback inputs	I _{11, I₁₃, I₁₅}	typ.	2 μA
Output current swing	I _{10, I₁₂, I₁₄}		-4, 4 to +4, 4 mA

PACKAGE OUTLINES (see general section)

TDA2530 : 16-lead DIL; plastic.

TDA2530Q : 16-lead QIL; plastic.

BLOCK DIAGRAM



7775189

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Supply voltage (pin 9)	V_P (V ₉₋₁₆) max.	15 V
Pin 1	V_{1-16}	0 to V_P
Pins 3, 5 and 7	$V_{3;5;7-16}$	0 to V_P
Pins 2, 4 and 6	$V_{2;4;6-16}$	0 to V_P
Pin 8	V_{8-16} max.	V_P
Pin 10	V_{10-16}	V_{11-16} to $V_P + 3$ V
Pin 12	V_{12-16}	V_{13-16} to $V_P + 3$ V
Pin 14	V_{14-16}	V_{15-16} to $V_P + 3$ V
Pins 11, 13 and 15	$V_{11;13;15-16}$	0,3 V_P to V_P

Current

Pin 8	$-I_8$ max.	1 mA
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Power dissipation

Total power dissipation	P_{tot} max.	1 W
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Temperatures

Storage temperature	T_{stg}	-20 to +125 °C
Operating ambient temperature	T_{amb}	-20 to +60 °C

CHARACTERISTICS at $V_P = 12$ V; $V_{1-16} = 1,5$ V; $T_{amb} = 25$ °C; measured in circuit on page 5.

Current consumption	I_9 typ.	50 mA
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Luminance input

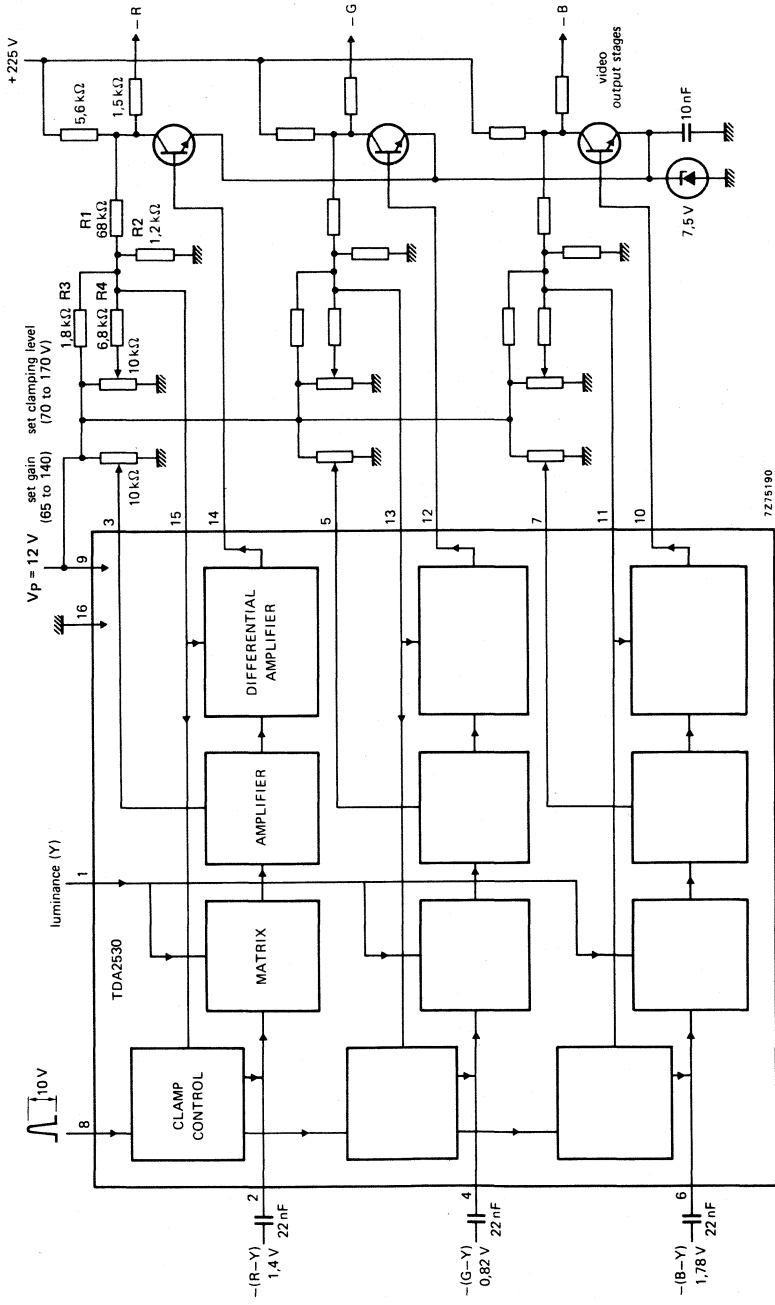
Black level	V_{1-16} typ.	1,5 V
Black-to-white input voltage (peak-to-peak value)	$V_{1-16(p-p)}$ typ.	1,0 V
Input resistance	R_{1-16} >	100 k Ω

Colour difference input

Input signals (peak-to-peak values)	R-Y 1)	$V_{2-16(p-p)}$ typ.	1,4 V
	G-Y 1)	$V_{4-16(p-p)}$ typ.	0,82 V
	B-Y 1)	$V_{6-16(p-p)}$ typ.	1,78 V
Input currents	I_2, I_4, I_6 typ.	2 μ A	
	<	4 μ A	
Input currents during clamping	I_2, I_4, I_6	-0,2 to +0,2 mA	

1) This prescribed order is not mandatory, as all three channels are identical.

APPLICATION INFORMATION



TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2540 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using n-p-n tuners.

It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal

QUICK REFERENCE DATA

Supply voltage	V_{11-13}	typ.	12	V
Supply current	I_{11}	typ.	50	mA
I.F. input voltage at $f = 38,9$ MHz (r. m. s. value)	V_{1-16} (rms)	typ.	100	μ V
Video output voltage	V_{12-13}	typ.	3	V
I.F. voltage gain control range	G_v	typ.	64	dB
Signal-to-noise ratio at $V_i = 10$ mV	S/N	typ.	58	dB
A.F.C. output voltage swing for $\Delta f = 100$ kHz	V_{6-13}	>	10	V

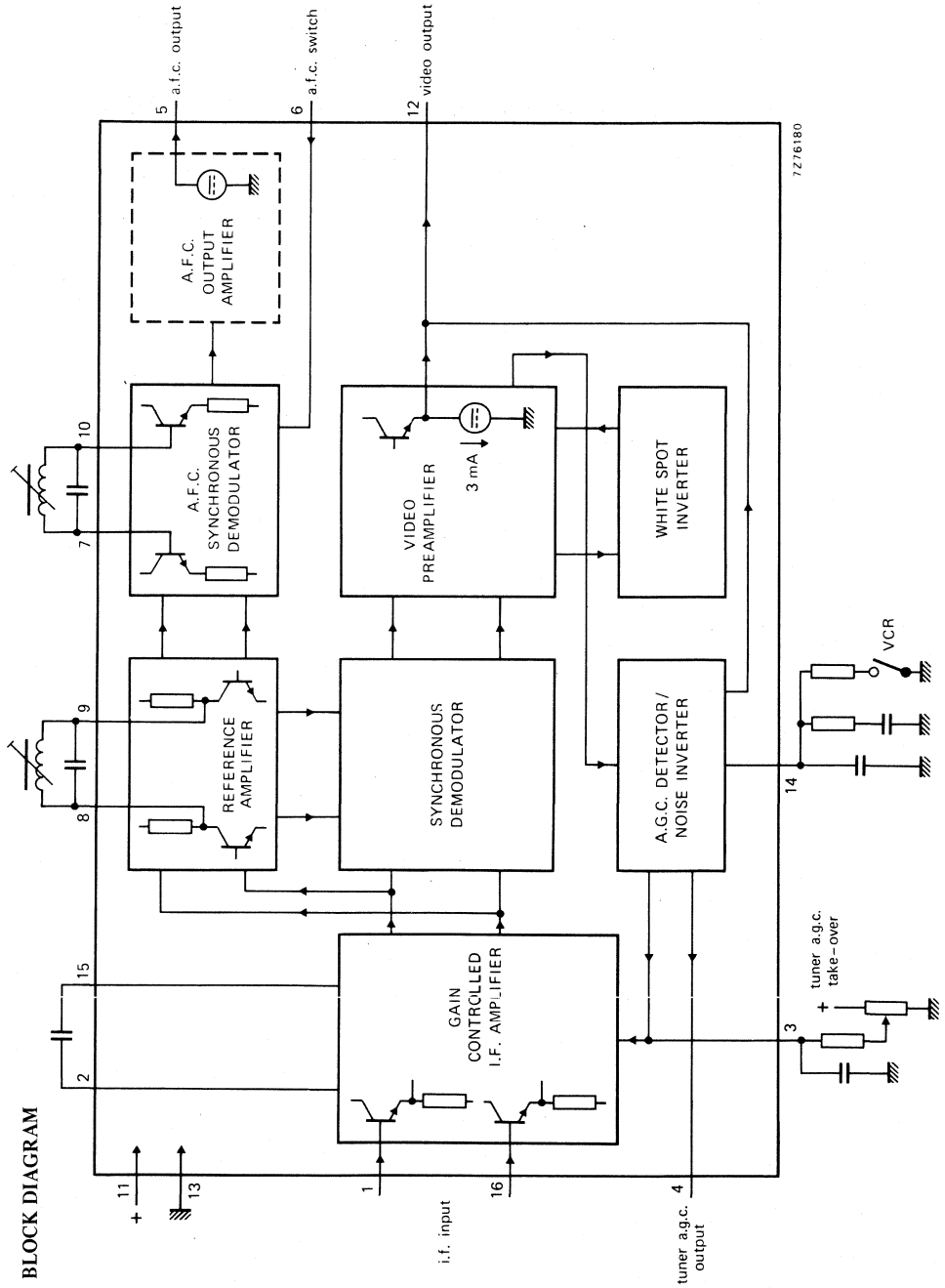
PACKAGE OUTLINES (see general section)

TDA2540 : 16-lead DIL; plastic.

TDA2540Q : 16-lead QIL; plastic.

**TDA2540
TDA2540Q**

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

<u>Supply voltage</u>	V_{11-13}	max. 13,8	V
<u>Tuner a. g. c. voltage</u>	V_{4-13}	max. 12	V
<u>Power dissipation</u>	P_{tot}	max. 900	mW
<u>Temperatures</u>			
Storage temperature	T_{stg}	-55 to +125	°C
Operating ambient temperature	T_{amb}	-25 to +60	°C

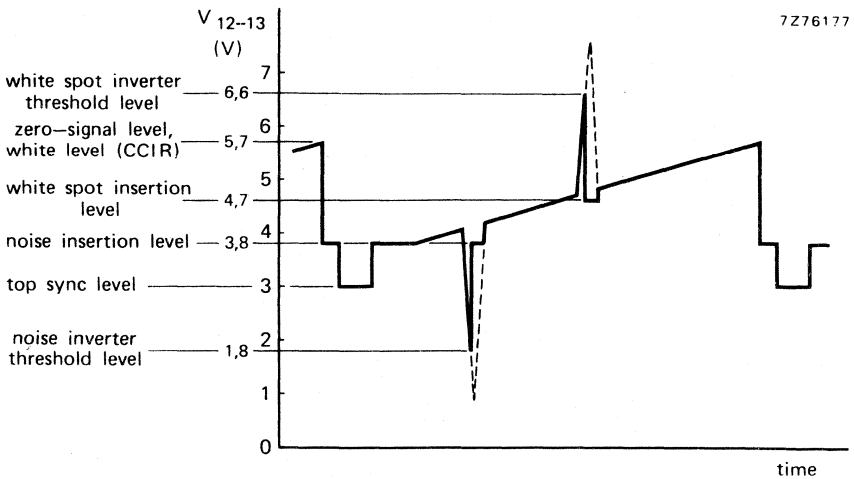
CHARACTERISTICS measured in circuit on page 6

<u>Supply voltage range</u>	V_{11-13}	typ. 12 10, 2 to 13, 8	V V
The following characteristics are measured at $T_{amb} = 25\text{ °C}$; $V_{11-13} = 12\text{ V}$			
I. F. input voltage for onset of a. g. c. at $f = 38,9\text{ MHz}$ (r. m. s. value)	$V_{1-16(rms)}$	typ. 100 < 150	μV μV
Differential input impedance	$ Z_{1-16} $	typ. $2\text{ k}\Omega$ in parallel with 2 pF	
Zero-signal output level	V_{12-13}	typ. $6 \pm 0,3$	V
Top sync output level	V_{12-13}	{ typ. 3,07 2,9 to 3,2	V V
A. F. C. output voltage swing for $\Delta f = 100\text{ kHz}$	V_{6-13}	{ > 10 typ. 11	V V
I. F. voltage gain control range	G_v	typ. 64	dB
Signal-to-noise ratio at $V_i = 10\text{ mV}$	S/N	typ. 58	dB ¹⁾
Bandwidth of video amplifier (3 dB)	B	typ. 6	MHz
Differential gain	dG	typ. 4 < 10	% %
Differential phase	$d\phi$	typ. 20° < 10°	
Carrier signal at video output		typ. 4 < 30	mV mV
2nd harmonic of carrier at video output		typ. 20 < 30	mV mV
Change of frequency at a. f. c. output voltage swing of 10 V	Δf	typ. 100 < 200	kHz kHz

$$1) S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5\text{ MHz}}$$

CHARACTERISTICS (continued)

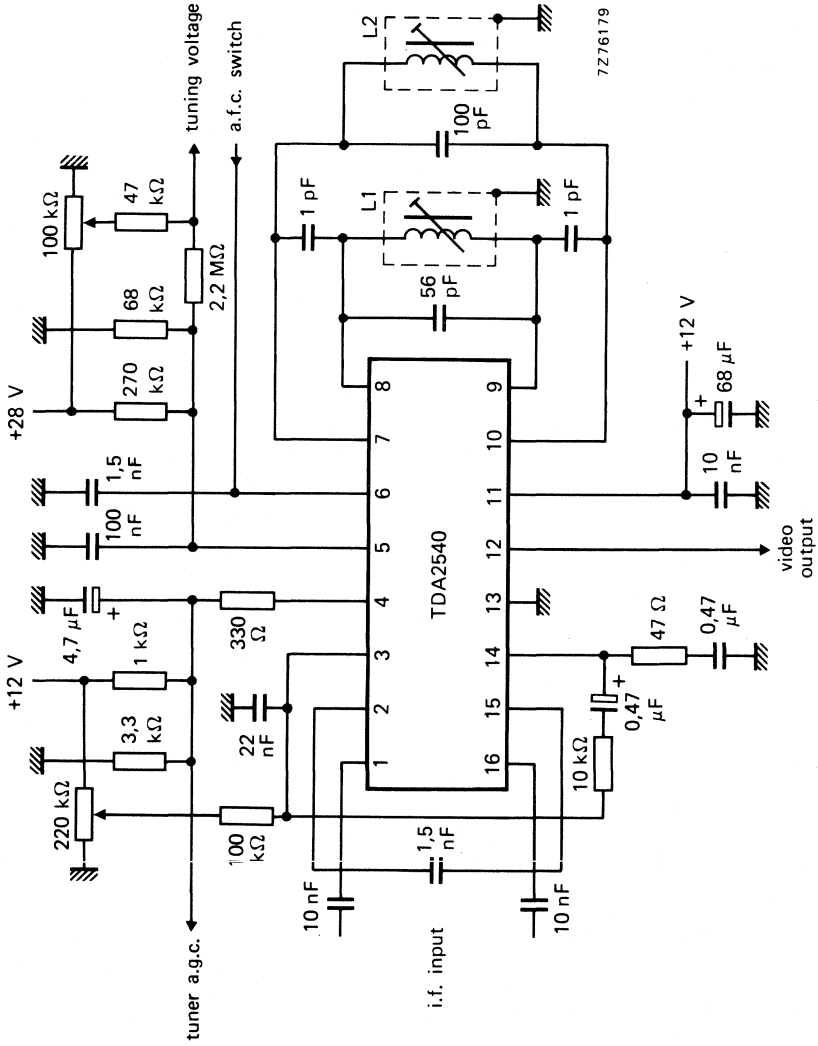
A.F.C. switches off at:	V_{6-13}	<	2,5	V
VCR switches off at:	V_{14-13}	<	1,1	V
White spot inverter threshold level		typ.	6,6	V ¹⁾
White spot insertion level		typ.	4,7	V ¹⁾
Noise inverter threshold level		typ.	1,8	V ¹⁾
Noise insertion level		typ.	3,8	V ¹⁾
Tuner a. g. c. output current range	I_4		0 to 10	mA
Tuner a. g. c. output voltage at $I_4 = 10$ mA	V_{4-13}	<	0,3	V
Tuner a. g. c. output leakage current	I_4	<	15	μ A
$V_{14-13} = 3$ V; $V_{4-13} = 12$ V				



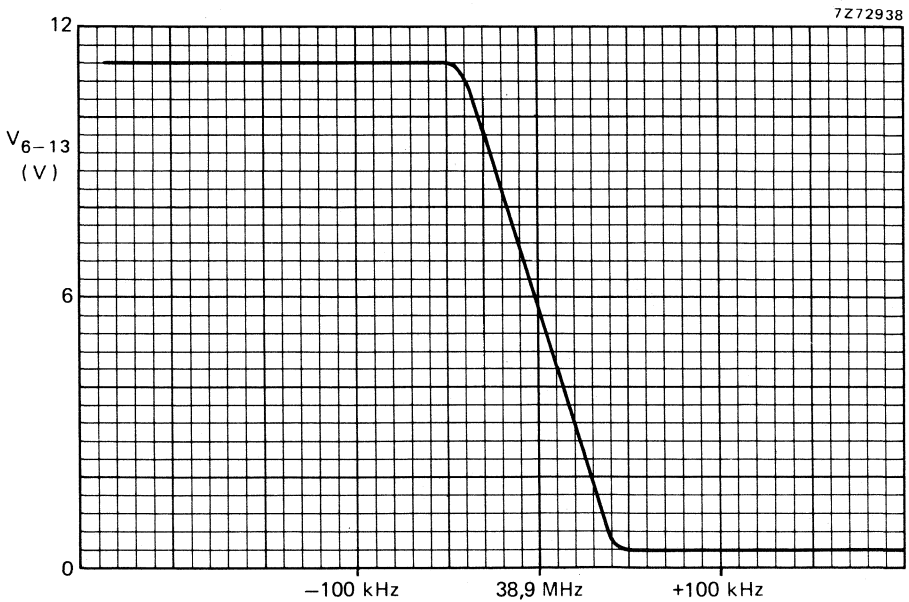
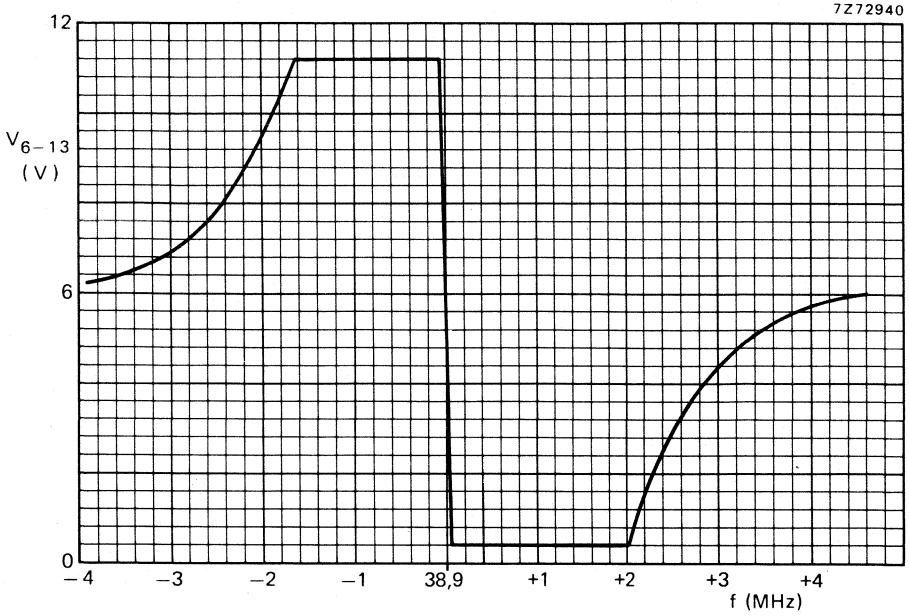
Video output waveform showing white spot and noise inverter threshold levels.

¹⁾ See waveform above.

APPLICATION INFORMATION

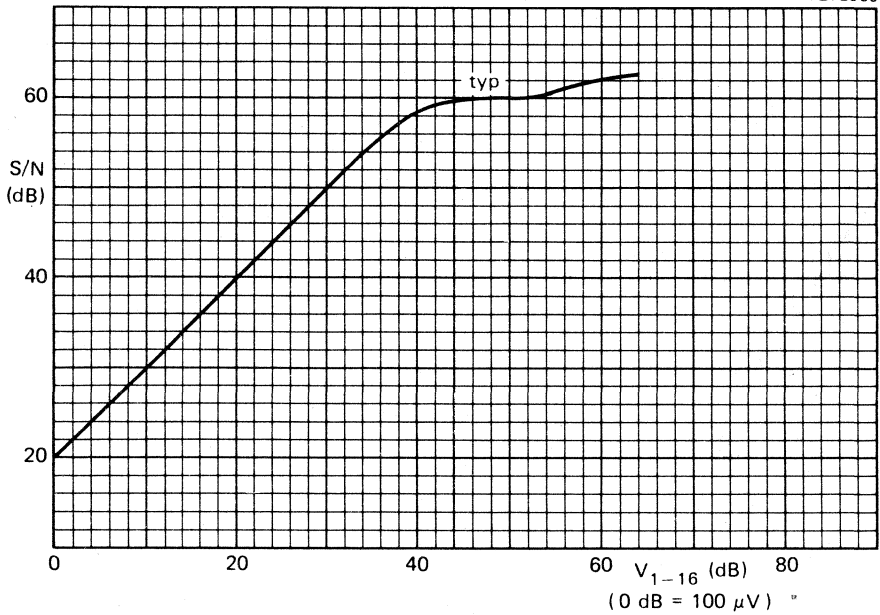


Q of L1 and L2 ≈ 80.



A.F.C. output voltage (V_{6-13}) as a function of the frequency.

7272939



Signal-to-noise ratio as a function of input voltage (V_{1-16}).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2541 is an i. f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.

It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i. f gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a. f. c. circuit which can be switched on/off by a d. c. level, e. g. during tuning
- a. g. c. circuit with **noise gating**
- tuner a. g. c. output (p-n-p tuners)
- VCR switch, which switches off the video output; e. g. for insertion of a VCR playback signal.

QUICK REFERENCE DATA

Supply voltage	V_{11-13}	typ.	12 V
Supply current	I_{11}	typ.	50 mA
I. F. input voltage at $f = 38,9$ MHz (r. m. s. value)	$V_{1-16(\text{rms})}$	typ.	100 μV
Video output voltage	V_{12-13}	typ.	3 V
I. F. voltage gain control range	G_v	typ.	64 dB
Signal-to-noise ratio at $V_i = 10$ mV	S/N	typ.	58 dB
A. F. C. output voltage swing for $\Delta f = 100$ kHz	V_{6-13}	>	10 V

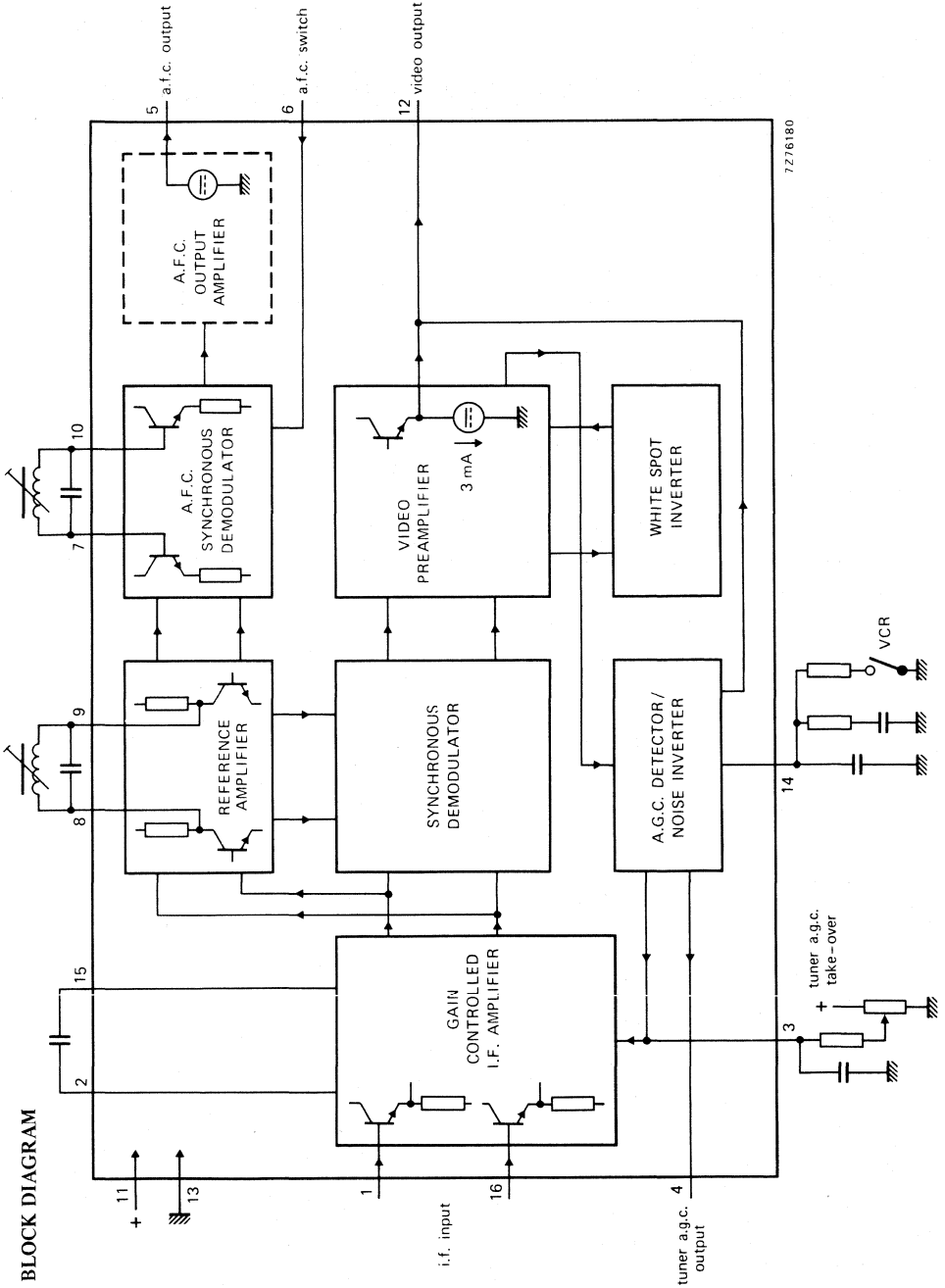
PACKAGE OUTLINES (see general section)

TDA2541 : 16-lead DIL; plastic.

TDA2541Q : 16-lead QIL; plastic.

TDA2541 TDA2541Q

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

<u>Supply voltage</u>	V_{11-13}	max. 13,8	V
<u>Tuner a.g.c. voltage</u>	V_{4-13}	max. 12	V
<u>Power dissipation</u>	P_{tot}	max. 900	mW
<u>Temperatures</u>			
Storage temperature	T_{stg}	-55 to +125	°C
Operating ambient temperature	T_{amb}	-25 to +60	°C

CHARACTERISTICS measured in circuit on page 6

<u>Supply voltage range</u>	V_{11-13}	typ. 12 10,2 to 13,8	V V
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The following characteristics are measured at $T_{amb} = 25\text{ °C}$; $V_{11-13} = 12\text{ V}$

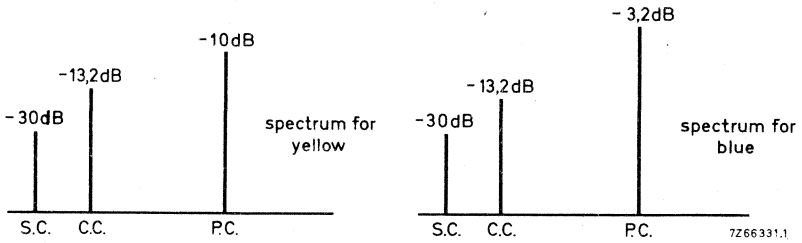
I.F. input voltage for onset of a.g.c. at $f = 38,9\text{ MHz}$ (r. m. s. value)	$V_{1-16(rms)}$	typ. 100 < 150	μV μV
Differential input impedance	$ Z_{1-16} $	typ. 2 k Ω in paral- 1el with 2 pF	
Zero-signal output level	V_{12-13}	typ. $6 \pm 0,3$	V
Top sync output level	V_{12-13}	{ typ. 3,07 2,9 to 3,2	V V
A.F.C. output voltage swing for $\Delta f = 100\text{ kHz}$	V_{6-13}	{ > 10 typ. 11	V V
I.F. voltage gain control range	G_v	typ. 64	dB
Signal-to-noise ratio at $V_i = 10\text{ mV}$	S/N	typ. 58	dB ¹⁾
Bandwidth of video amplifier (3 dB)	B	typ. 6	MHz
Differential gain	dG	typ. 4 < 10	% %
Differential phase	$d\phi$	typ. 2° < 10°	
Carrier signal at video output		typ. 4 < 30	mV mV
2nd harmonic of carrier at video output		typ. 20 < 30	mV mV
Change of frequency at a.f.c. output voltage swing of 10 V	Δf	typ. 100 < 200	kHz kHz

1) $S/N = \frac{V_o \text{ black-to-white}}{V_n(rms) \text{ at } B=5\text{ MHz}}$

CHARACTERISTICS (continued)

Intermodulation at 1, 1 MHz; blue	1)	>	46 dB	
		typ.	60 dB	
	yellow	1)	>	46 dB
		typ.	50 dB	
at 3, 3 MHz	2)	>	46 dB	
		typ.	54 dB	

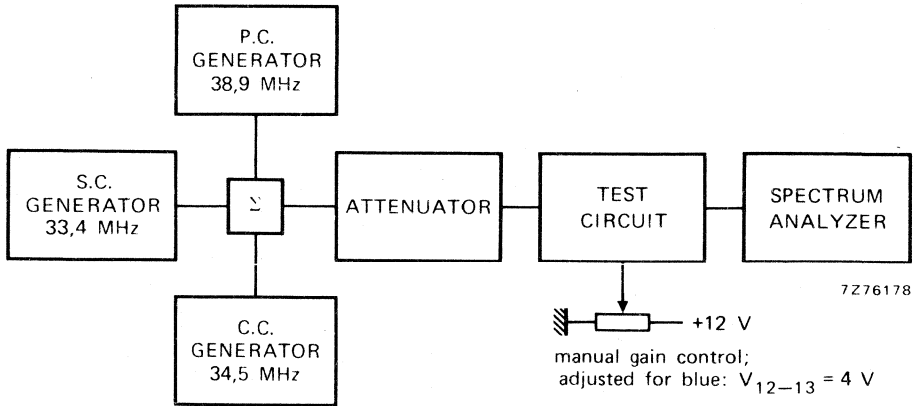
Input conditions for intermodulation measurements:
standard colour bar with 75% contrast



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level

} with respect to top sync level

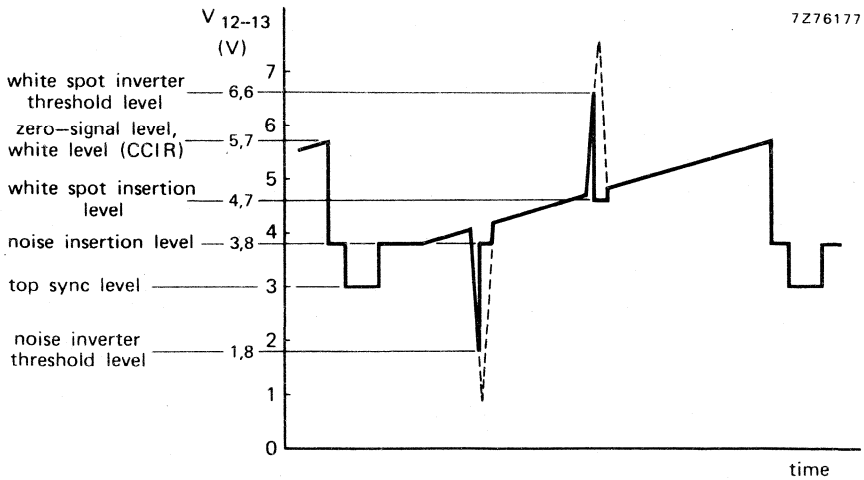
Test set-up for intermodulation



1) $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 1,1 \text{ MHz}} + 3,6 \text{ dB.}$ 2) $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 3,3 \text{ MHz}}$

CHARACTERISTICS (continued)

A.F.C. switches off at:	V_{6-13}	<	2,5 V
VCR switches off at:	V_{14-13}	<	1,1 V
White spot inverter threshold level		typ.	6,6 V ¹⁾
White spot insertion level		typ.	4,7 V ¹⁾
Noise inverter threshold level		typ.	1,8 V ¹⁾
Noise insertion level		typ.	3,8 V ¹⁾
Tuner a. g. c. output current range	I_4		0 to 10 mA
Tuner a. g. c. output voltage at $I_4 = 10$ mA	V_{4-13}	<	0,3 V
Tuner a. g. c. output leakage current $V_{14-13} = 11$ V; $V_{4-13} = 12$ V	I_4	<	15 μ A

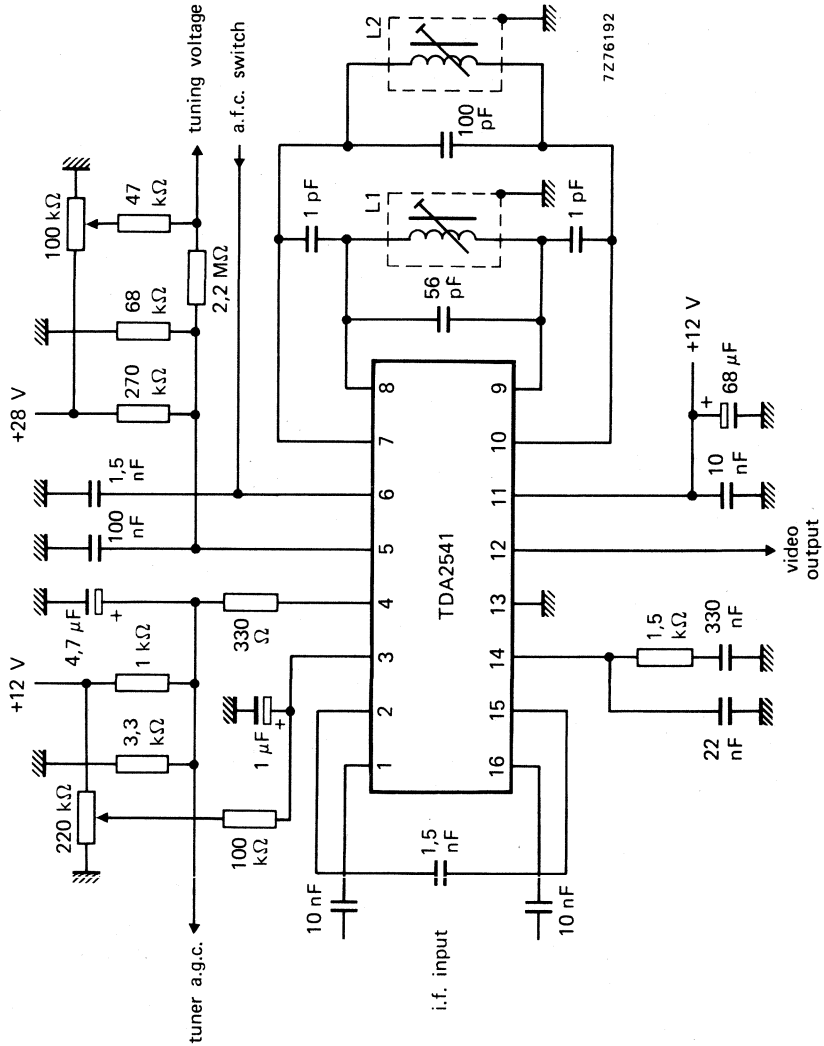


Video output waveform showing white spot and noise inverter threshold levels.

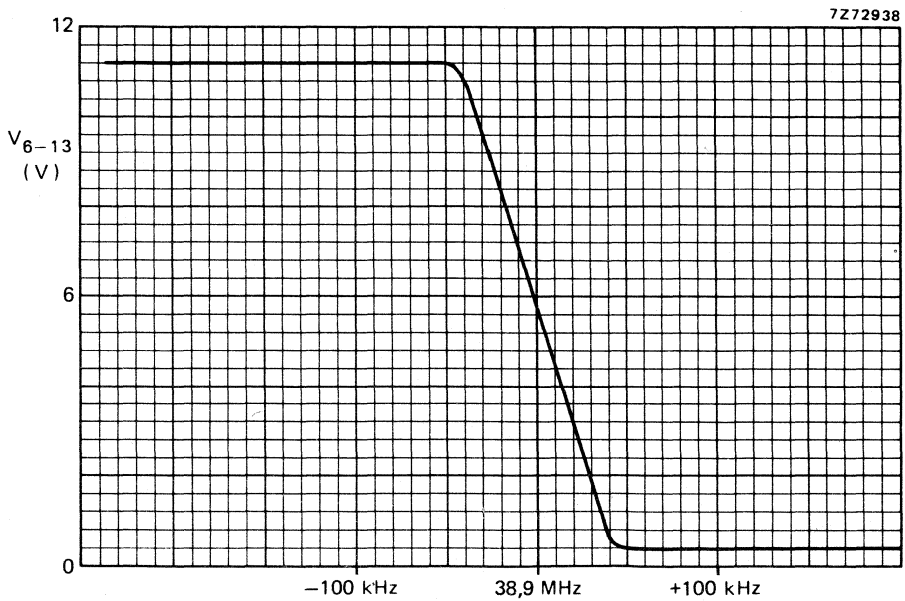
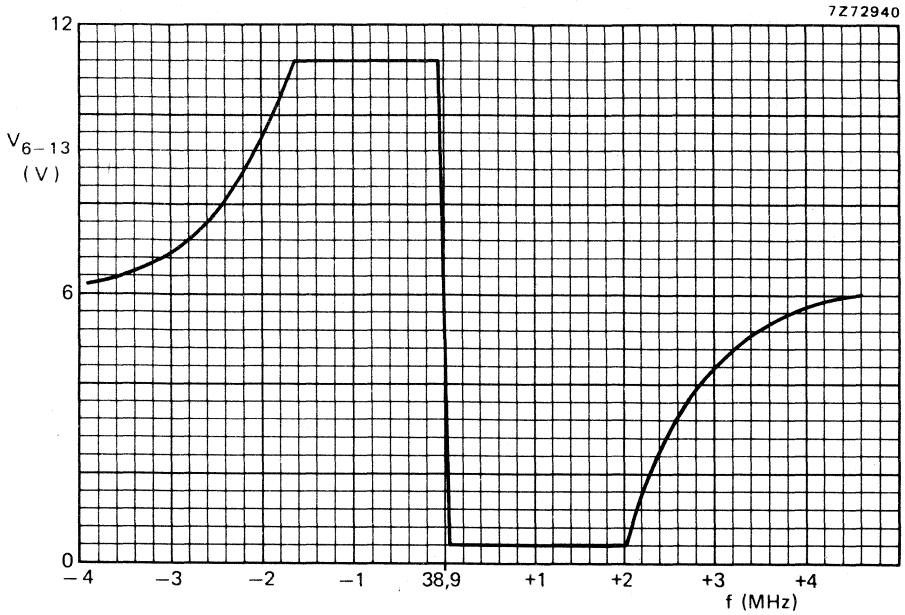
¹⁾ See waveform above.

TDA2541
TDA2541Q

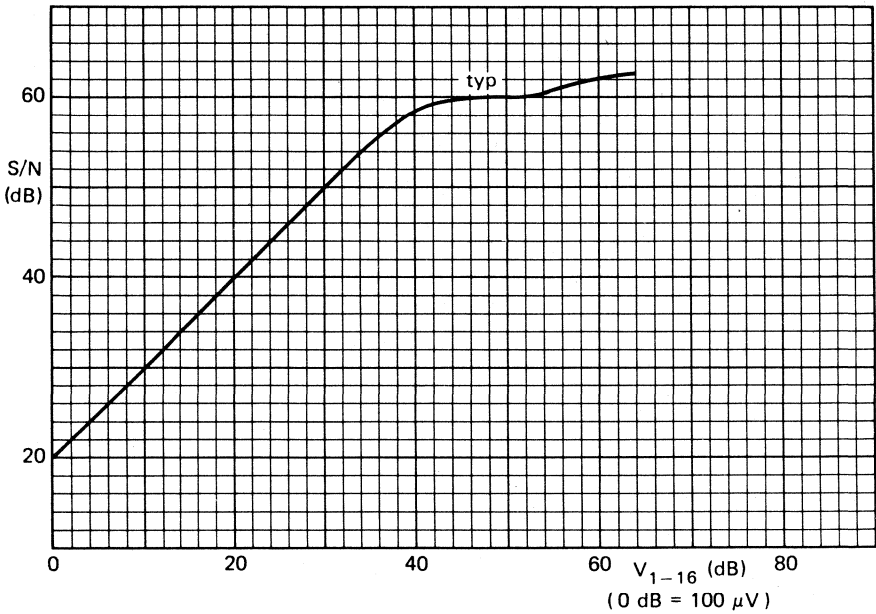
APPLICATION INFORMATION



Q of L1 and L2 ≈ 80



A.F.C. output voltage (V_{6-13}) as a function of the frequency.



Signal-to-noise ratio as a function of input voltage (V_{1-16})

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TDA2560 is a monolithic integrated circuit for use in decoding systems of colour television receivers. The circuit consists of a luminance and chrominance amplifier. The luminance amplifier has a low input impedance so that matching of the luminance delay line is very easy.

It also incorporates the following functions:

- d. c. contrast control;
- d. c. brightness control;
- black level clamp;
- blanking;
- additional video output with positive-going sync.

The chrominance amplifier comprises:

- gain controlled amplifier;
- chrominance gain control tracked with contrast control;
- separate d. c. saturation control;
- combined chroma and burst output, burst signal amplitude not affected by contrast and saturation control;
- the delay line can be driven directly by the IC.

QUICK REFERENCE DATA

Supply voltage	V_{8-5}	typ.	12	V
Supply current	I_8	typ.	45	mA
Luminance signal input current (black-to-white value)	I_{14}	typ.	0,2	mA
Chrominance input signal (peak-to-peak value)	$V_{2-1(p-p)}$		4 to 80	mV
Luminance output signal at nominal contrast (black-to-white value)	V_{10-5}	typ.	3	V
Chrominance output signal at nominal contrast and saturation and 1,25 V peak-to-peak burst output (peak-to-peak value)	$V_{6-5(p-p)}$	typ.	2,5	V
Contrast control range		>	20	dB
Saturation control range		>	20	dB

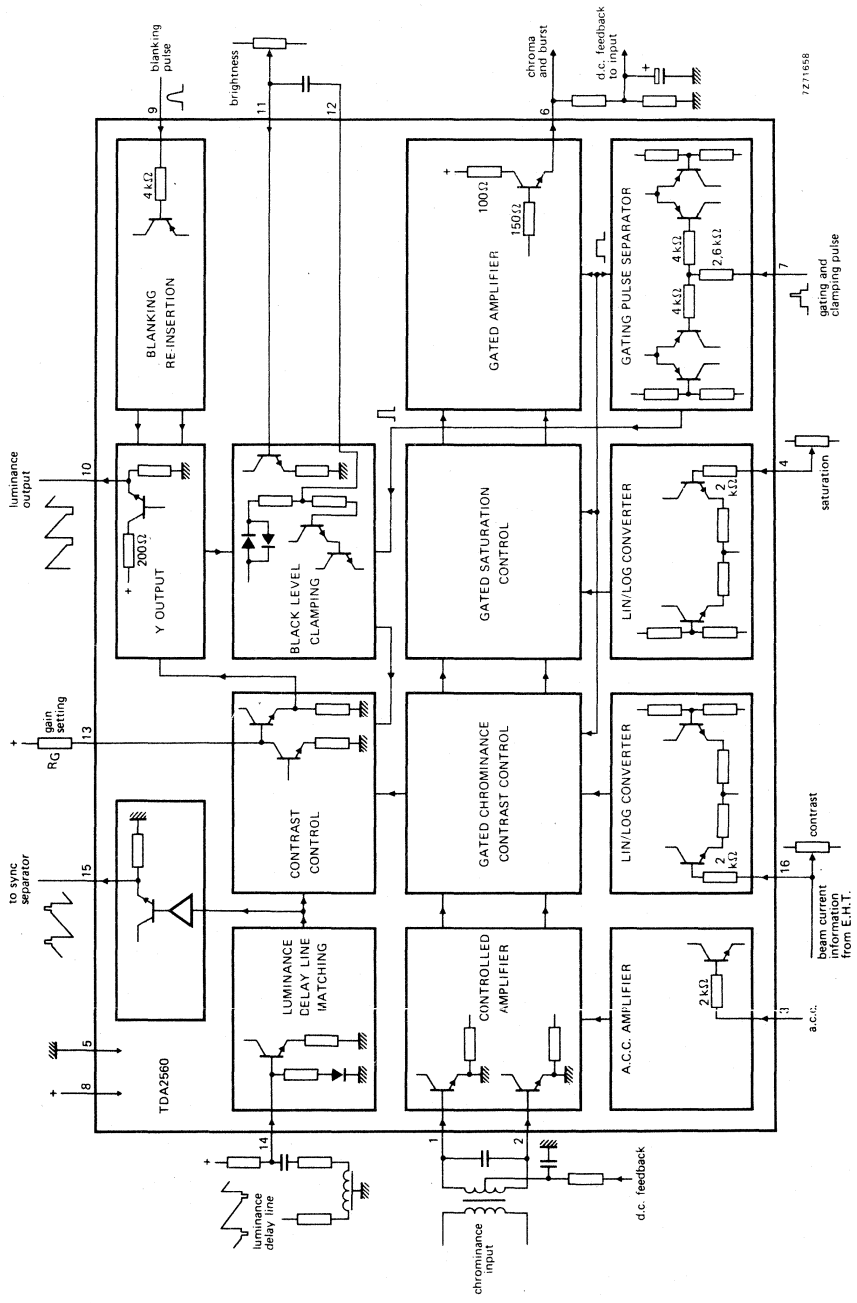
PACKAGE OUTLINES (see general section)

TDA2560 : 16-lead DIL; plastic.

TDA2560Q: 16-lead QIL; plastic.

TDA2560 TDA2560Q

BLOCK DIAGRAM



7271658

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage

Supply voltage V_{8-5} max. 14 V

Power dissipation

Total power dissipation P_{tot} max. 930 mW

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} 0 to +65 °C

CHARACTERISTICS measured in the circuit on page 7

Supply voltage range V_{8-5} typ. 12 V
10 to 14 V

Supply current I_8 typ. 45 mA¹⁾

Allowable hum on supply line (peak-to-peak value) $V_{8-5(p-p)}$ < 100 mV

The following data are measured at $V_{8-5} = 12$ V; $T_{amb} = 25$ °C; $R_G = 2,7$ k Ω

Luminance amplifier

Input signal current; black-to-white value I_{14} typ. 0,2 mA

Input bias current I_{14} typ. 0,25 mA

Input impedance $|Z_{14-5}|$ typ. 150 $\Omega^2)$

Gain (pin 13) see note 1 on page 5

Contrast control range > 20 dB

Contrast control voltage range V_{16-5} (see control curve on page 6)

Contrast control current I_{16} < 8 μ A

Black level range V_{10-5} 1 to 3 V

Brightness control voltage range V_{11-5} typ. 1 to 3 V

Brightness control current I_{11} < 20 μ A³⁾

Black level stability when changing temperature typ. 0,1 mV/°C

Black level stability when changing contrast see page 9 (pin 10)

Bandwidth (-3 dB) B > 5 MHz⁴⁾

1) At a load on pin 6 of 1,5 k Ω , and no load on pins 10 and 15.

2) At an input bias current of 0,25 mA.

3) At $V_{11-5} > 4$ V.

4) At nominal contrast (max. contrast setting -3 dB).

CHARACTERISTICS (continued)

Output voltage (black-to-white value)	V_{10-5}	typ.	3	V
Output voltage (additional; positive-going sync peak-to-peak value)	$V_{15-5(p-p)}$	typ.	3, 4	$V^1)$
Black level clamp pulse (see note 2 on page 5)				
on level	V_{7-5}		7 to V_{8-5}	V
off level	V_{7-5}	<	5	V
Blanking pulse (see note 3 on page 5)				
for 0 V on pin 10: on level	V_{9-5}		2, 5 to 4, 5	V
off level	V_{9-5}	<	1, 5	V
for 1, 5 V on pin 10: on level	V_{9-5}		6 to V_{8-5}	V
off level	V_{9-5}	<	4, 5	V
Chrominance amplifier 2)				
Input signal (peak-to-peak value)	$V_{2-1(p-p)}$		4 to 80	mV
Chrominance output signal at nominal contrast and saturation setting (peak-to-peak value)	$V_{6-5(p-p)}$	typ.	2	$V^3)$
Maximum chrominance output signal	V_{6-5}		4, 6	V
Bandwidth (-3 dB)	B	typ.	6	MHz
Ratio of burst and chrominance at nominal contrast and saturation			see notes 4 and 5 on page 5	
A.C.C. starting voltage (see note 6 on page 5)	V_{3-5}	typ.	1, 2	V
A.C.C. range		>	30	dB
Tracking between luminance and chrominance with contrast control (10 dB control)		typ.	± 1	dB
Saturation control range		>	20	dB
Saturation control voltage range	V_{4-5}	(see control curve on page 6)		
Gating pulse for chrominance amplifier				
on level	V_{7-5}		2, 3 to 5	V
off level	V_{7-5}	<	1	V
width	t_7	>	8	μs
Signal-to-noise ratio at nominal input voltage	S/N	>	46	dB
Phase shift between burst and chrominance		<	5°	

¹⁾ For $I_{14} = 0, 2$ mA (black-to-white value).

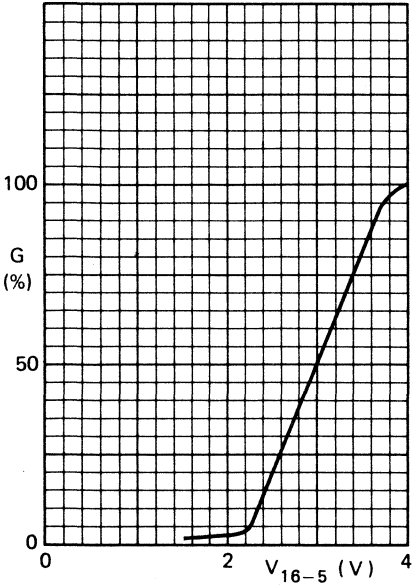
²⁾ All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i. e. burst-to-chrominance ratio is 1:2.

³⁾ At a burst signal of 1 V peak-to-peak; see also notes 4 and 5 on page 5.

NOTES

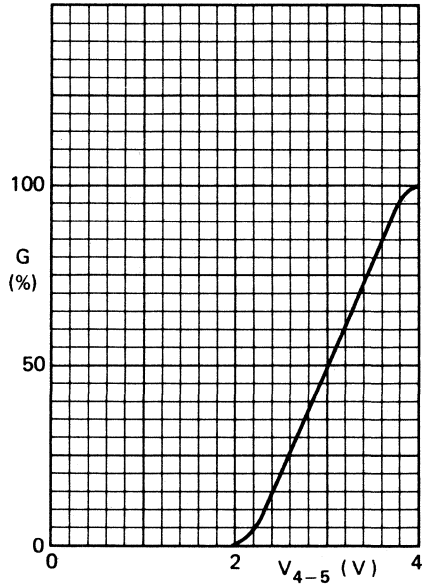
1. The gain of the luminance amplifier can be adjusted, by setting the gain of the contrast control circuit by selection of discrete resistor R_G (see also circuit on page 7). This circuit configuration has been chosen to reduce the spread of the gain to a minimum (main cause of spread is now the spread of the ratio of the delay line matching resistors and the resistor R_G). At $R_G = 2,7 \text{ k}\Omega$ the output voltage at nominal contrast (maximum -3 dB) is 3 V black-to-white for an input current of $0,2 \text{ mA}$ black-to-white.
2. This pulse (pin 7) is used for gating of the chrominance amplifier and black level clamping. The latter function is actuated at a $+7 \text{ V}$ level. The input pulse must have such an amplitude that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above $2,3 \text{ V}$ and switches it back to normal setting when the pulse falls below 1 V .
3. This pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds the $+2,5 \text{ V}$ level the output signal is blanked to a level of about 0 V . When the input exceeds a $+6 \text{ V}$ level a fixed level of typ. $+1,5 \text{ V}$ is inserted in the output signal. This level can be used for clamping purposes.
4. The chrominance and burst signal are both available on this pin (6). The burst signal is not affected by the contrast and saturation control and is kept constant by the a. c. c. circuit of the TDA2522. The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for the insertion losses. This means that the output signal of the TDA2560 is determined by the insertion losses of the delay line. At nominal contrast and saturation setting the ratio of burst to chrominance signal at the output is typically identical to that at the input.
5. Nominal contrast is specified as maximum contrast -3 dB . Nominal saturation is specified as maximum saturation -6 dB .
6. A negative-going control voltage gives a decrease in gain.

7Z72190.1



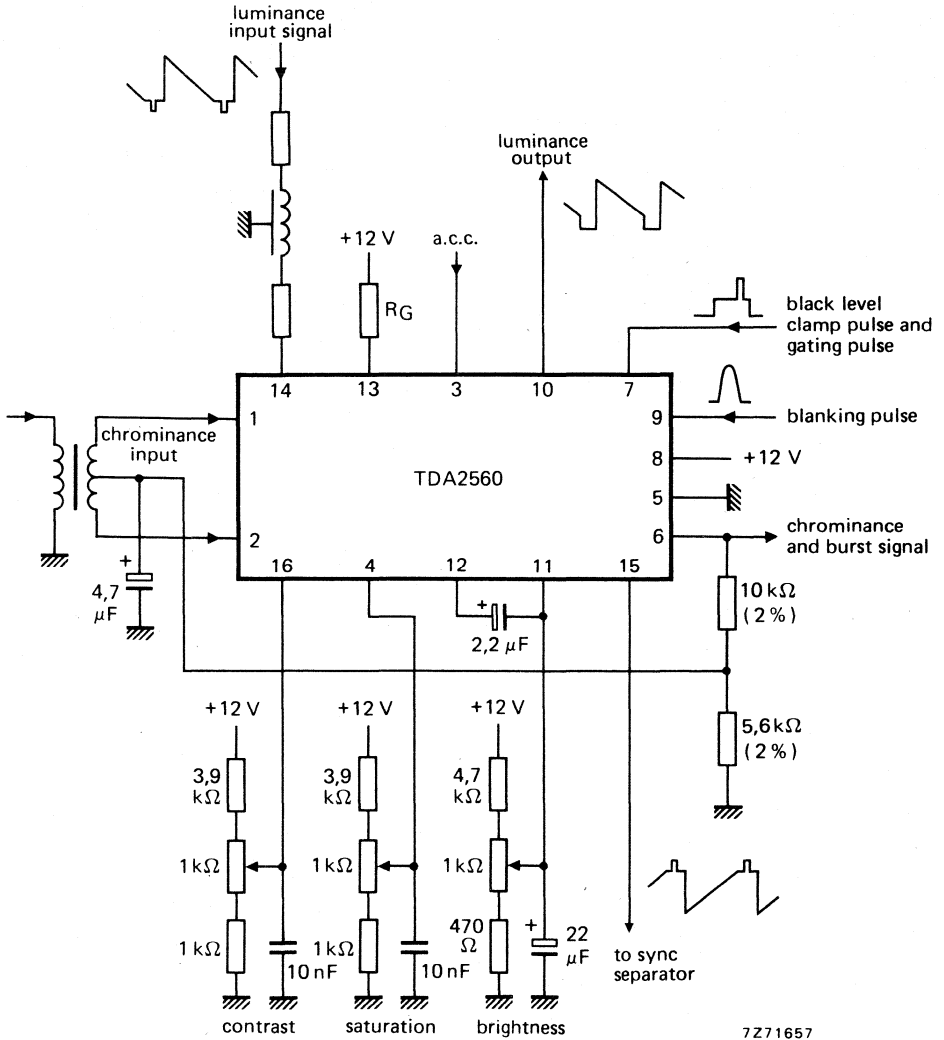
Contrast control of luminance and chrominance amplifier

7Z72189.1



Saturation control of chrominance amplifier

APPLICATION INFORMATION



7271657

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Balanced chrominance input signal (in conjunction with pin 2)

This is derived from the chrominance signal bandpass filter, designed to provide a push-pull input. A signal amplitude of at least 4 mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 will be 3 V.

All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i. e. burst-to-chrominance ratio of input signal is 1 : 2.

2. Chrominance signal input (see pin 1)

3. A. C. C. input

A negative-going potential, starting at +1,2 V, gives a 40 dB range of a. c. c. Maximum gain reduction is achieved at an input voltage of 500 mV.

4. Chrominance saturation control

A control range of +6 dB to >-14 dB is provided over a range of d. c. potential on pin 4 from +2 to +4 V. The saturation control is a linear function of the control voltage.

5. Negative supply (earth)

6. Chrominance signal output

For nominal settings of saturation and contrast controls (max. -6 dB for saturation, and max. -3 dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The a. c. c. circuit of the TDA2522 will hold constant the colour burst amplitude at the input of the TDA2522. As the PAL delay line is situated here between the TDA2560 and TDA2522 there may be some variation of the nominal 1 V peak-to-peak burst output of the TDA2560, according to the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide d. c. negative feedback in the chroma channel via pins 1 and 2.

7. Burst gating and clamping pulse input

A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7 V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide, at least 8 μ s, at the actuating level of 2,3 V.

APPLICATION INFORMATION (continued)

8. +12 V power supply

Correct operation occurs within the range 10 to 14 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels.

9. Flyback blanking input waveform

This pin is used for blanking the luminance amplifier. When the input pulse exceeds the +2,5 V level, the output signal is blanked to a level of about 0 V. When the input exceeds a +6 V level, a fixed level of about 1,5 V is inserted in the output. This level can be used for clamping purposes.

10. Luminance signal output

An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3 V. An external emitter load resistor is not required.

The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12 V supply. At an input bias current I_{14} of 0,25 mA during black level the amplifier is compensated so that no black level shift more than 10 mV occurs at contrast control. When the input current deviates from the quoted value the black level shift amounts to 100 mV/mA.

11. Brightness control

The black level at the luminance output (pin 10) is identical to the control voltage required at this pin. A range of black level from 1 to 3 V may be obtained.

12. Black level clamp capacitor13. Luminance gain setting resistor

The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12 V. Nominal luminance output amplitude is then 3 V black-to-white at pin 10 when this resistor is 2,7 k Ω and the input current is 0,2 mA black-to-white. Maximum and minimum values of this resistor are 3,9 k Ω and 1,8 k Ω .

14. Luminance signal input

A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0,2 mA black-to-white. The luminance signal may be coupled to pin 14 via a d. c. blocking capacitor and, in addition, a resistor employed to give a d. c. current into pin 14 at black level of about 0,25 mA. Alternatively d. c. coupling from a signal source such as the TDA2540 and TDA2541 may be employed.

APPLICATION INFORMATION (continued)

15. Luminance signal output for sync separator purposes

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3,4 V peak-to-peak when the luminance signal input is 0,2 mA black-to-white.

16. Contrast control

With 3 V on this pin the gain of the luminance channel is such that 0,2 mA black-to-white at pin 14 gives a luminance output on pin 10 of 3 V black-to-white. The nominal value of 2,7 k Ω is then assumed for the resistor from pin 13 to the +12 V supply. The variation of control potential at pin 16 from 2 to 4 V gives -17 to +3 dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.

HORIZONTAL SYNCHRONIZATION AND VERTICAL DIVIDER

The TDA2571 is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages.

When supplied with a composite video signal the TDA2571 delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator.
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (divider system).
- Automatic VCR recognition (on VCR identification signal).

QUICK REFERENCE DATA

Supply voltage; horizontal	V_{12-11}	typ.	12	V
vertical	V_{16-11}	typ.	12	V
Sync input voltage (peak-to-peak value)	$V_{2-11(p-p)}$		0.07 to 1	V
Slicing level		typ.	50	%
Control sensitivity of horizontal PLL		typ.	1800	Hz/V
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{8-11(p-p)}$	typ.	11	V
Vertical sync output pulse (peak-to-peak value)	$V_{1-11(p-p)}$	typ.	11	V
Burst-key output pulse (peak-to-peak value)	$V_{13-11(p-p)}$	typ.	11	V

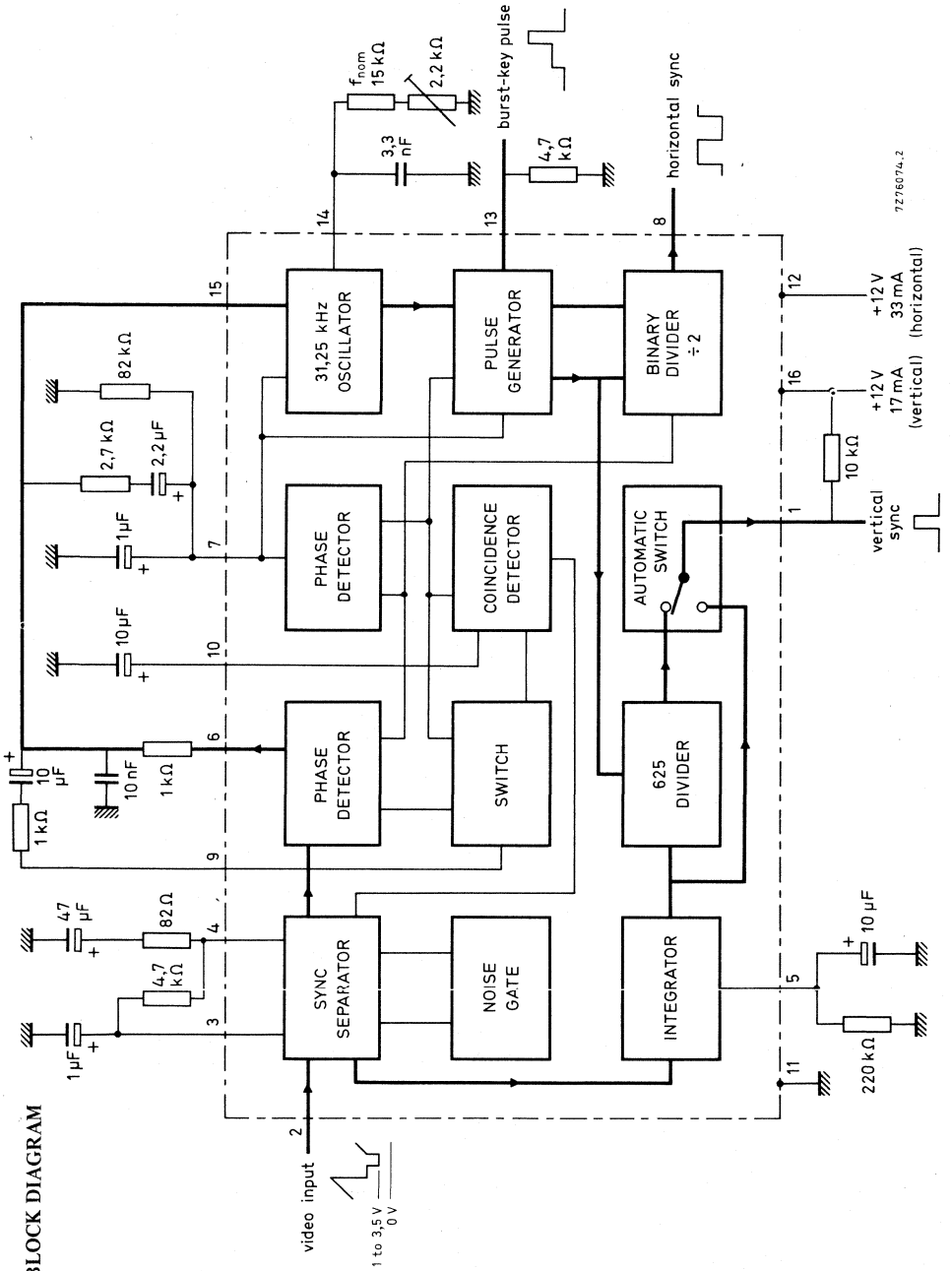
PACKAGE OUTLINES (see general section)

TDA2571 : 16-lead DIL; plastic.

TDA2571Q : 16-lead QIL; plastic.



BLOCK DIAGRAM



7276074-2

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (horizontal)	V_{12-11}	max.	13,2	V
(vertical)	V_{16-11}	max.	13,2	V

Power dissipation

Total power dissipation	P_{tot}	max.	1	W
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Temperatures

Storage temperature	T_{stg}	-55 to +125	°C
Operating ambient temperature	T_{amb}	-25 to +65	°C

CHARACTERISTICS at $V_{12-11} = 12$ V; $V_{16-11} = 12$ V; $T_{amb} = 25$ °C
measured in the circuit on page 2

<u>Supply voltage range</u> (pins 12 and 16)	$V_{12-11}; V_{16-11}$	typ.	12	V
			10 to 13,2	V

Current consumption

$I_{12} + I_{16}$	typ.	50	mA
	<	70	mA

Sync separator and noise gate

Sync pulse amplitude (negative going) peak-to-peak value	$V_{2-11(p-p)}$	0,07 to 1	V 1)
Top-sync level	V_{2-11}	1,0 to 3,5	V
Slicing level		typ.	50 % 2)
Slicing level noise gating	V_{2-11}	<	0,7 V

Phase locked loop

Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Control sensitivity of horizontal PLL		typ.	1800	Hz/V
Control sensitivity of phase detector		typ.	1,2	V/ μ s

1) Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

2) The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

CHARACTERISTICS (continued)

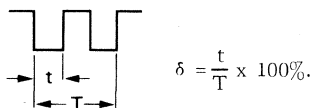
Horizontal oscillator

Frequency; free running	f_0	typ.	31,250	kHz
Frequency at output pin 8	f_8	typ.	15,625	kHz
Spread of frequency without spread of external components	Δf_0	typ.	± 4	%
Temperature coefficient	T	<	$2,5 \times 10^{-4}$	/°C
Change of frequency when V_{12-11} drops to 6 V	Δf_0	<	10	%
Change of frequency when V_{12-11} increases from 10 to 13,2 V	Δf_0	<	0,5	%
Output voltage; no load (peak-to-peak value)	$V_{8-11(p-p)}$	>	10	V
Output resistance	R_{8-11}	typ.	300	Ω
Output current range (peak-to-peak value)	$I_{8(p-p)}$		0 to 40	mA
Duty factor of output pulse	δ	typ.	46	% 1)
Delay between falling edge of output pulse and end of sync pulse at pin 2	t_d	typ.	0,9	μs 2)

Burst-key pulse

Output voltage (peak-to-peak value)	$V_{13-11(p-p)}$	<	10	V
Duration of upper part of output pulse	t_p	typ.	3,3	μs 2)
Duration of lower part of output pulse	t_p	typ.	8,8	μs 2)
Amplitude of lower part of output pulse	$V_{13-11(p-p)}$	typ.	3	V 2)
Output resistance	R_{13-11}	typ.	200	Ω
Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse	t_p	typ.	0,9	μs 2)

1) The duty factor is specified as follows :

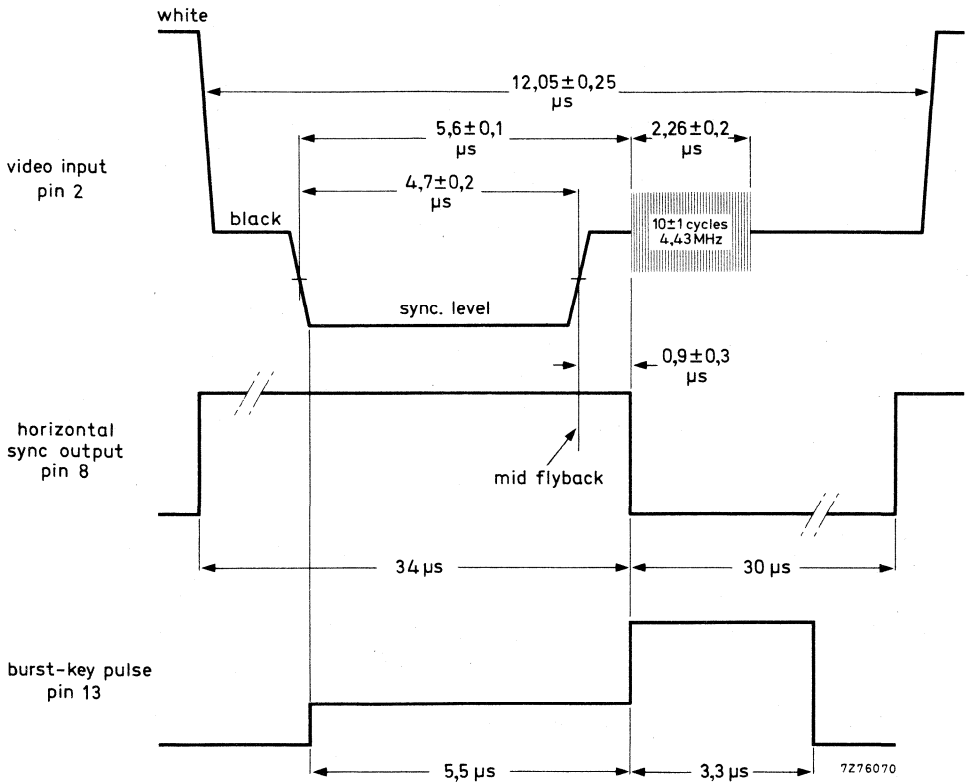


2) See waveforms on page 5.

CHARACTERISTICS (continued)

Vertical sync pulse

Output voltage (peak-to-peak value)	$V_{1-11(p-p)}$	>	10	V
Duration of output pulse during indirect synchronization	t_p	typ.	170	μs
Load resistor to pin 2	R_L	>	2	k Ω
Ratio between basic horizontal oscillator frequency and vertical pulse			625	\downarrow



Relationship between the video input signal to the TDA2571 and the horizontal sync and burst-key pulse output.

¹⁾ When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Vertical sync pulse output

A resistor of about 10 k Ω must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

The output pulse will come from the 625 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2.

The standard and non-standard signals are detected automatically.

2. Video input

The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3.5 V without affecting the sync separator operation.

The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

The noise gate is activated at an input level < 0,7 V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V.

When i. f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2571 is not required.

3. Sync separator slicing level output

The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 1 μ F.

4. Black level detector output

The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μ F in series with a resistor of 82 Ω has to be connected to this pin. A 4,7 k Ω resistor must be connected between pins 3 and 4.

APPLICATION INFORMATION (continued)5. Vertical sync pulse integrator bias network

The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: $R = 220 \text{ k}\Omega$; $C = 10 \text{ }\mu\text{F}$.

6. Horizontal phase detector output

The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is **obtained which may be present on the supply line**). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch

This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

During out-of-sync or VCR playback for signals containing VCR identification signal only, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

A 10 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.

The following output voltages can occur:

- when in-sync: 0,4 V
- when out-of-sync: 2,0 V
- during noise at input: 1,0 V
- with gap in sync pulse: 2,35 V

APPLICATION INFORMATION (continued)

The gap in the sync pulse is intended for a VCR identification signal, and has a width of $0.5 \mu\text{s}$.

When such an identification is recognized, the receiver will automatically switch to a short flywheel filter time constant during VCR playback.

When the output voltage $< 1.85 \text{ V}$, the flywheel filter is switched to a long time constant, the phase detector output current to a low value and the gating of the phase detector is switched-on.

For a voltage $> 1.85 \text{ V}$, the flywheel filter has a short time constant, the phase detector has a high current and the **gating** of the phase detector is switched-off.

The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screaming of the horizontal output transformer).

The output impedance is high thus the time constant can be switched-off manually (to $+12 \text{ V}$).

11. Negative supply (ground)12. Positive supply horizontal oscillator

Interference and hum on this supply line can affect the oscillator frequency.

It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA .

13. Burst-key pulse output

This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of $8,8 \mu\text{s}$ (for phase relation see page 5). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of $3,3 \mu\text{s}$.

The leading edge of this pulse has a delay of $0,9 \mu\text{s}$ with respect to the falling edge of the sync pulse at the input (pin 2).

This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

14. RC-network horizontal oscillator

Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable.

This part should be as small as possible, because of poor stability of variable carbon resistors.

The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin16. Positive supply sync separator and divider circuit (vertical)

For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA .

CONTROL CIRCUIT FOR SMPS

The TDA2581 is a monolithic integrated circuit for controlling switched-mode power supplies (SMPS) which are provided with the drive for the horizontal deflection stage. The circuit features the following:

- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the positive-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.

QUICK REFERENCE DATA

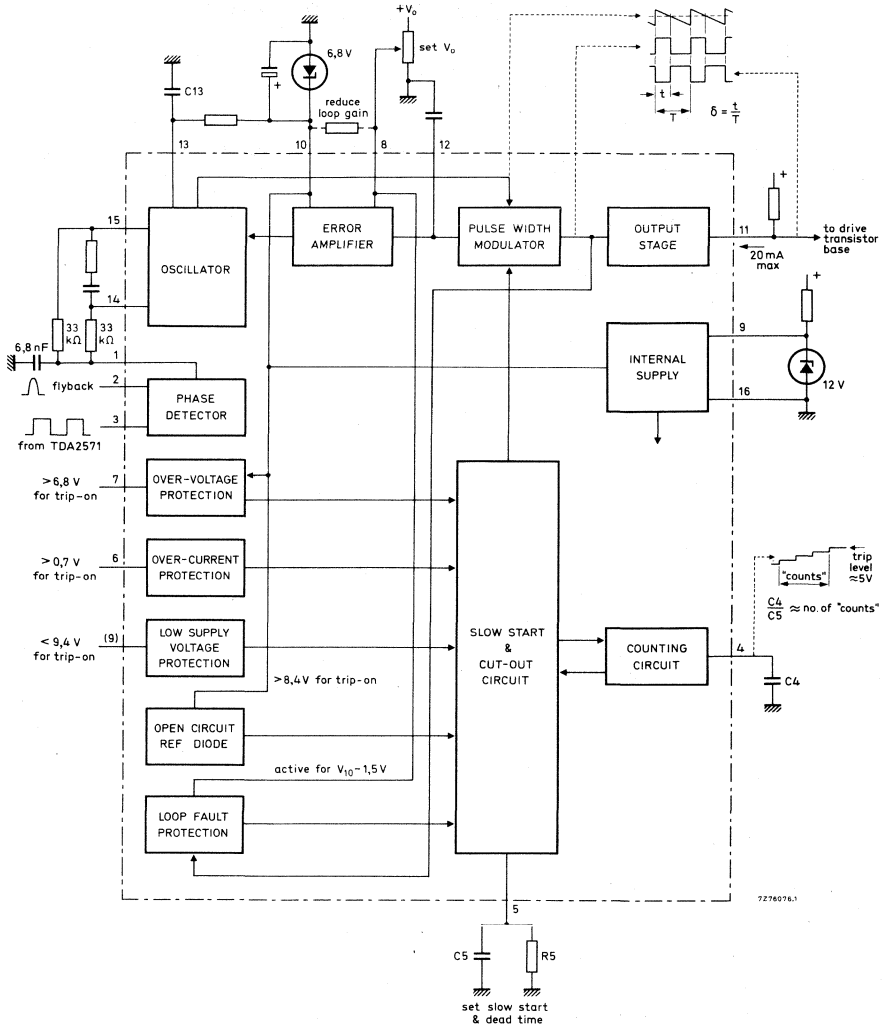
Supply voltage	V_{9-16}	typ.	12	V
Supply current	I_9	typ.	15	mA
<u>Input signals</u>				
Horizontal drive pulse (peak-to-peak value)	$V_{3-16(p-p)}$	typ.	11	V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2-16(p-p)}$	typ.	5	V
External reference voltage	V_{10-16}	typ.	6,7	V
<u>Output signals</u>				
Duty factor of output pulse	δ		0 to 98	%
Output voltage at $I_0 < 20$ mA (peak value)	V_{11-16M}	typ.	11,8	V
Output current (peak value)	I_{11M}	<	40	mA

PACKAGE OUTLINES (see general section)

TDA2581 : 16-lead DIL; plastic.

TDA2581Q : 16-lead QIL; plastic.

BLOCK DIAGRAM



Note: trip levels are nominal values.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage	V_{9-16}	max.	14	V
Pin 11	V_{11-16}		0 to 14	V

Current

Output current	I_{11}	max.	40	mA
----------------	----------	------	----	----

Power dissipation

Total power dissipation	P_{tot}	max.	340	mW
-------------------------	-----------	------	-----	----

Temperatures

Storage temperature	T_{stg}	-25 to +125	°C
Operating ambient temperature	T_{amb}	-25 to +80	°C

CHARACTERISTICS at $V_{9-16} = 12$ V; $V_{10-16} = 6,7$ V; $T_{amb} = 25$ °C
measured in the circuit on page 2

Supply voltage range	V_{9-16}	typ.	12	V
			10 to 14	V
Protection voltage for too low supply voltage	V_{9-16}	typ.	9,4	V
			8,6 to 9,9	V
Supply current at $\delta = 50\%$	I_9	typ.	15	mA
Supply current during protection	I_9	typ.	15	mA
Minimum required supply current	I_9	<	18,5	mA ¹⁾
Power consumption	P	typ.	180	mW

Required input signals

Reference voltage	V_{10-16}	typ.	6,7	V
			5,6 to 7,5	V ²⁾
High reference voltage protection : threshold voltage	V_{10-16}	typ.	8,4	V
			7,7 to 9,1	V
Feedback input impedance at pin 8	$ Z_{8-16} $	typ.	100	k Ω
Horizontal drive pulse (square-wave or differentiated; negative transient is reference) peak-to-peak value	$V_{3-16(p-p)}$	typ.	11	V
			5 to 12	V

1) This value refers to the minimum required supply current that will start all devices under the following conditions : $V_{9-16} = 10$ V; $V_{10-16} = 6,8$ V; $\delta = 50\%$.

2) Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.

CHARACTERISTICS (continued)

Flyback pulse or differential deflection current	V_{2-16}		1 to 5	V
Over-current protection : threshold voltage	$\pm V_{6-16}$	typ.	710 660 to 760	mV ¹⁾ mV
Over-voltage protection : threshold voltage	V_{7-16}	typ.	$V_{10-16} - 0,1$ $V_{10-16} - 0,35$ to $V_{10-16} + 0,15$	V V
Remote control voltage; switch off	V_{4-16}	>	5,8	V ²⁾
switch on	V_{4-16}	<	4,5	V

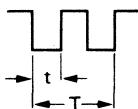
Delivered output signals

Horizontal drive pulse (loaded with a resistor of 560Ω to +12V) peak-to-peak value	$V_{11-16(p-p)}$	>	11,6	V
Output current; peak value	I_{11M}	<	40	mA
Saturation voltage of output transistor at $I_{11} = 20$ mA	V_{CEsat}	typ. <	200 400	mV mV
at $I_{11} = 40$ mA	V_{CEsat}	<	525	mV
Duty factor of output pulse	δ		0 to 98,6	% ³⁾
Charge current for capacitor on pin 4	I_4	typ.	120	μ A
Charge current for capacitor on pin 5	I_5	typ.	130	μ A
Supply current for reference	I_{10}	typ.	0,9 0,6 to 1,45	mA mA

¹⁾ The temperature coefficient is typical $-1,7$ mV/ $^{\circ}$ C.

²⁾ See pin 4 pages 7 and 8.

³⁾ The duty factor is specified as follows :



$$\delta = \frac{t}{T} \times 100\%$$

The maximum duty factor value can be set to a desired value (see application information pin 12).

CHARACTERISTICS (continued)**Oscillator**

Temperature coefficient	typ.	-300	ppm/°C
	<	-400	ppm/°C
Relative frequency deviation for V_{10-16} changing from 6 to 7 V	typ.	-1,5	%
	<	-2	%
Oscillator frequency spread (with fixed external components)	<	±3	%
Frequency control sensitivity at pin 15	typ.	4,5	kHz/V ¹⁾

Phase control loop

Loop gain of APC-system (automatic phase control)	typ.	5	kHz/μs
Catching range	Δf	typ. ±1,5	kHz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ. 1	μs
Tolerance of phase relation	Δt	< ±0,4	μs

PINNING

- | | |
|--|--|
| 1. Phase detector output | 9. Positive supply |
| 2. Flyback pulse position input | 10. Reference input |
| 3. Reference frequency input | 11. Output |
| 4. Re-start count capacitor/
remote control input | 12. Maximum duty factor adjustment/
smoothing |
| 5. Slow start and transfer characteristic
for low feedback voltages | 13. Oscillator timing network |
| 6. Over-current protection input | 14. Reactance stage reference voltage |
| 7. Over-voltage protection input | 15. Reactance stage input |
| 8. Feedback voltage input | 16. Negative supply (ground) |

¹⁾ For component values see circuit diagram on page 2.

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Phase detector output

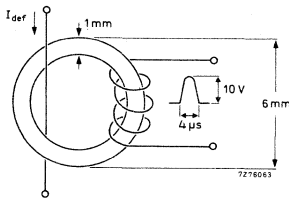
The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.

The current values are chosen such that the correct phase relation is obtained when the reference signal on pin 3 is delivered by the TDA2571.

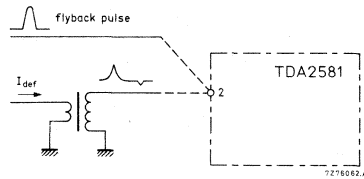
With a resistor of 18 k Ω and a capacitor of 2,7 nF the control steepness is 0,55 V/ μ s.

2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 μ s. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 μ s).



(a)



(b)

The toroidal transformer in (a) is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in (b).

3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.

The negative-going transient switches the current source connected to pin 1 from positive to negative. The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation).

The input circuit switching level is about 3 V and the input impedance is about 10 k Ω .

4. Re-start count capacitor/remote control inputCounting

An external capacitor ($C_4 = 47 \mu$ F) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.

If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.

After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.

If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

APPLICATION INFORMATION (continued)

The number of times this action is repeated (n) for a persisting fault condition is now determined by: $n = C4/C5$.

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 k Ω . When the externally applied voltage $V_{4-16} > 5,8$ V, the circuit switches off; switching on occurs when $V_{4-16} < 4,5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor ($C5 = 4,7$ μ F) and resistor ($R5 = 270$ k Ω) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5.

The transfer for three different resistor values is given in the graph on page 11.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16.

The protection circuit operates at a typical value of about 710 mV. The circuit trips on both positive and negative polarity.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level, the protection circuit will operate. When this function is not used, pin 7 should be connected to pin 16.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.

Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the graphs on pages 11 and 12.

APPLICATION INFORMATION (continued)9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16. The reference voltage must be between 5,6 and 7,5 V. The IC delivers about 0,9 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothingMaximum duty factor adjustment

Pin 12 is connected to the output voltage of the amplitude comparator (V_{10-8}). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A low voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of a p-n-p transistor used as a voltage source.

The graph on page 12 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 k Ω limits the maximum duty factor to about 50%.

This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.

The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω .

APPLICATION INFORMATION (continued)

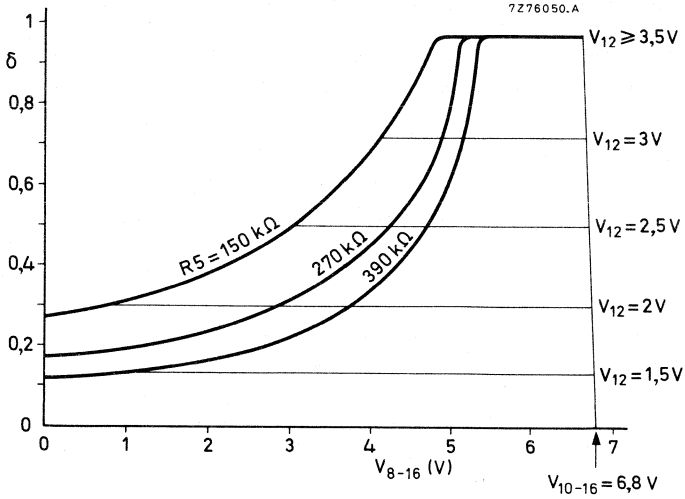
14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,5 V for reference voltage $V_{10-16} = 6,8$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

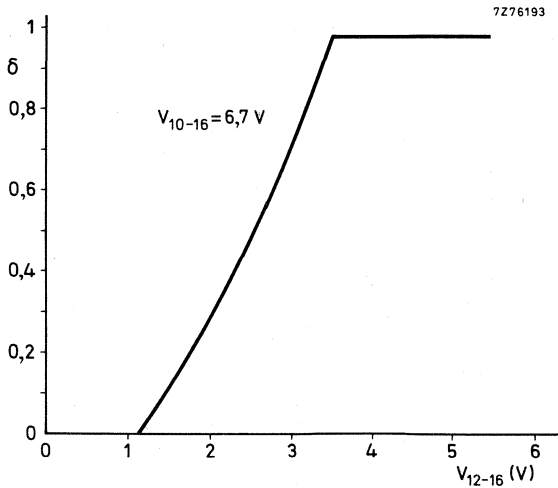
15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between pins 14 and 15. Control sensitivity is typically 4,5 kHz/V.

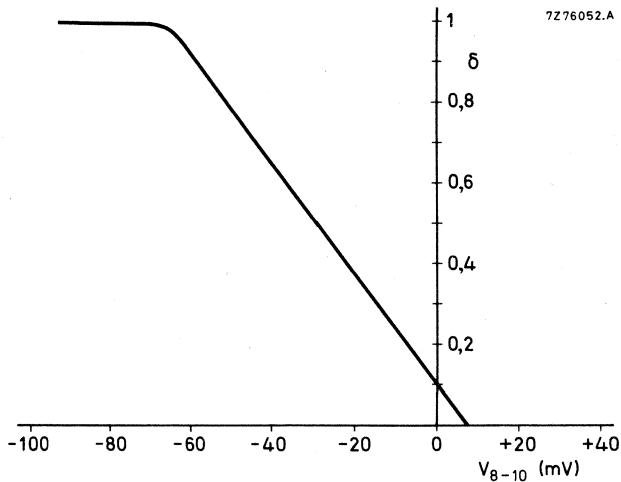
16. Negative supply (ground)



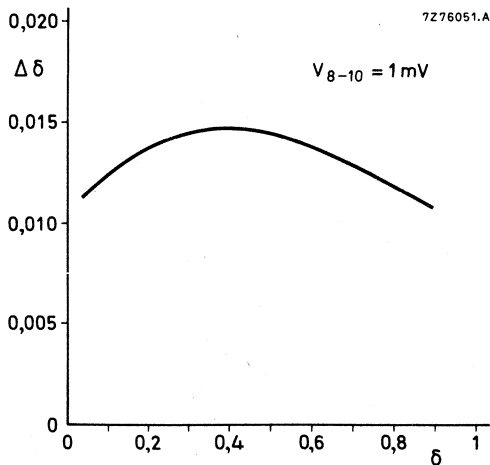
Duty factor of output pulses as a function of V_{8-16} with R_5 as a parameter, and with V_{12} as a limiting value; $V_{10-16} = 6.8\text{ V}$.



Maximum duty factor limitation as a function of V_{12-16} .



Duty factor of output pulses as a function of error amplifier input (V_{8-10}).



Change in duty factor of output pulses for a 1 mV error amplifier input change (V_{8-10}) as a function of initial duty factor.

LINE OSCILLATOR COMBINATION

The TDA2590 is an integrated line oscillator circuit for colour television receivers using thyristor or transistor line deflection output stages.

The circuit incorporates the following functions:

- line oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage
- phase comparison between line flyback pulse and oscillator voltage
- switch for changing the filter characteristic and the gate circuit (when used for VCR)
- coincidence detector
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage for direct drive of thyristor deflection circuits
- sync gating pulse generator
- low supply voltage protection

QUICK REFERENCE DATA

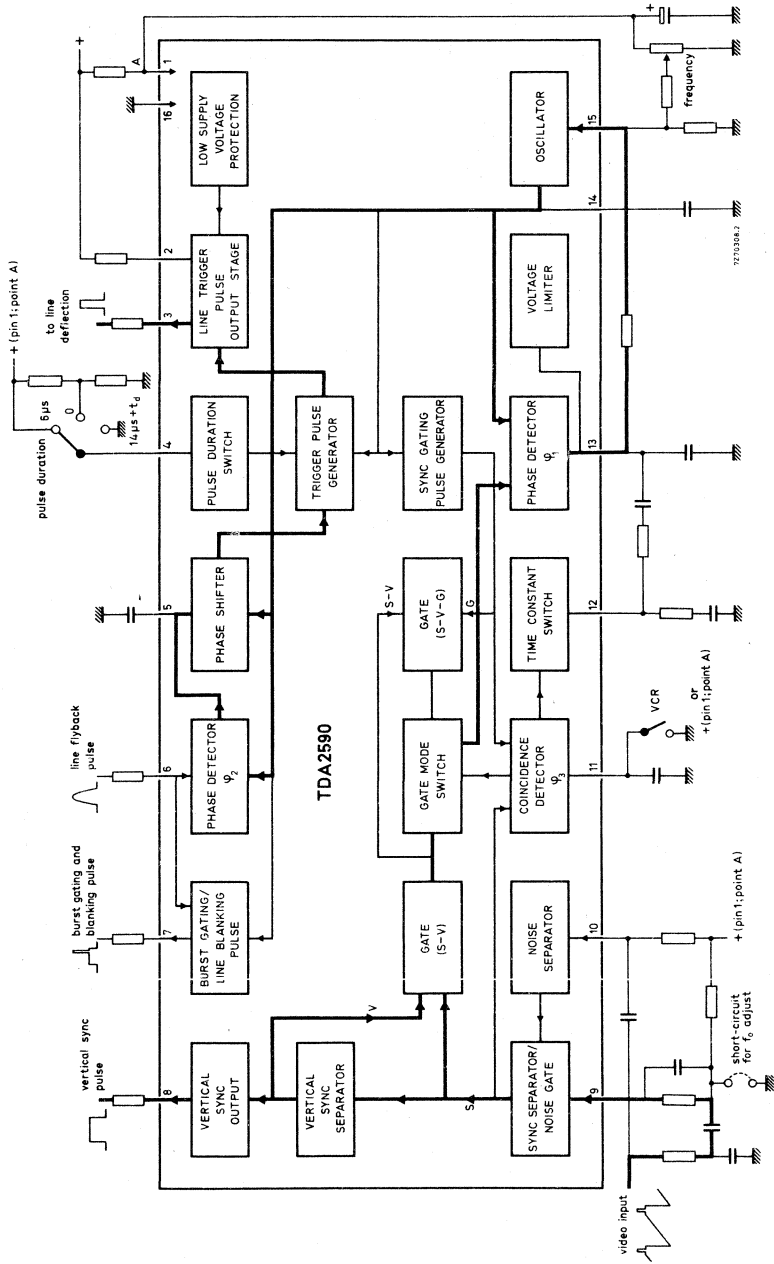
Supply voltage	V_{1-16}	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	3 V
Noise separator input voltage (peak-to-peak value)	$V_{10-16(p-p)}$	typ.	3 V
Pulse duration switch input voltage at $t = 6 \mu s$ $t = 14 \mu s + t_d$	V_{4-16}	9, 4 to V_{1-16}	V
	V_{4-16}	0 to 4, 0	V
Voltage for switching on VCR	V_{11-16}	0 to 1, 5	V
		9 to V_{1-16}	V
Output signals			
Vertical sync output pulse (peak-to-peak value)	$V_{8-16(p-p)}$	typ.	11 V
Burst gating output pulse (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	11 V
Line drive pulse (peak-to-peak value)	$V_{3-16(p-p)}$	typ.	10, 5 V

PACKAGE OUTLINES (see general section)

TDA2590 : 16-lead DIL; plastic.

TDA2590Q : 16-lead QIL; plastic.

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage at pin 1 (when supplied by the IC) at pin 2	V_{1-16} V_{2-16}	max.	13,2	V
		max.	18	V
Pin 4	V_{4-16}		0 to 13,2	V
Pin 9	V_{9-16}		-6 to +6	V
Pin 10	V_{10-16}		-6 to +6	V
Pin 11	V_{11-16}		0 to 13,2	V

Currents

Pin 2 (peak value)	I_{2M}	max.	400	mA
Pin 3 (peak value)	$-I_{3M}$	max.	400	mA
Pin 4	I_4	max.	1	mA
Pin 6	$\pm I_6$	max.	10	mA
Pin 7	$-I_7$	max.	10	mA
Pin 11	I_{11}	max.	2	mA

Power dissipation

Total power dissipation	P_{tot}	max.	800	mW
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Temperatures

Storage temperature	T_{stg}		-20 to +125	$^{\circ}\text{C}$
Operating ambient temperature	T_{amb}		-20 to +60	$^{\circ}\text{C}$

CHARACTERISTICS at $V_{1-16} = 12\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

Required input signals

Sync separator

Input switching voltage	V_{9-16}	typ.	0,8	V
Input keying current	I_9		5 to 100	μA
Input blocking current at $V_{9-16} = -5\text{ V}$	I_9	<	1	μA
Input switching current	I_9	\leq	5	μA

Noise separator

Input switching voltage	V_{10-16}	typ.	1,4	V
Input keying current	I_{10}		5 to 100	μA
Input switching current	I_{10}	typ.	150	μA
Input blocking current at $V_{10-16} = -5\text{ V}$	I_{10}	<	1	μA

CHARACTERISTICS (continued)

Line flyback pulse

Input current	I_6	>	10 μ A
Input switching voltage	V_{6-16}	typ.	1,4 V
Input limiting voltage	V_{6-16}		-0,7 to +1,4 V
Input resistance	R_{6-16}	typ.	0,4 k Ω

Pulse duration switch

For $t = 6 \mu$ s

Input voltage	V_{4-16}		9,4 to V_{1-16} V
Input current	I_4	>	200 μ A

For $t = 14 \mu$ s + t_d

Input voltage	V_{4-16}		0 to 4,0 V
Input current	$-I_4$	>	200 μ A

For $t = 0$; $V_{3-16} = 0$

Input voltage	V_{4-16}		5,4 to 6,5 V ¹⁾
Input current (input open)	I_4	typ.	0 μ A

Switching on VCR

Input voltage	V_{11-16}		0 to 1,5 V ²⁾
	V_{11-16}		9 to V_{1-16} V
Input current	$-I_{11}$	>	200 μ A ²⁾
	I_{11}		1 to 2 mA

Delivered output signals

Vertical sync pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{8-16(p-p)}$	>	10 V
		typ.	11 V
Output resistance	R_8	typ.	2 k Ω

Burst gating pulse (positive-going)

Output voltage (peak-to-peak value)	V_{7-16}	>	10 V
		typ.	11 V
Output resistance	R_7	typ.	0,4 k Ω

1) Can also be not connected.

2) When supplied by the IC.

CHARACTERISTICS (continued)Blanking pulse

Output voltage (peak-to-peak value)	$V_{7-16(p-p)}$	2,5 to 3,5 V
Output resistance	R_7	typ. 0,4 k Ω

Line drive pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{3-16(p-p)}$	typ. 10,5 V
Output current (average value)	$-I_{3(AV)}$	typ. 100 mA
Output resistance for leading edge of line pulse for trailing edge of line pulse	R_{3-16}	typ. 2,5 Ω
	R_{3-16}	typ. 20 Ω

Oscillator

Threshold voltage low level	V_{14-16}	typ. 4,4 V
Threshold voltage high level	V_{14-16}	typ. 7,6 V
Discharge current	$\pm I_{14}$	typ. 0,47 mA

Phase comparison (ϕ_1 ; sync pulse/oscillator)

Control voltage range	V_{13-16}	3,8 to 8,2 V
Control current (peak value)	$\pm I_{13M}$	typ. 2,1 mA 1,9 to 2,3 mA
	I_{13}	< 1 μ A
Output blocking current at $V_{13-16} = 4$ to 8 V		1) 2)
Output resistance at $V_{13-16} = 4$ to 8 V at $V_{13-16} < 3,8$ V or $> 8,2$ V		high ohmic low ohmic

Time constant switch

Output voltage	V_{12-16}	typ. 6 V
Output current	$\pm I_{12}$	< 1 mA
Output resistance		
at $V_{11-16} = 2,5$ to 7 V	R_{12-16}	typ. 0,1 k Ω
at $V_{11-16} < 1,5$ V or > 9 V	R_{12-16}	typ. 60 k Ω

1) Current source.

2) Emitter follower.

CHARACTERISTICS (continued)

Coincidence detector (φ_3)

Output voltage	V_{11-16}	0,5 to 6 V
Output current (peak value)		
without coincidence	I_{11M}	typ. 0,1 mA
with coincidence	$-I_{11M}$	typ. 0,5 mA

Phase comparison (φ_2 ; oscillator/line flyback pulse)

Control voltage range	V_{5-16}	5,4 to 7,6 V
Control current (peak value)	$\pm I_{5M}$	typ. 1 mA
Output resistance		
at $V_{5-16} = 5,4$ to $7,6$ V	high ohmic	1)
at $V_{5-16} < 5,4$ V or $> 7,6$ V	R_{5-16}	typ. 8 k Ω
Input current at blocked phase detector		
$V_{5-16} = 5,4$ to $7,6$ V	I_5	$< 5 \mu\text{A}$

APPLICATION INFORMATION at $V_{1-16} = 12$ V; measured in circuit on page 9

Sync separator

Input voltage (positive video signal; peak-to-peak value)	$V_{9-16(p-p)}$	typ. 3 V 1 to 7 V
Input keying current	I_9	5 to 100 μA

Noise gating

Input voltage (positive video signal; peak-to-peak value)	$V_{10-16(p-p)}$	typ. 3 V 1 to 7 V
Input keying current	I_{10}	5 to 100 μA
Superimposed noise voltage (peak-to-peak value)	$V_{n(p-p)}$	< 7 V

Vertical sync pulse separator

Delay between leading edge of input and output signal	t_{on}	typ. 12 μs
Delay between trailing edge of input and output signal	t_{off}	$> t_{on}$ μs
Output voltage (peak-to-peak value)	$V_{8-16(p-p)}$	typ. 11 V
Output resistance	R_{8-16}	typ. 2 k Ω

1) Current source.

APPLICATION INFORMATION (continued)OscillatorFrequency; free running ($C_{14-6} = 4,7 \text{ nF}$; $R_{15-16} = 12 \text{ k}\Omega$) f_0 typ. 15,625 kHz

Spread of frequency

 $\Delta f_0/f_0$ < ± 5 % 1)

Frequency control sensitivity

 $\Delta f_0/\Delta I_{15}$ typ. 31 Hz/ μA

Adjustment range of network in circuit on page 2

 $\Delta f_0/f_0$ typ. ± 10 %Influence of supply voltage on frequency
at $V_{1-16} = 12 \text{ V}$ $\frac{\Delta f_0/f_0}{\Delta V/V_{\text{nom}}}$ < $\pm 0,05$ 1)Change of frequency when V_{1-16} drops to 5 V Δf_0 < ± 10 % 1)Temperature coefficient of oscillator
frequency per $^{\circ}\text{C}$ < $\pm 10^{-4}$ 1)Phase comparison (φ_1 ; sync pulse/oscillator)

Control sensitivity

typ. 2 kHz/ μs Catching and holding range (82 k Ω between
pins 13 and 15) Δf typ. ± 780 Hz

Spread of catching and holding range

 $\Delta(\Delta f)$ typ. ± 10 % 1)Phase comparison (φ_2 ; oscillator/line flyback pulse)Permissible delay between leading edge of output
pulse and leading edge of flyback pulse ($t_{fp} = 12 \mu\text{s}$) t_d 0 to 15 μs

Static control error

 $\Delta t/\Delta t_d$ < 0,2 %Overall phase relationPhase relation between middle of sync pulse
and the middle of the flyback pulse t typ. 2,6 μs

Tolerance of phase relation

 $|\Delta t|$ < 0,7 μs

The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase control φ_2 .

If additional adjustment is applied the following values are valid.

Adjustment sensitivity

caused by: adjustment voltage
adjustment current

$\Delta V_{5-16}/\Delta t$ typ. 0,1 V/ μs
 $\Delta I_{15}/\Delta t$ typ. 30 $\mu\text{A}/\mu\text{s}$

1) Excluding external component tolerances.

APPLICATION INFORMATION (continued)

Burst gating pulse

Phase relation between middle of sync pulse at the input
and the trailing edge of the burst gating pulse; $V_{7-16} = 7\text{ V}$ t typ. 6,6 μs
5,8 to 7,4 μs

Phase relation between middle of sync pulse at the input
and the leading edge of the burst gating pulse ; $V_{7-16} = 7\text{ V}$ t typ. 1,9 μs
1,0 to 2,8 μs

Line drive pulse

Output pulse duration
at $V_{4-16} > 9,4\text{ V}$ t_p typ. 6 μs
4,5 to 7,5 μs

at $V_{4-16} < 4\text{ V}$ t_p 14 + t_d μs ¹⁾

Supply voltage for switching off the output pulse V_{1-16} typ. 4 V

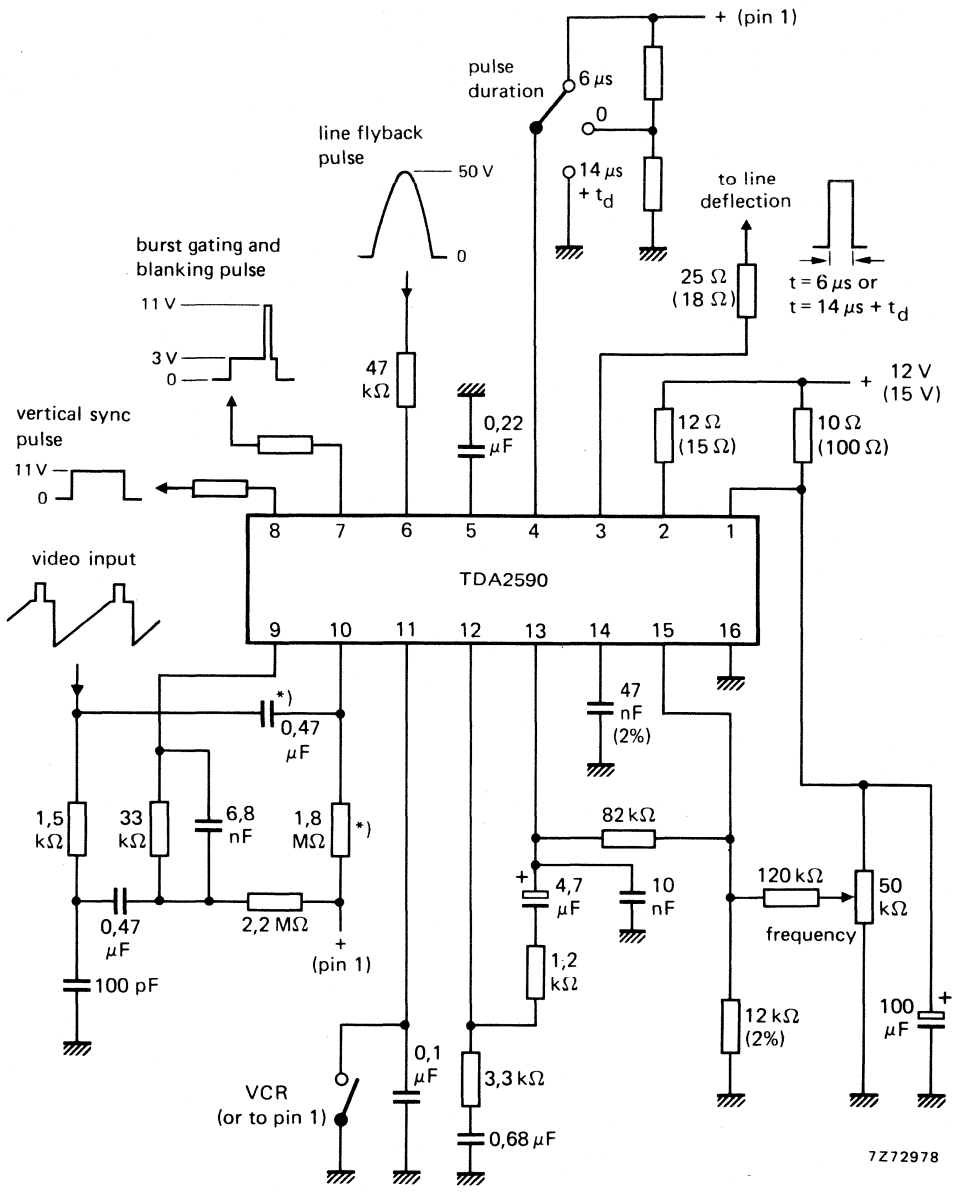
Internal gating pulse

Pulse duration t_p typ. 7,5 μs

⋮

¹⁾ t_d = switch-off delay of line output stage.

APPLICATION INFORMATION (continued)



*) These components are not needed if the TDA2540; TDA2541 ICs are used, because these devices already incorporate a noise inverter.



VERTICAL DEFLECTION CIRCUIT

The TDA2600 is a monolithic integrated circuit in a plastic 16-lead power dual in-line package intended for use in a vertical deflection circuit in both 90° and 110° colour television receivers.

The circuit operates in the class-D switching mode with modulated pulse width and is capable of handling currents up to 7 A peak-to-peak at a maximum power dissipation of 7 W.

A feature is excellent immunity against e. h. t. flashover.

QUICK REFERENCE DATA

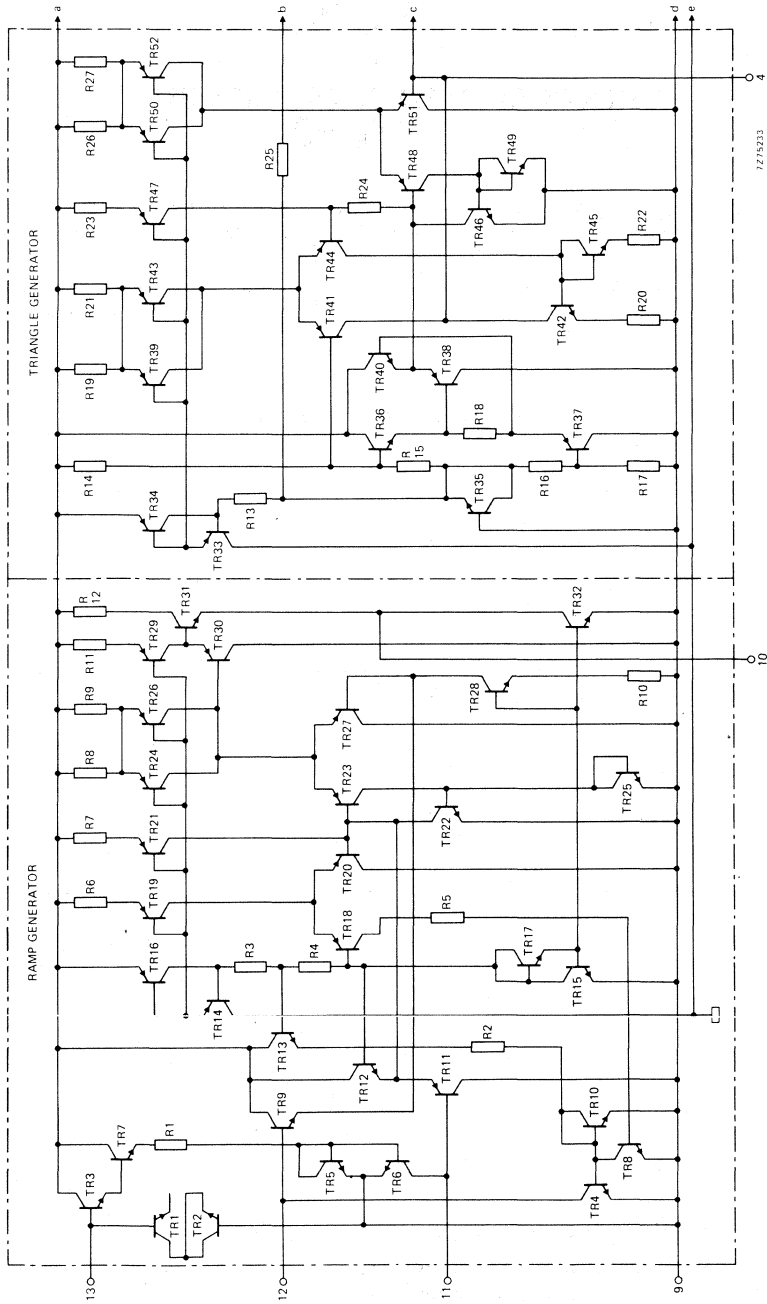
Supply voltage	V_{15-1}	typ.	36	V
Supply current	I_{15}	typ.	380	mA
Output current (peak-to-peak value)	$I_{16(p-p)}$	typ.	4	A
Total power dissipation	P_{tot}	typ.	4, 5	W
Positive sync sensitivity	V_{13-1}		2, 5 to 8	V
Negative sync sensitivity	$-V_{11-1}$	typ.	10	V

PACKAGE OUTLINES (see general section)

TDA2600 : 16-lead DIL; plastic power (SOT-69B).

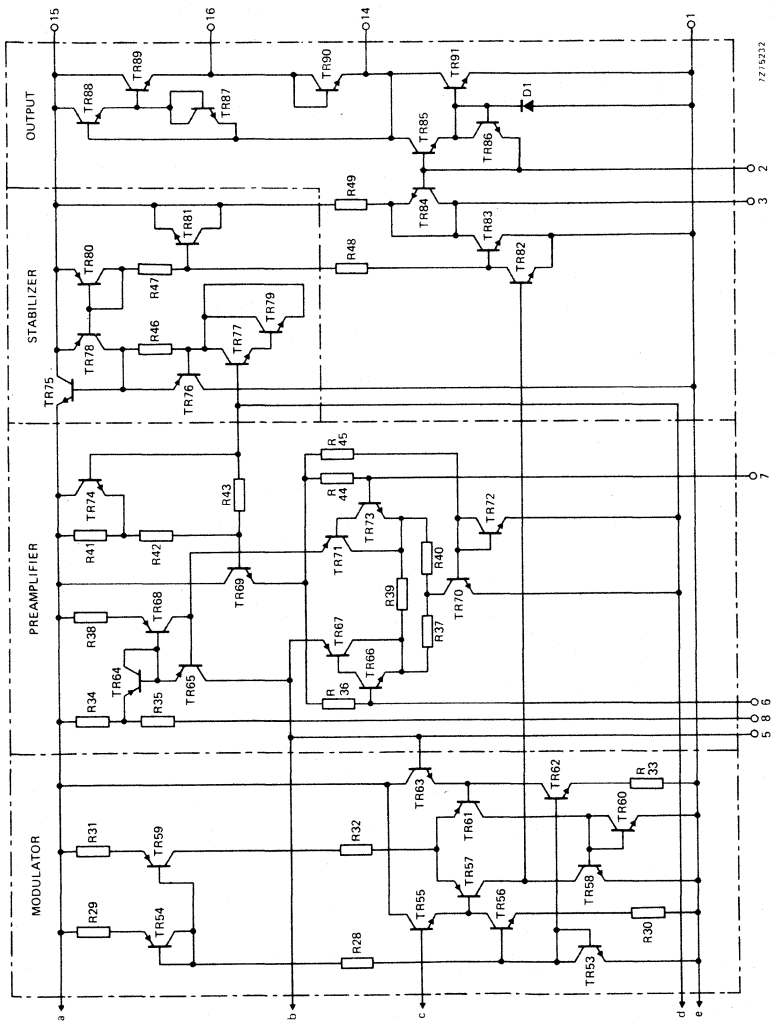
TDA2600Q : 16-lead QIL; plastic power (SOT-76B).

CIRCUIT DIAGRAM



1275233

CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)Voltages

Supply voltage	V_{15-1}	max.	40	V
Short-term setting; V_{15-1} up rating	V_{15-1}	max.	42	V

Current

Output current (peak-to-peak value)	$I_{16(p-p)}$	max.	7	A
-------------------------------------	---------------	------	---	---

Power dissipation

Total power dissipation	P_{tot}	max.	7	W
-------------------------	-----------	------	---	---

Temperatures

Storage temperature	T_{stg}	-25 to +150	°C
Operating ambient temperature	T_{amb}	0 to +65	°C

TYPICAL OPERATING CONDITIONS

For 20AX system with series dynamic correction and AT4043/35 class-D filter choke and AT1080 deflection coils.

Supply voltage	V ₁₅₋₁	typ.	37	V
Supply current	I ₁₅	typ.	0,38	A
Deflection coil current (6% overscan)	I ₁₆	typ.	3,6	A
Dissipation	P _{tot}	typ.	4,4	W
Non-linearity of deflection circuit		<	5	%
Average d. c. output level		typ.	18 ± 1	V
Switching frequency		typ.	150	kHz
Scan height variation at T _{amb} = 0 to 65 °C			1	%
Vertical deflection flyback time		typ.	900	µs
Recommended thermal resistance of heatsink (driving the 20AX system at T _{amb} = 65°; T _j = 100 °C)	R _{th h-a}	typ.	7	°C/W

CHARACTERISTICS at V₁₅₋₁ = 36 V; T_{amb} = 25 °C; measured in application circuit on page 7

Triangle level (pin 4)	V ₄₋₉	typ.	7,5	V
Triangle amplitude (peak-to-peak value)	V _{4-9(p-p)}	typ.	2,1	V
Preamplifier average output level (pin 5)	V _{5-9(av)}	typ.	7,5	V
Preamplifier input voltage for internal biasing (pins 6 and 7)	V _{6;7-9}	typ.	2	V
D. C. feedback reference voltage (pin 8)	V ₈₋₁	typ.	14	V
Sawtooth generator output current capability (pin 10)	I ₁₀	>	5	mA ¹⁾
Current from pin 11	I ₁₁	<	20	µA
Current into pin 12 during scan	I ₁₂	<	2	µA
Current into pin 12 during flyback	I ₁₂	typ.	2,5	mA
Sawtooth voltage (peak-to-peak value; pin 12)	V _{12-9(p-p)}	typ.	5	V
Positive sync pulse clamping voltage (pin 13)	V ₁₃₋₉	typ.	8	V

¹⁾ The voltage waveform at pin 10 is substantially the same as at pin 12.

APPLICATION INFORMATION (continued)

Pinning

- | | |
|---|--|
| 1. Negative supply (ground) | 9. Common of small signal stages |
| 2. Bottom drive input of power output stage | 10. Ramp generator output; amplitude and linearity control |
| 3. Output of pulse-width modulator | 11. Negative sync input and frequency control |
| 4. Triangle generator timing capacitor | 12. Ramp timing capacitor |
| 5. High frequency decoupling of preamplifier output | 13. Positive sync input |
| 6. Preamplifier input | 14. Top drive input of power output stage |
| 7. Preamplifier input | 15. Positive supply |
| 8. D.C. feedback reference voltage | 16. Output |

The function is quoted against the corresponding pin number

1. Negative supply (ground)
2. Bottom drive input of power output stage

The square wave from the pulse-width modulator is a.c. coupled to pin 2 allowing either positive or negative drive of the output stage. This method ensures reliable switching of the output transistors.

3. Output of pulse-width modulator

The power output stage must be driven by an a.c. signal, so the modulator output at pin 3 is externally connected via a capacitor to pin 2. A 39 Ω resistor in series with a 3,3 nF capacitor is also connected to pin 3. These components, together with some others suppress the radiation which may occur in class-D circuits.

4. Timing of the triangle oscillator

The frequency of the signal generated in the triangle oscillator is determined by the capacitor between pins 4 and 9. With a capacitor of 330 pF the frequency is 150 kHz (typical). The triangle generator waveform is internally fed into the pulse-width modulator which transforms it into a square-wave signal.

5. Preamplifier output

The preamplifier output varies with the 50 Hz ramp generator frequency around an average level of 7,5 V (typical). This signal is also fed into the modulator. A 2,2 nF capacitor is connected between pins 5 and 9 to avoid a 150 kHz ripple at the average level.

- 6:7 Preamplifier input

The part of the preamplifier which is connected to pin 6 should be biased with a constant d.c. voltage of 2 V (typical). Therefore pin 6 is decoupled for the 150 kHz signal by means of a 2,2 nF capacitor. The sawtooth signal, which is composed of the sawtooth of the ramp generator and a feedback sawtooth from the output stage, is applied to the preamplifier input via pin 7 (by varying the ramp sawtooth amplitude, the height of the picture can be adjusted). The signal is nominally amplified 15 times and internally fed into the modulator, which then modulates the width of the 150 kHz pulses into a 50 Hz rhythm.

APPLICATION INFORMATION (continued)8. D.C. feedback reference voltage

A d.c. reference voltage with an imposed parabolic waveform is derived from the capacitor in series with the deflection unit and supplied into pin 8.

This feedback signal gives a proper biasing of the output stage.

9. Common of small signal stages

The common rail of the small signal stages must be connected to ground (pin 1) via a diode, avoiding common impedance with the "high current" ground leads.

10. Ramp generator output

A 50 Hz sawtooth signal with a nominal amplitude of 5 V is fed from pin 10 to the external components for amplitude and linearity control. The signal is also applied to the preamplifier input via a 3,9 k Ω resistor in series with a 4,7 μ F electrolytic capacitor.

11. Negative sync input and frequency control

The voltage to this pin is applied via an external 470 Ω variable resistor, and controls the timing capacitors charging level (connected to pin 12).

When the appropriate level is reached, the flyback starts. Pin 11 is also the input for negative-going sync pulses. The amplitude of these pulses determines the pull-in range of the oscillator. When sync pulses with a high amplitude are available a resistive divider circuit should be used to obtain the right pull-in range.

Because of the very high input impedance of the sync inverter input (pin 13), it is recommended that when negative-going sync is being employed, pin 13 should be connected to ground (pin 9) to avoid any leakage currents or "pick-up" disturbing the oscillator.

12. Ramp timing

The timing network comprises two capacitors in series between pins 12 and 9.

The linearity of the sawtooth can be adjusted by means of a controlled signal which is fed back from the output (pin 10) to the mid-tap of the capacitors.

13. Positive sync input

The ramp signal frequency can be synchronized by positive-going sync pulses with amplitudes between 2,5 V and 8 V peak-to-peak. The smaller amplitudes result in a smaller pull-in range. A series resistor of 4,7 k Ω , or (better) a resistive divider, should be used to obtain the correct pull-in range at those sync pulse amplitudes in excess of 8 V which have a low impedance.

14. Top drive input of power output stage

The top power transistor is driven from the 37 V supply via an external resistor of 1,5 k Ω .

APPLICATION INFORMATION (continued)

15. Positive supply

The maximum voltage to be applied is 40 V (42 V for short-term operation). The integrated circuit comprises an internal stabilized voltage of 14, 6 V to supply the small signal stages. This internal voltage stabilizer already operates at a supply voltage of 21 V, and enables the TDA2600 to drive deflection systems with supply voltages < 36 V.

16. Output

From pin 16 the 150 kHz square wave with 50 Hz modulated pulse-width is applied to an external low-pass filter. The resulting 50 Hz signal is fed to the vertical deflection unit. The maximum current derived from pin 16 is 7 A peak-to-peak.

SOUND OUTPUT CIRCUIT

The TDA2610 and TDA2610A are sound output circuits for use in colour and black and white television receivers.

The output circuit in the TDA2610 is a class-B arrangement and can deliver an output power of 7 W. A current stabilizing circuit is incorporated in the TDA2610A to obtain a constant current drain and an output power of 4 W is available.

This constant current mode allows the TDA2610A to be supplied by the horizontal output transformer.

Furthermore the TDA2610 and TDA2610A feature :

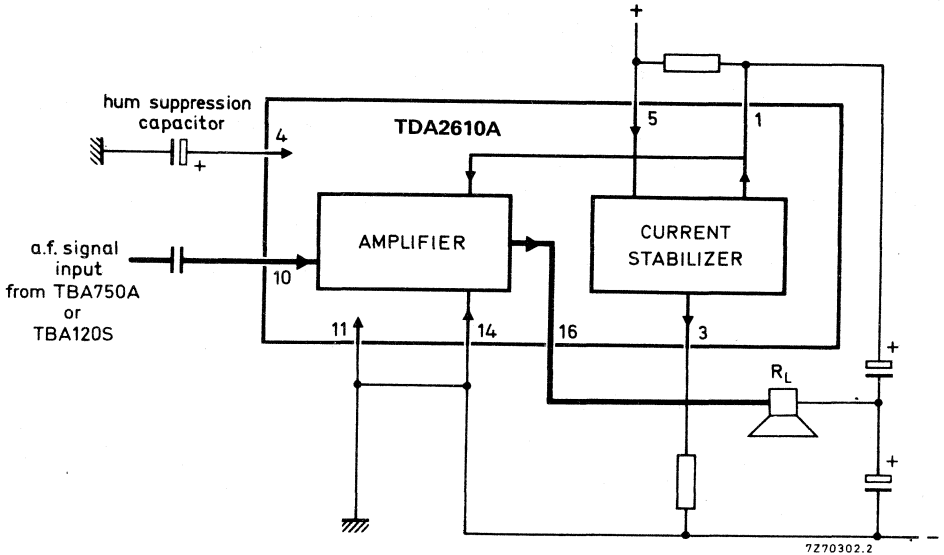
- short circuit protected output
- thermal shut-down circuit
- low number of external components

QUICK REFERENCE DATA				
Supply voltage	V ₅₋₁₁	typ.	25	V
Supply current	I ₅	typ.	300	mA
Load resistance	R ₁₆₋₁₁	typ.	15	Ω
Output power at f = 1 kHz; d _{tot} = 10%	P _O	typ.	4	W
Input voltage for P _O = P _O max	V ₁₀₋₁₁	typ.	100	mW
Input impedance	Z ₁₀₋₁₁	typ.	45	kΩ

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic power (SOT-69B).

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage at pin 5	V_{5-11}	max.	35	V
at pin 1	V_{1-11}	max.	35	V

Current

Output current (peak value)	I_{16M}	max.	2	A
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Power dissipation

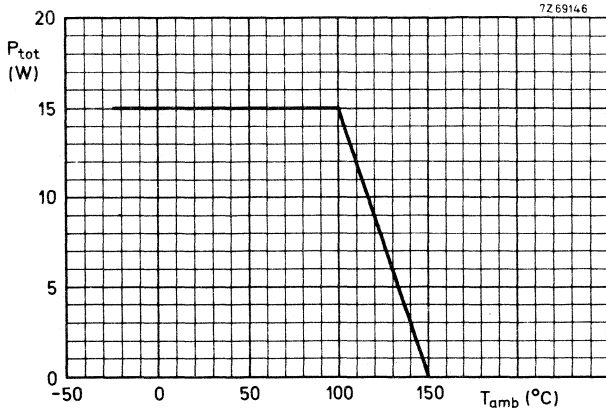
Total power dissipation see derating curve on page 3

Temperatures

Storage temperature	T_{stg}	-55 to +150	°C
Operating ambient temperature	T_{amb}	-25 to +150	°C

RATINGS (continued)

Power derating curve



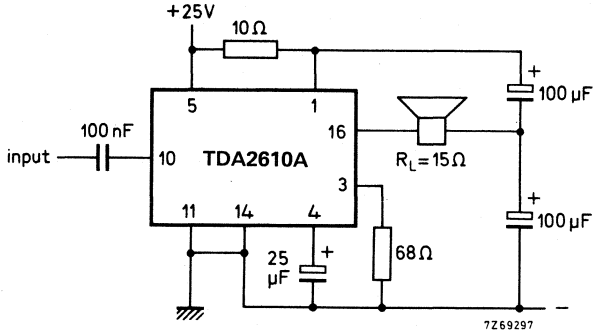
CHARACTERISTICS at T_{amb} = 25 °C; measured in the top circuit on page 4

<u>Supply voltage</u>	V ₅₋₁₁	typ.	25 V
			15 to 35 V
Performance at V ₅₋₁₁ = 25 V; R _L = 15 Ω; f = 1 kHz			
Stabilizing current	I ₄	typ.	0,3 A
		<	0,5 A
Output power at d _{tot} = 10%	P _o	typ.	4 W
Output current (repetitive peak value)	I _{16RM}	typ.	0,8 A
Input voltage for P _o = P _{o max}	V ₁₀₋₁₁	typ.	100 mV
Input impedance	Z ₁₀₋₁₁	typ.	45 kΩ
Frequency response	f	>	15 kHz
Noise output voltage at R _S = 5 kΩ; B = 60 Hz to 15 kHz	V ₁₆₋₁₁	<	0,5 mV

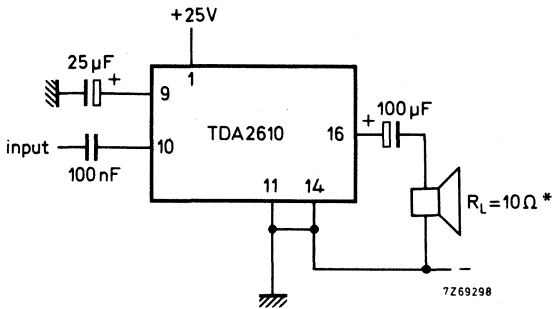
CHARACTERISTICS at T_{amb} = 25 °C; measured in the bottom circuit on page 4

Performance at V ₁₋₁₁ = 25 V; R _L = 10 Ω; f = 1 kHz			
Output power at d _{tot} = 10%	P _o	typ.	7 W
Output current (repetitive peak value)	I _{16RM}	typ.	1,2 A
Input voltage for P _o = 4 W	V ₁₀₋₁₁	typ.	90 mV
Total quiescent current	I _{tot}	typ.	22 mA

APPLICATION INFORMATION



Sound output circuit with shunt stabilizer ($P_O = 4 \text{ W}$)



Sound output circuit without shunt stabilizer ($P_O = 7 \text{ W}$)

* Obtained via a transformer.

TUNING VOLTAGE SWITCH AND DRIVER FOR PROGRAMME INDICATOR

The TDA2620 provides the drive for four digits of a gas-filled numeral indicator tube and effects the tuning voltage switching.

Temperature-compensated "floating" switches are used to select the tuning voltage.

Together, the TDA2620 and TDA2630 contain all the circuits for touch selection of four television programmes and generate the drive for a gas-filled numeral indicator tube to indicate the selected programme.

Selection and indication capacity can be extended to 8, 12 or 16 programmes by using additional pairs of ICs (one TDA2620 and one TDA2631).

QUICK REFERENCE DATA

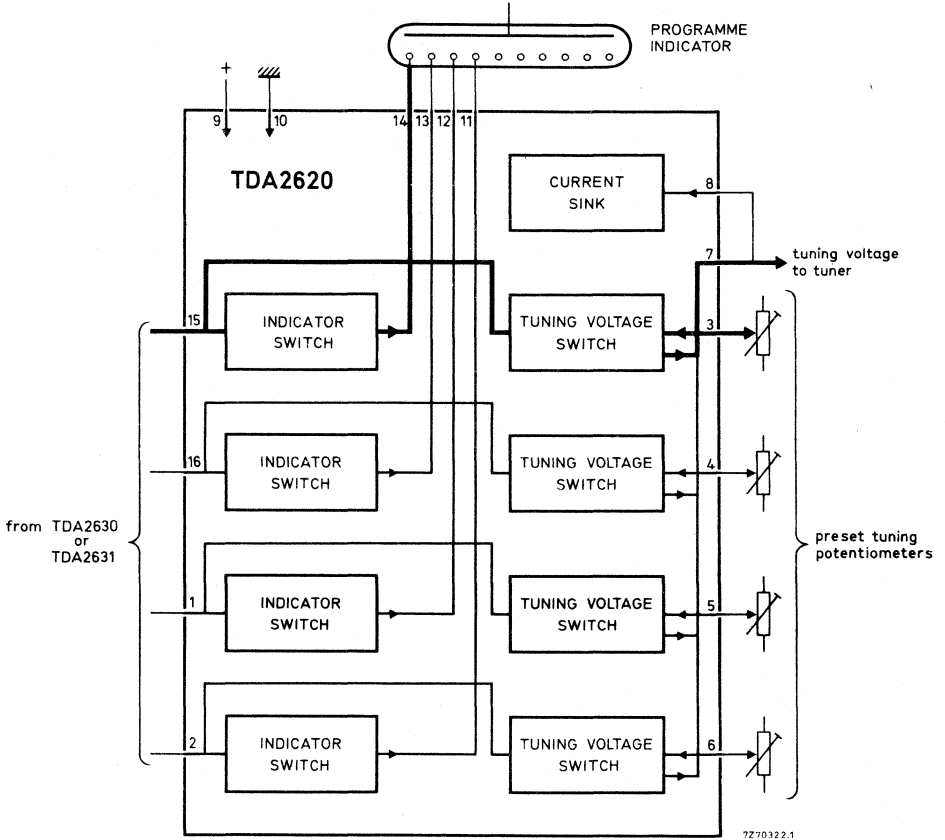
Supply voltage	V_{9-10}	typ.	33	V
Tuning output voltage at < 0,3 V on pins 3, 4, 5 and 6	V_{7-10}	<	0,3	V
Voltage drop of each switch		typ.	± 10	mV
Thermal drift of each switch		typ.	15	$\mu\text{V}/^\circ\text{C}$
Input voltage: switches active	$V_{1;2;15;16-10}$		0 to 2	V
switches non-active	$V_{1;2;15;16-10}$		10 to 16,5	V
Tuning voltage switch input current	$-I_3$	typ.	0,2	μA
Supply current (output pin 7: unloaded)	I_9	<	550	μA
(output pin 7: loaded)	I_9	<	800	μA
Output voltage: output selected (indication)	$V_{11;12;13;14-10}$	<	2,5	V
output not selected	$V_{11;12;13;14-10}$	>	60	V

PACKAGE OUTLINES (see general section)

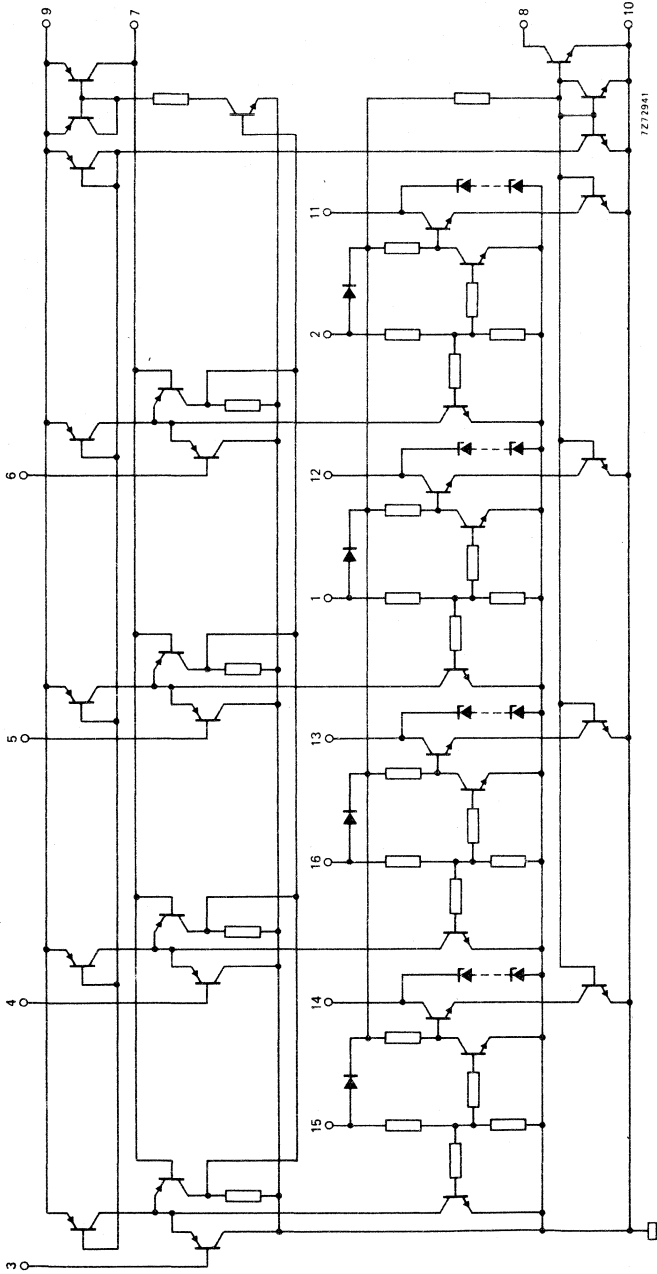
TDA2620 : plastic 16-lead dual in-line.

TDA2620Q : plastic 16-lead quadruple in-line.

BLOCK DIAGRAM



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage	V_{9-10}	max.	36	V
Voltage at pins 3, 4, 5 and 6	$V_{3;4;5;6-10}$	max.	36	V
Voltage at pins 1, 2, 15 and 16	$V_{1;2;15;16-10}$	max.	18	V

Currents

Output current at pins 11, 12, 13 and 14

output selected (indication) ¹⁾	$I_{11}, I_{12}, I_{13}, I_{14}$	max.	15	mA
output not selected ²⁾	$I_{11}, I_{12}, I_{13}, I_{14}$	max.	2	mA

Power dissipation

Total power dissipation	P_{tot}	max.	500	mW
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Temperatures

Storage temperature	T_{stg}	-20 to +125	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

CHARACTERISTICS at $V_{9-10} = 33$ V; $T_{amb} = 0$ to 70 °C; one channel preset; unless otherwise specified

Tuning output voltage³⁾

at $V_{3-10} < 0,3$ V	V_{7-10}	<	0,3	V
at $V_{3-10} = 0,3$ V to $V_{9-10}-1$ V	V_{7-10}	>	$V_{3-10}-25$	mV
		<	$V_{3-10}+25$	mV
at $V_{3-10} > V_{9-10}-1$ V	V_{7-10}	>	$V_{9-10}-1$	V

Tuning voltage switch input current

$-I_3, -I_4, -I_5, -I_6$	typ.	0,2	µA
	<	1,0	µA

Thermal drift of each switch

	typ.	15	µV/°C
	<	50	µV/°C

1) Output selected means that the output transistor is conducting and the numeral indicator tube shows appropriate number.

2) Output not selected means that the output transistor is non-conducting and current flows into voltage limiting circuit connected in parallel to the transistor.

3) The circuit consists of four identical indicator and tuning voltage switches. Values quoted for pin 3 also apply to pins 4, 5 and 6.

CHARACTERISTICS (continued)Output voltage at pins 11, 12, 13 and 14

output selected (indication);

$I_{11}, I_{12}, I_{13}, I_{14} = 8 \text{ mA}$ (see also note 1 p. 4)	$V_{11; 12; 13; 14-10}$	<	2,5	V ¹⁾
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output not selected;

$I_{11}, I_{12}, I_{13}, I_{14} = 0,5 \text{ mA}$ (see also note 2 p. 4)	$V_{11; 12; 13; 14-10}$	>	60	V
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Input voltage to indicator and tuning voltage switch

switches active	$V_{1; 2; 15; 16-10}$		0 to 2	V
-----------------	-----------------------	--	--------	---

switches non-active	$V_{1; 2; 15; 16-10}$		10 to 16,5	V
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Supply current²⁾at $V_{1; 2; 15; 16-10} = 16,5 \text{ V}$ (switches non-active) and

pin 7: unloaded	I_9	typ.	300	μA
-----------------	-------	------	-----	---------------

		<	550	μA
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pin 7: loaded (250 k Ω between pins 7 and 10)	I_9	<	800	μA
--	-------	---	-----	---------------

Input current to indicator and tuning voltage switch

switches non-active

$(V_{1; 2; 15; 16-10} = 10 \text{ to } 16,5 \text{ V})$	$\Sigma I_{1, I_2, I_{15}, I_{16}}$	typ.	13	mA
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Propagation delay from input to output

t_d	typ.	135	ms ³⁾
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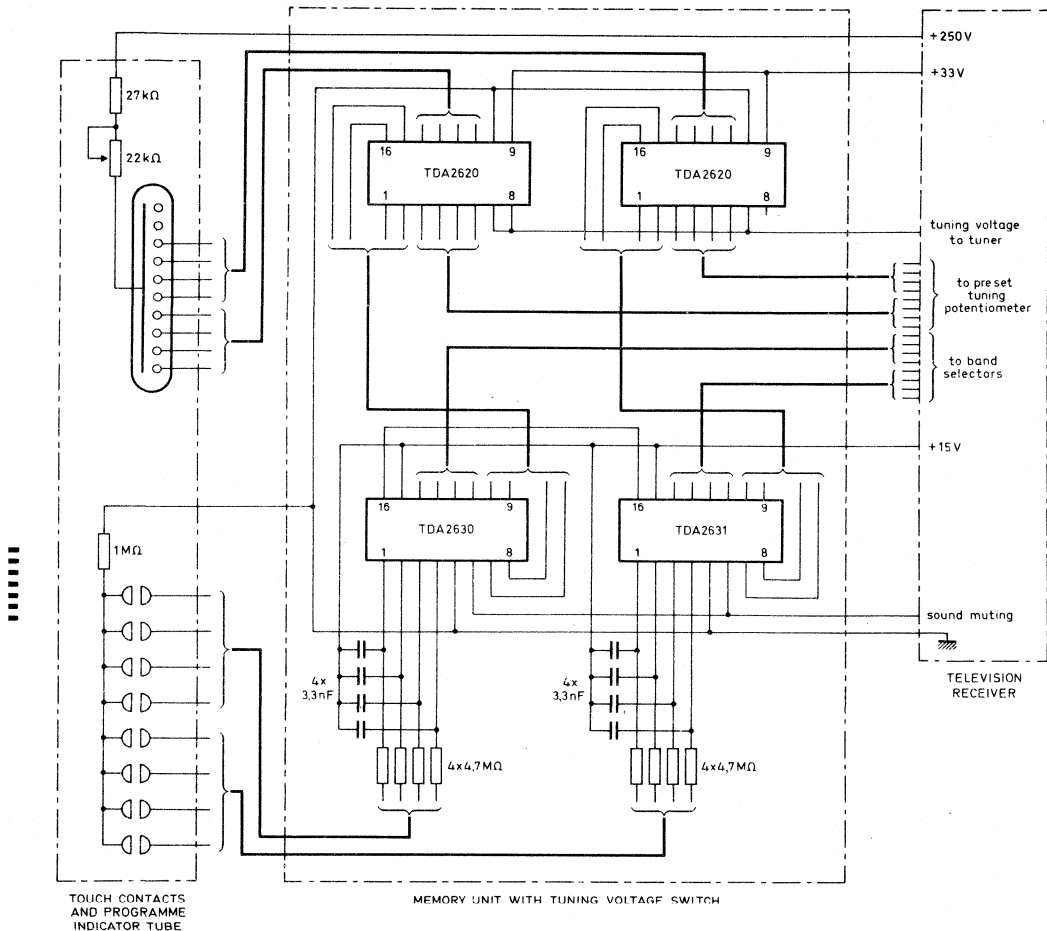
¹⁾ At a voltage $\geq 12 \text{ V}$ at pins 1, 2, 15 and 16 (switches non-active) an output current at pins 11, 12, 13 and 14 of 8 mA will be guaranteed at $V_{11; 12; 13; 14-10} < 2,5 \text{ V}$.
The IC includes a current limiting circuit to avoid switching transients.

²⁾ The supply current with pin 7 not loaded is typ. 300 μA . If pin 7 is loaded, I_9 increases by twice the load current; when extending the system (to 8, 12 or 16 programmes), the total current I_9 rises by 100 μA per additional connected TDA2620.

³⁾ At a load capacitance of max. 0,5 μF between pins 7 and 10, $V_{1; 2; 15; 16-10} = 14 \text{ V}$ and V_{7-10} increased to 27 V.

APPLICATION INFORMATION

Touch control circuit for 8 programmes with 2 x TDA2620, TDA2630 and TDA2631.



TOUCH AMPLIFIER, LOGIC AND BAND SELECTION SWITCH

The TDA2630 provides amplification and "memorizing" of the touch signals, band switching and automatic resetting to the same programme after switch-on.

Facilities are provided for muting the receiver sound circuits during programme switching. The logic information from the output of the selected touch amplifier is stored in a latch (flip-flop) and is also used to reset the latches associated with the remaining touch contacts. The same signal also activates the sound muting circuit.

Together, the TDA2630 and TDA2620 contain all the circuits for touch selection of four television programmes and generate the drive for a gas-filled numeral indicator tube to indicate the selected programme.

Selection and indication capacity can be extended to 8, 12 or 16 programmes by using additional pairs of ICs (one TDA2620 and one TDA2631).

The TDA2631 is similar to the TDA2630 except for omission of the switch-on reset facility which is not required in the additional ICs that are only used for extending the selection capacity of the system.

QUICK REFERENCE DATA

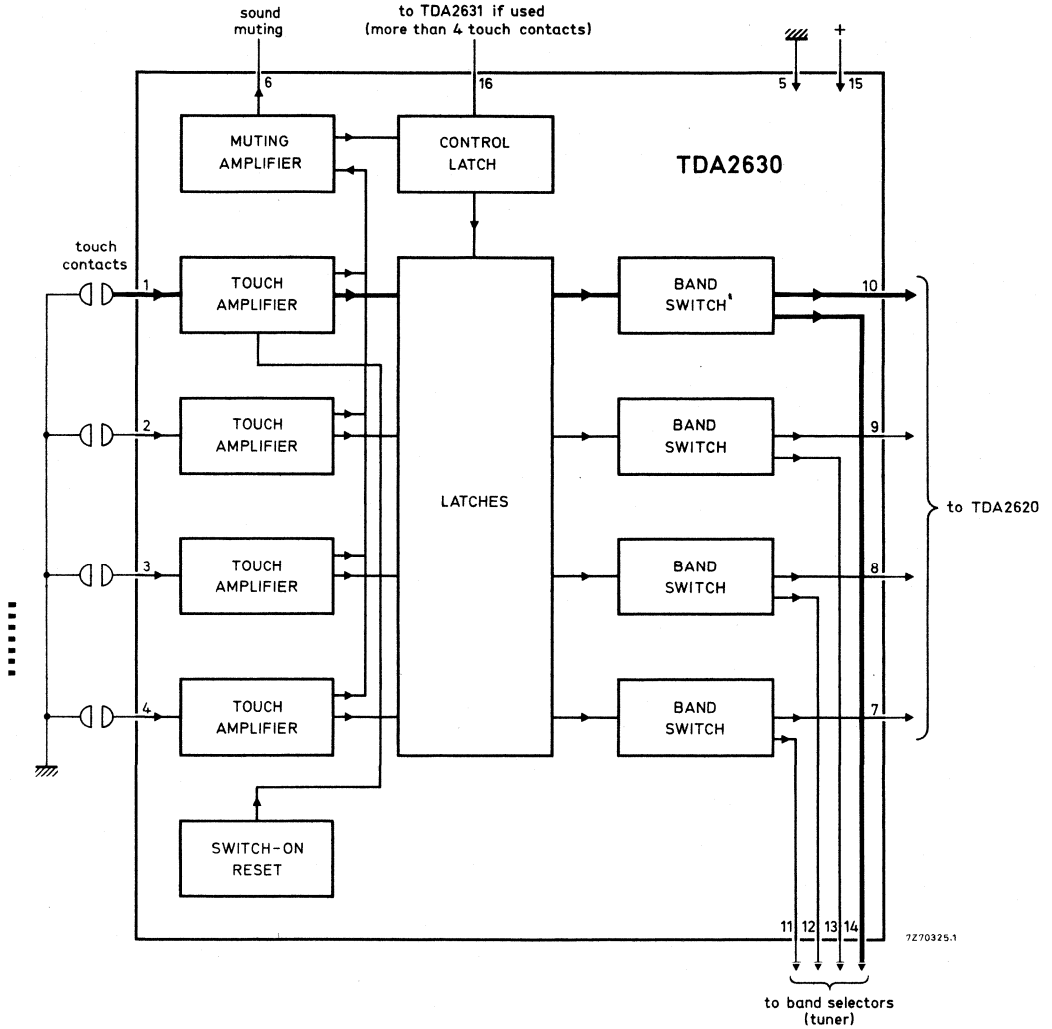
Supply voltage	V_{15-5}	typ.	15	V
Supply current	I_{15}	typ.	8,5	mA
Resistance parallel to input				
to set latch	$R_{1;2;3;4-5}$	<	25	M Ω
at which latch will not be set	$R_{1;2;3;4-5}$	>	50	M Ω
Input current				
to set latch	$I_{1;I_2;I_3;I_4}$	>	500	nA
at which latch will not be set	$I_{1;I_2;I_3;I_4}$	<	250	nA
Muting amplifier output voltage at $I_6 = 5$ mA	V_{6-5}	<	1,5	V

PACKAGE OUTLINES (see general section)

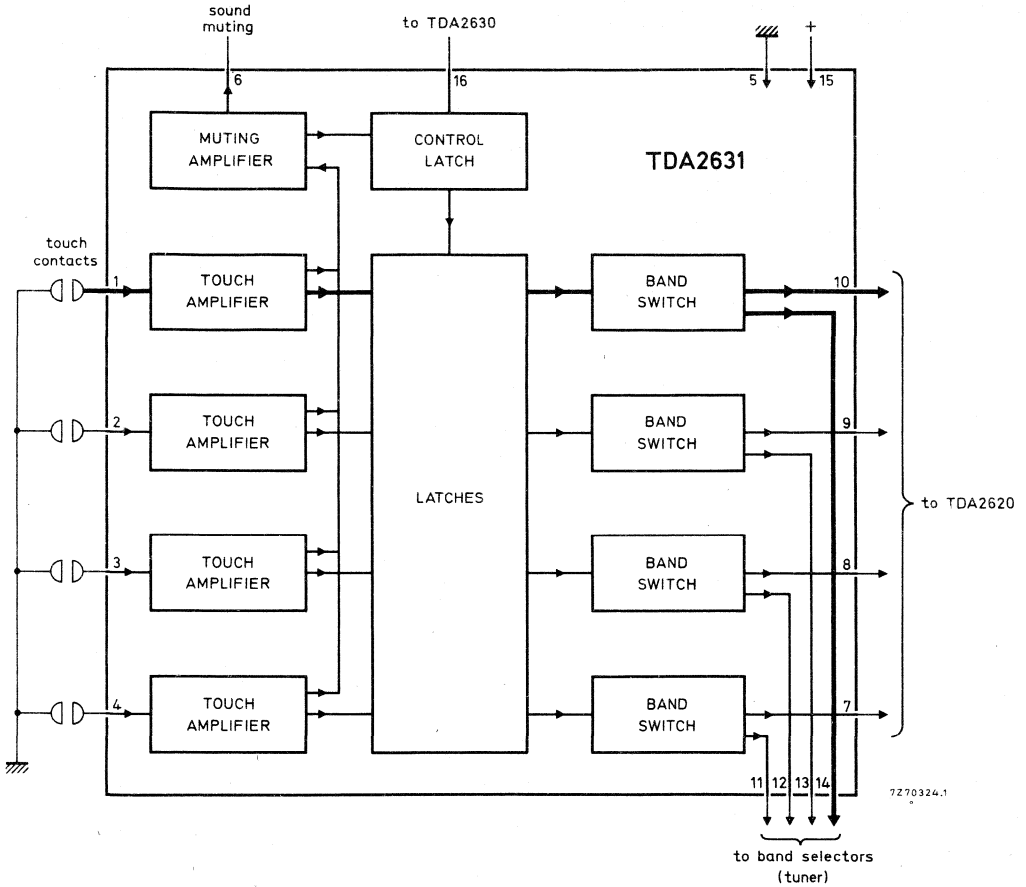
TDA2630 : TDA2631 : plastic 16-lead dual in-line.

TDA2630Q; TDA2631Q: plastic 16-lead quadruple in-line.

BLOCK DIAGRAM



BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage	V_{15-5}	max.	20 V
Touch amplifier input voltage	$V_{1;2;3;4-5}$	max.	V_{15-5} V

Currents

Output current of band switches to TDA2620	$-I_7, -I_8, -I_9, -I_{10}$	max.	15 mA
Output current to band selectors	$-I_{11}, -I_{12}, -I_{13}, -I_{14}$	max.	50 mA
	$\Sigma -I_{11}, -I_{12}, -I_{13}, -I_{14}$	max.	80 mA
Output current muting amplifier	I_6	max.	8 mA
Current at pin 16	I_{16}	max.	500 μ A

Power dissipation

Total power dissipation	P_{tot}	max.	500 mW
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Temperatures

Storage temperature	T_{stg}	-20 to +125 °C
Operating ambient temperature	T_{amb}	0 to +70 °C

CHARACTERISTICS at $V_{15-5} = 15$ V ¹⁾; $T_{amb} = 0$ to +70 °C; one channel activated; unless otherwise specified

<u>Supply current</u>	I_{15}	typ.	8,5 mA
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<u>Power dissipation</u>	P_{tot}	typ.	200 mW
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Touch amplifier (input sensitivity)

Resistance parallel to input

to set latch	$R_{1;2;3;4-5}$	<	25 M Ω
at which latch will not be set	$R_{1;2;3;4-5}$	>	50 M Ω

Input current

to set latch	I_1, I_2, I_3, I_4	>	500 nA
at which latch will not be set	I_1, I_2, I_3, I_4	<	250 nA

Band switch output (to TDA2620)

Output voltage when latch is set ($R_L = 10$ k Ω)	$V_{7;8;9;10-5}$	<	2 V
Output voltage when latch is not set	$V_{7;8;9;10-5}$	>	9 V
Output current when latch is not set	$-I_7, -I_8, -I_9, -I_{10}$	<	4 mA

Muting amplifier output

Output voltage when active ($I_6 = 5$ mA)	V_{6-5}	<	1,5 V
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¹⁾ Supply voltage range 11,5 to 16,5 V.

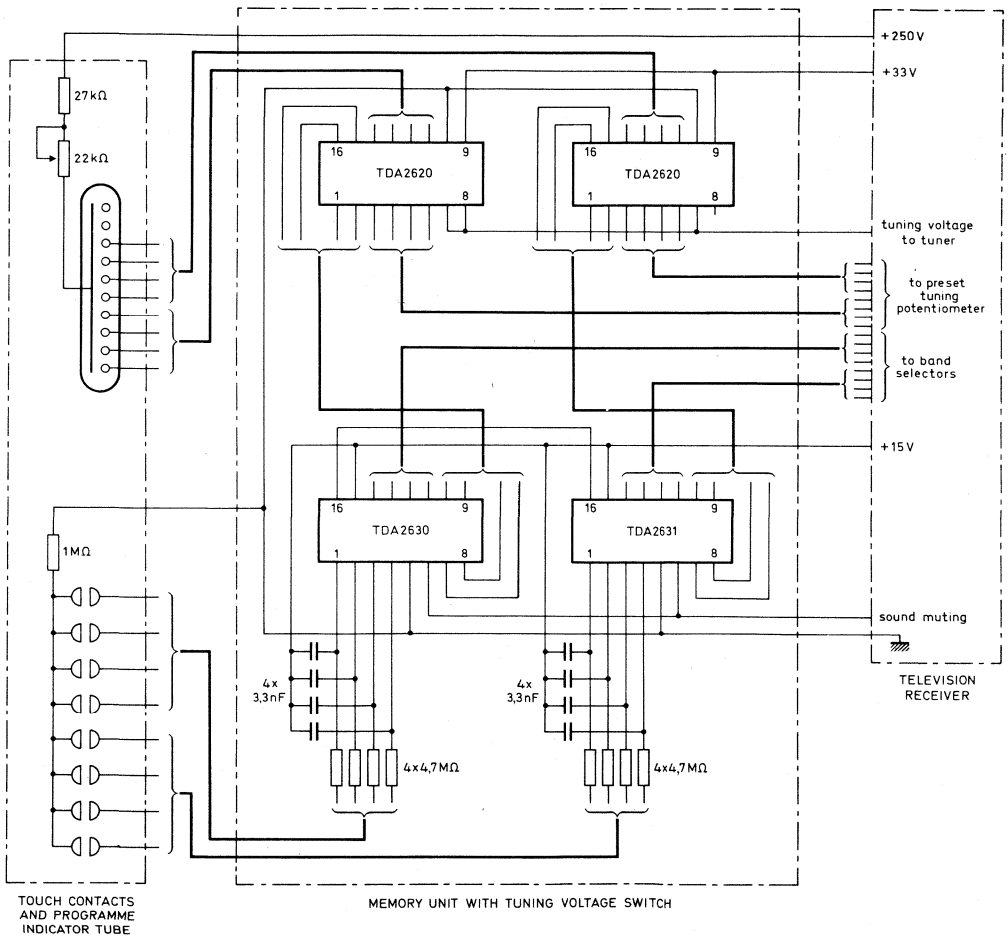
CHARACTERISTICS (continued)

Output to band selectors

Output current ¹⁾	$-I_{11}, -I_{12}, -I_{13}, -I_{14}$	<	35	mA
Voltage drop at 35 mA	$-V_{11; 12; 13; 14-15}$	<	1,5	V
Leakage current at $V_{11; 12; 13; 14-5} = -5$ V		<	250	nA

APPLICATION INFORMATION

Touch control circuit for 8 programmes with 2 x TDA2620, TDA2630 and TDA2631.



¹⁾ The outputs may be loaded during $t \leq 2$ s with a resistance of 39Ω .

SWITCHED-MODE POWER SUPPLY DRIVE CIRCUIT

The TDA2640 is a monolithic integrated circuit for driving the switched-mode power supply of a colour or black and white television receiver.

Except for the drive and output voltage stabilizing circuitry the TDA2640 incorporates the following functions:

- fixed frequency determined by external components
- remote switch off and restart
- over-current protection
- over-voltage protection
- slow starting
- low-supply voltage protection
- open-circuit feedback protection
- optional synchronization

QUICK REFERENCE DATA

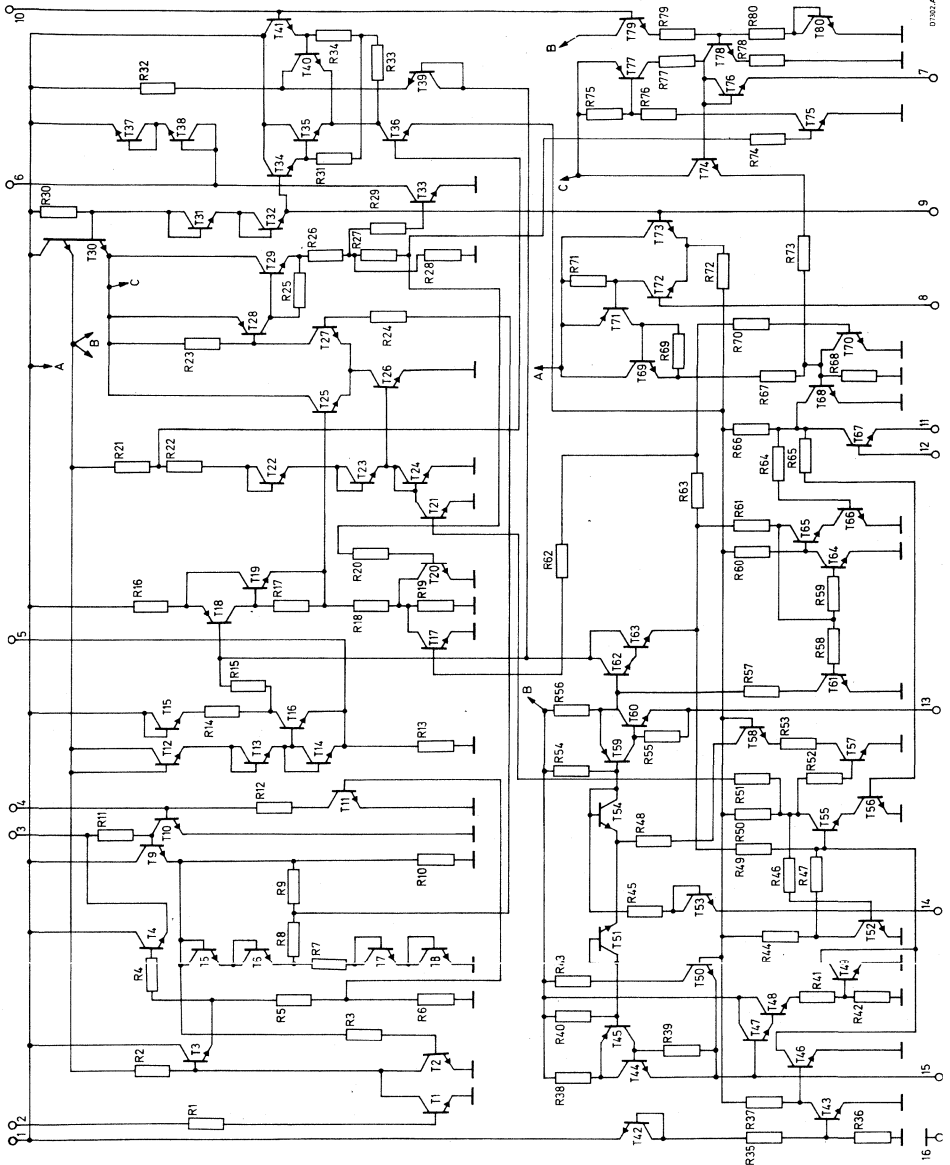
Supply voltage	V_{1-16}	typ.	12	V
Supply current	I_1	typ.	8,1	mA
Output voltage (peak-to-peak value)	$V_{6-16(p-p)}$	>	11,5	V
Output current (peak value)	I_{6M}	<	20	mA
Duty factor of output pulse	δ	typ.	20 to 85	%
Reference input voltage	V_{9-16}	typ.	6,2	V
Sync pulse (peak-to-peak value)	$V_{2-16(p-p)}$		1 to 10	V

PACKAGE OUTLINES (see general section)

TDA2640 : 16-lead DIL; plastic.

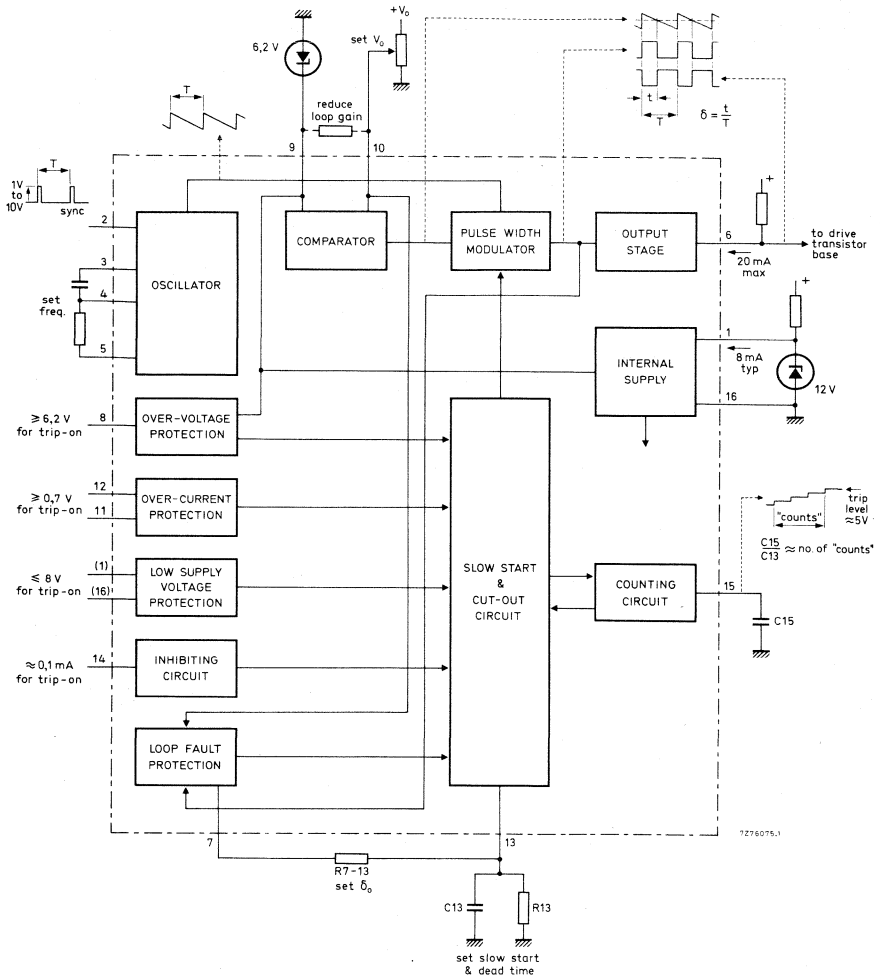
TDA2640Q: 16-lead QIL; plastic.

CIRCUIT DIAGRAM



00004A

BLOCK DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Supply voltage	V_{1-16}	max.	13,8 V
Pin 2	V_{2-16}		-5 to +10 V
Pin 8	V_{8-16}		0 to +10 V
Pin 9	V_{9-16}		0 to +10 V
Pin 10	V_{10-16}		0 to $V_{9-16} + 1$ V
Pin 9 with respect to pin 10	V_{9-10}		-1 to +7 V
Pin 11 (pin 12 not connected)	V_{11-16}		-1 to 0 V

Current

Output current (peak value)	I_{6M}	max.	20 mA
-----------------------------	----------	------	-------

Power dissipation

Total power dissipation	P_{tot}	max.	145 mW
-------------------------	-----------	------	--------

Temperatures

Storage temperature	T_{stg}		-55 to +125 °C
Operating ambient temperature	T_{amb}		-25 to +65 °C

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C

Supply current at $\delta = 50\%$	I_1	typ.	8,1 mA
			5,1 to 10,4 mA
Reference voltage		typ.	6,2 V ¹⁾
			5,6 to 6,5 V
Sync pulse (peak-to-peak value)	$V_{2-16(p-p)}$		1 to 10 V
Remote switch: inhibit (switched off)	V_{14-16}		0 to 3 V
normal (switched on)	V_{14-16}		5 to 12 V ²⁾
Over-voltage protection: threshold voltage	V_{8-16}	typ.	6,2 V ³⁾
input current	I_8	typ.	2 μ A
temperature coefficient		typ.	0,1 mV/°C
Over-current protection: threshold voltage	V_{12-11}		660 to 760 mV ⁴⁾
Low supply voltage protection: threshold voltage	V_{1-16}	typ.	8,6 V
			8 to 9,5 V
Horizontal drive pulse (peak-to-peak value)	$V_{6-16(p-p)}$	>	11,5 V ⁵⁾
Duty factor of output pulse: maximum	δ_{max}	>	85 % ⁶⁾
		typ.	90 %
minimum	δ_{min}	typ.	15 %
		<	20 %

For notes see page 5.

CHARACTERISTICS (continued)

Saturation voltage of output transistor at $I_6 = 20 \text{ mA}$	V_{CEsat}	typ. <	280 mV 400 mV
Feedback input impedance at pin 10	$ Z_{10-16} $	typ.	100 k Ω
Temperature coefficient for constant duty factor at pin 10		typ.	0,3 mV/ $^{\circ}\text{C}$
Oscillator frequency spread (with fixed external components)		<	$\pm 3 \%$
Rise time of leading edge of output pulse		typ.	0,1 μs

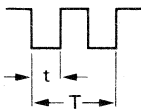
PINNING

- | | |
|---|---|
| 1. Positive supply | 9. Reference input |
| 2. Sync pulse input | 10. Feedback voltage input |
| 3. Oscillator timing capacitor | 11. Over-current protection input (emitter) |
| 4. Junction of oscillator timing C and R | 12. Over-current protection input (base) |
| 5. Oscillator timing resistor | 13. Slow start C and R controlling network |
| 6. Output | 14. Inhibitor |
| 7. Low feedback protection external
resistor | 15. Re-start count capacitor |
| 8. Over-voltage protection input | 16. Negative supply (ground) |

Notes (from page 4)

1. Voltage obtained via an external reference diode (6,2 V).
2. Or pin 14 not connected.
3. The over-voltage protection threshold is equal to the reference voltage $V_{9-16} \pm 50 \text{ mV}$.
4. The temperature coefficient is typ. $-1,7 \text{ mV}/^{\circ}\text{C}$ (pin 11 or pin 12 can be connected to pin 16).
5. The maximum voltage on pin 6 is limited to approximately the supply voltage (pin 1) by an internal diode.
6. Valid for normal operating conditions. The circuit starts with 0% duty factor, controlled by the switch-on circuit; the duty factor then rises to the normal operating value.

The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%$$

APPLICATION INFORMATION (see circuits on pages 3 and 8)

The function is quoted against the corresponding pin number

1. 12 V positive supply

The maximum voltage that may be applied is 13,8 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 1 and 16 to ensure that the maximum voltage does not exceed 13,8 V. When the voltage on this pin falls below a minimum of 8 V the protection circuit will switch off the power supply.

2. Sync pulse input

The switching repetition rate may be synchronized to a source of positive-going sync pulses between 1 and 10 V. The free-running frequency of the TDA2640 oscillator must be above the synchronized frequency.

The minimum duration of the sync pulses is the difference between the period of the oscillator pulses and the period of the sync pulses. Synchronization reduces the maximum obtainable duty factor. If synchronization is not required, connect pin 2 to pin 16.

3, 4 and 5. Oscillator timing network

The timing network consists of a capacitor connected between pins 3 and 4, and a resistor connected between pins 4 and 5. The value of these components determines the switching period of the SMPS drive pulses.

6. Output

An external resistor connected between this pin and the supply rail determines the base drive current for the drive transistor. The integrated output circuit consists of an n-p-n transistor with a catching diode connected between its collector and an internal 12 V supply. This provides a low impedance in the "ON" state, that is with the drive transistor turned off.

7. Low feedback protection

An external resistor connected between this pin and pin 13 determines the maximum obtainable duty factor for the output pulses if the feedback voltage (pin 10) remains below the specified limit during starting.

8. Over-voltage protection

A voltage that is proportional to the power supply output voltage can be connected to this pin to operate a protection circuit if a threshold level is exceeded. The threshold level is determined by the external voltage reference diode connected to pin 9 (6,2 V nominal). If over-voltage protection is not required, pin 8 should be connected to pin 16.

9. Reference input

An external voltage reference diode (6,2 V nominal) must be connected between this pin and pin 16. The stability of the reference source determines the overall stability of the power supply output voltage. The voltage reference diode current is derived from within the integrated circuit; it has a typical value of 0,8 mA.

APPLICATION INFORMATION (continued)

10. Feedback voltage input

The control loop input is applied to pin 10. This pin is internally connected to one input of a differential error amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 9. Under normal operating conditions with the comparator at balance, the voltage on pin 10 will be about equal to the reference voltage on pin 9 (6,2 V), and the d.c. feedback factor of the external network should be designed for this value.

11 and 12. Over-current protection

A voltage proportional to the output current of the SMPS is applied to these pins. Pin 11 is connected to the emitter of an internal n-p-n detection transistor; pin 12 is connected to its base. Either of these pins may be grounded (pin 16) depending on the polarity of the input during increasing current. For example, if pin 11 is grounded the trip level on pin 12 is 660 mV to 760 mV; if pin 12 is grounded, the trip level on pin 11 is -660 mV to -760 mV.

13. Slow start

A resistor and capacitor in parallel must be connected between this pin and pin 16 (1 μ F and 390 k Ω). This network controls the rate at which the duty factor of the SMPS drive pulses increases to its normal operating value after switch-on. This minimizes inrush current. The network also influences the repetition period of the slow start during a fault.

14. Inhibitor

The power supply is switched off if the voltage on this pin is between 0 V and 3 V ($-I_{14} > 0,1$ mA). The power supply is switched on if this pin is not connected, or is connected to a voltage of between 5 V and the 12 V supply. The slow start and protection circuits remain operative under both conditions.

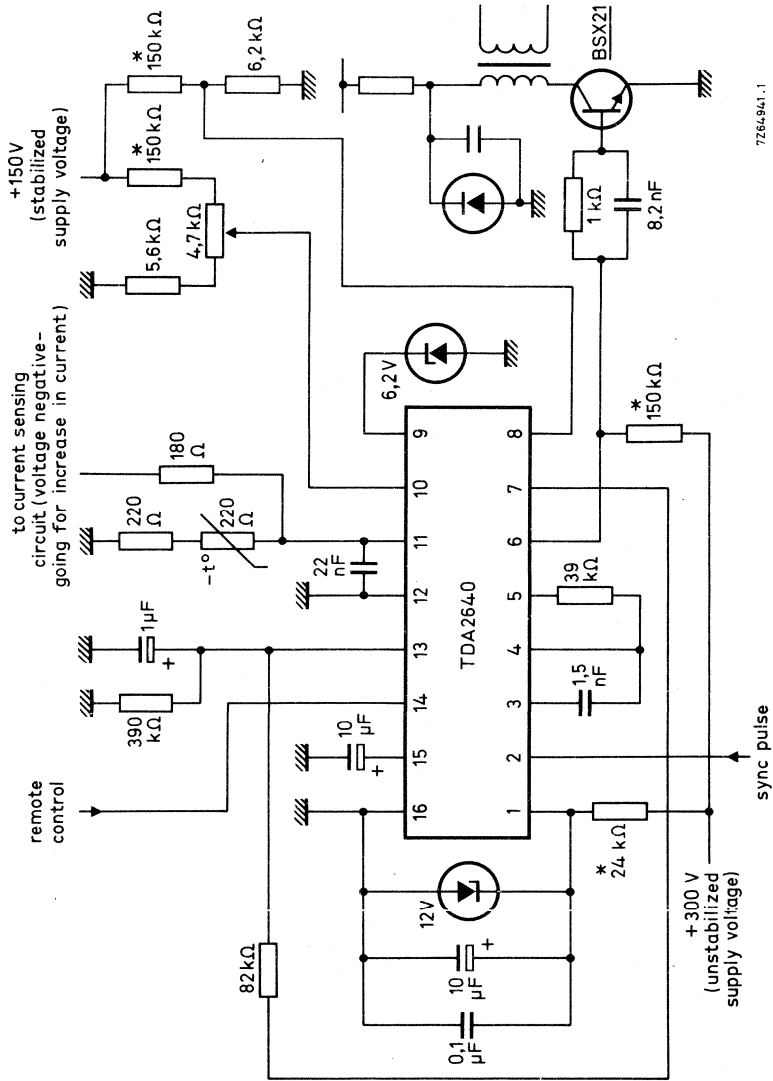
15. Re-start count capacitor

An external capacitor (C15 = 10 μ F) should be connected between pins 15 and 16. This capacitor controls the characteristics of the protection circuits as follows. When the protection circuit operates due to a fault, the duty factor of the drive pulses is reduced to zero. After an interval determined by the time-constant of the circuit connected to pin 13, the duty factor of the pulses slowly increases toward its normal operating value. If the fault persists, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated. The number of times that the cycle is repeated before the power supply drive pulses are permanently discontinued is determined by the value of the capacitor connected to pin 15. The number of counts is roughly C15/C13.

16. Negative supply (ground)

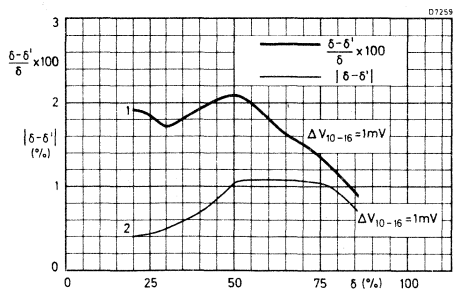
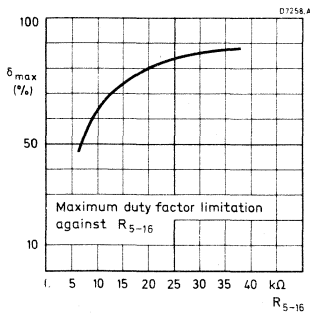
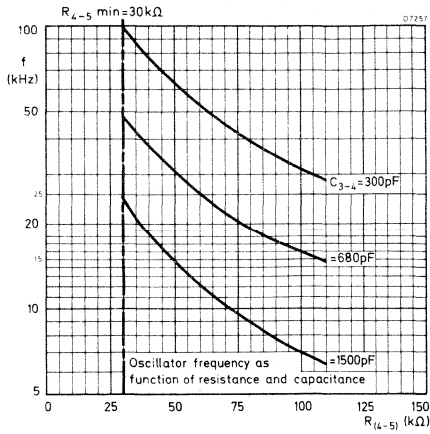
TDA2640
TDA2640Q

APPLICATION INFORMATION (continued)



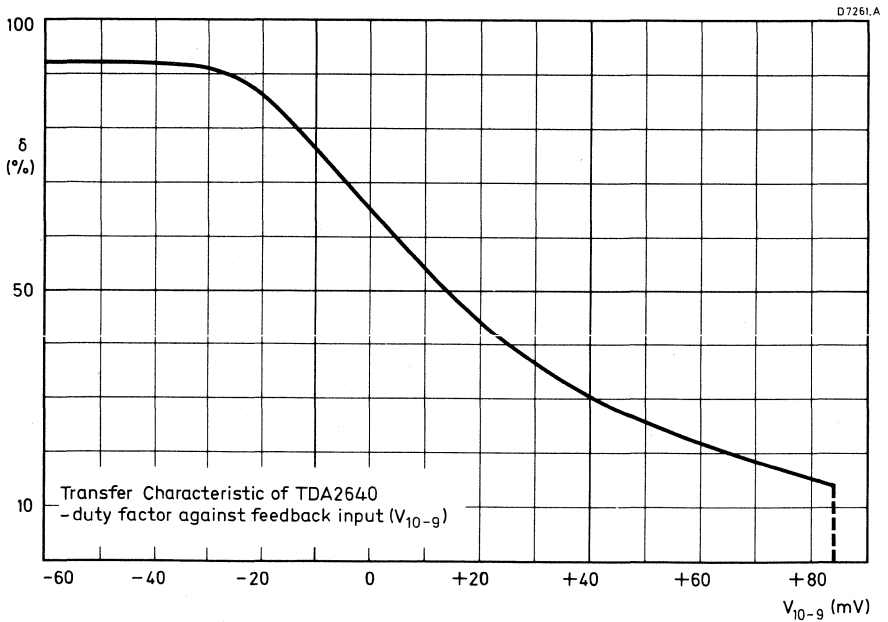
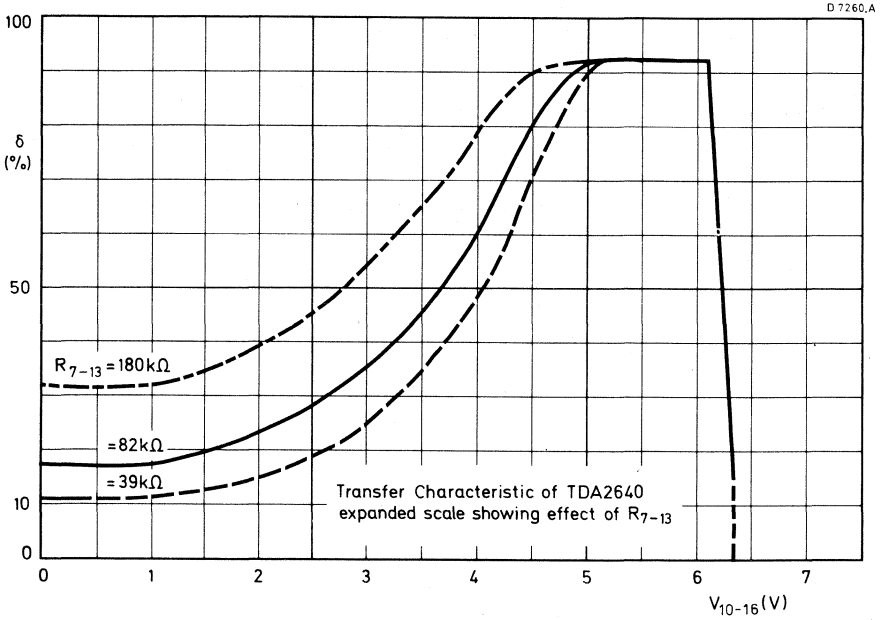
7Z56/94/1.1

Note: To operate with other supply and output voltages, alternative values of resistors marked thus * must be chosen.



1. Change of transfer characteristic against duty factor for $\Delta V_{10-16} = 1 \text{ mV}$.
2. Percentage change of transfer characteristics against duty factor for $\Delta V_{10-16} = 1 \text{ mV}$.

TDA2640
TDA2640Q



TELEVISION I.F. AMPLIFIER-DEMODULATOR

The TDA2670 is an i. f. amplifier and demodulator circuit for black and white television receivers.

It incorporates the following functions:

- gain-controlled wide-band amplifier;
- passive synchronous demodulator;
- video pre-amplifier with white-spot inverter (inverts the white noise peaks to grey).

The TDA2670 is primarily designed to be used in conjunction with the TBA 890 or TBA 900. The latter circuits provide the automatic gain control voltage for the i. f. amplifier in this device.

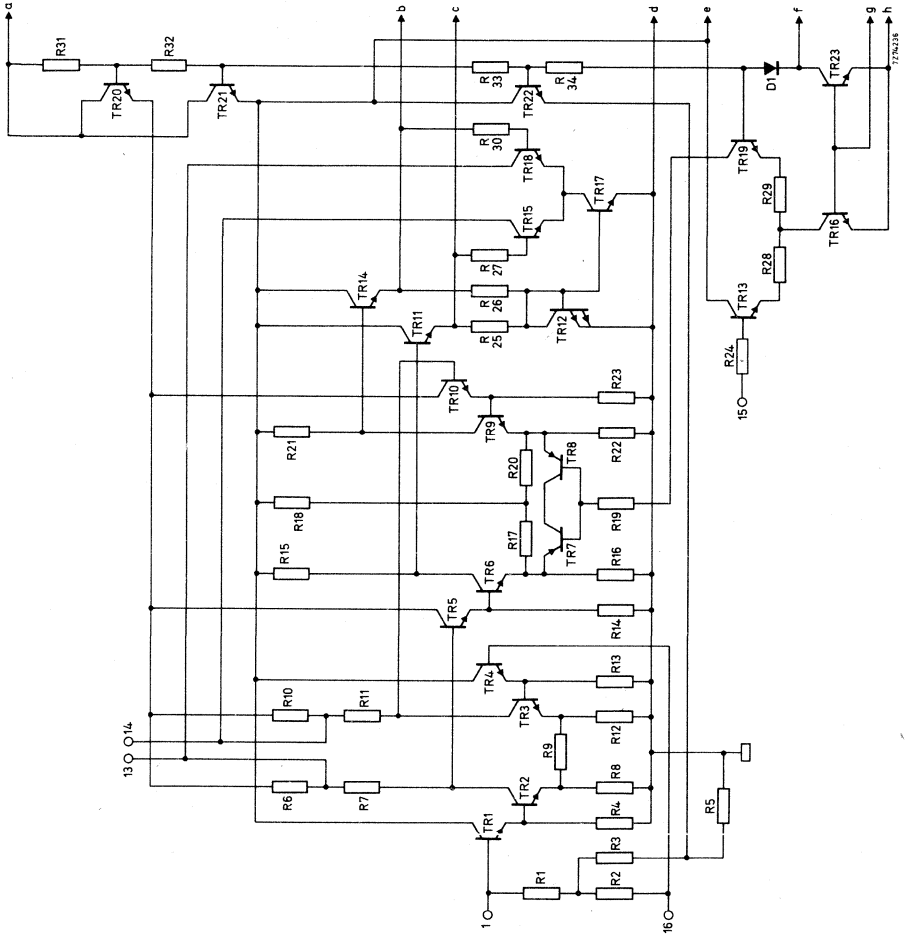
QUICK REFERENCE DATA

Supply voltage	$V_{4-3; 10}$	typ.	12	V
Supply current	I_4	typ.	35	mA
I. F. input voltage (r. m. s. value)	$V_{1-16(\text{rms})}$	typ.	900	μV
Video output voltage (peak-to-peak value)	$V_{6-3; 10(\text{p-p})}$	typ.	2,7	V
I. F. voltage gain control range	G_v	typ.	23	dB
Signal-to-noise ratio at 23 dB gain control	S/N	typ.	59	dB
Intermodulation at 1, 1 MHz and 3, 3 MHz		typ.	52	dB

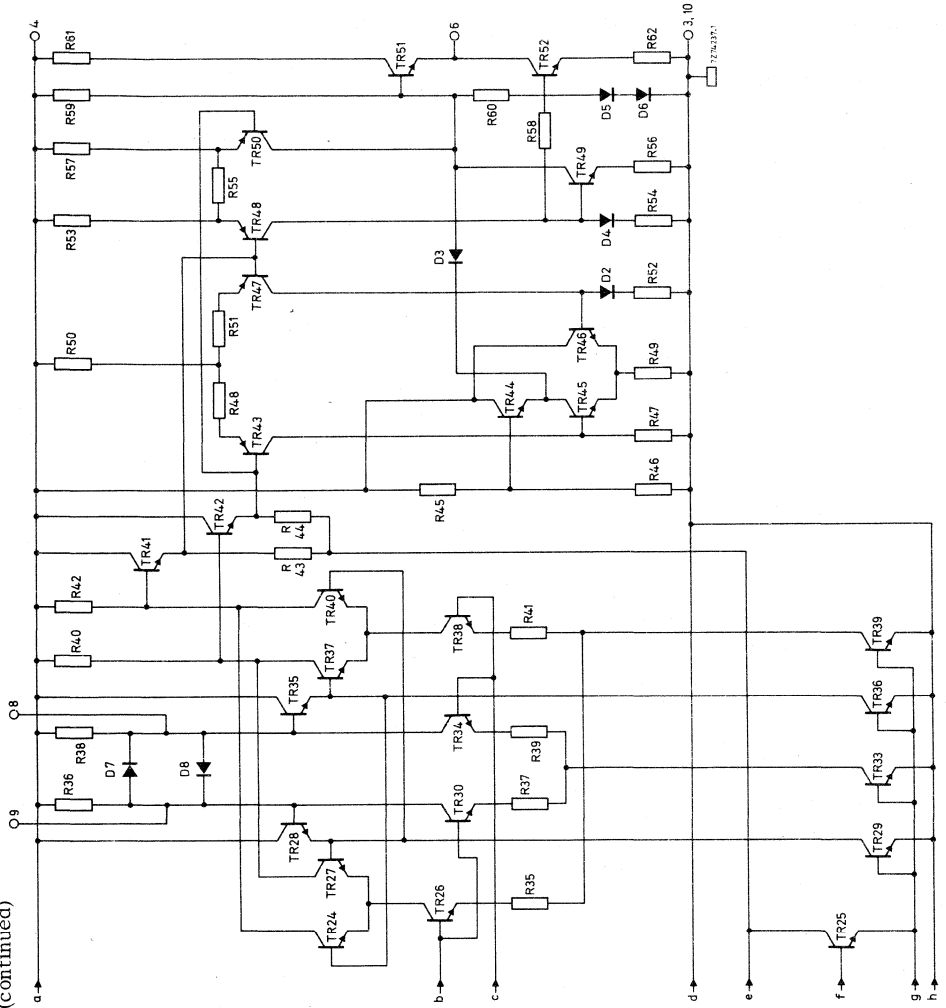
PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)

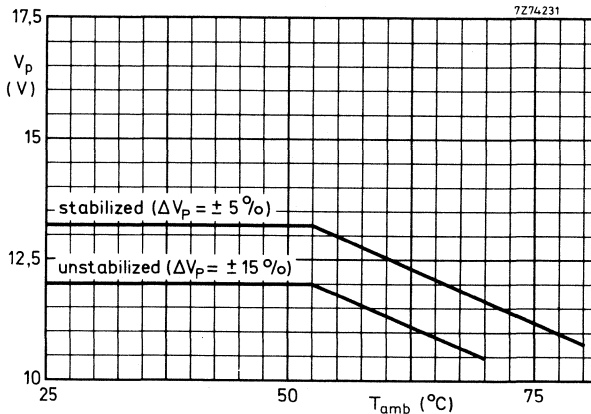


RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

<u>Supply voltage</u> (pin 4)	V_p	max.	14	V
<u>Power dissipation</u>	P_{tot}	max.	720	mW
<u>Temperatures</u>				
Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		-25 to +80	°C

CHARACTERISTICS

Supply voltage range see curves below



Maximum permissible nominal supply voltage as a function of the maximum ambient temperature.

The following characteristics are measured in the circuit on page 7 at $T_{amb} = 25$ °C;
 $V_{4-3} = V_{4-10} = 12$ V.

<u>Supply current</u>	I_4	typ.	35	mA
Required input signals				
I. F. input voltage (r. m. s. value)	$V_{1-16(rms)}$	typ.	900	μV 1)
Input impedance	$ Z_{1-16} $	typ.	3 k Ω in parallel with 4 pF	
White-spot inverter: threshold level clamping level	$V_{6-3;10}$	typ.	6,6	V
	$V_{6-3;10}$	typ.	4,7	V

1) Top sync level of an i. f. signal modulated in accordance with CCIR standard. Top sync level 0% modulation, peak of white signal 90% modulation.

CHARACTERISTICS (continued)

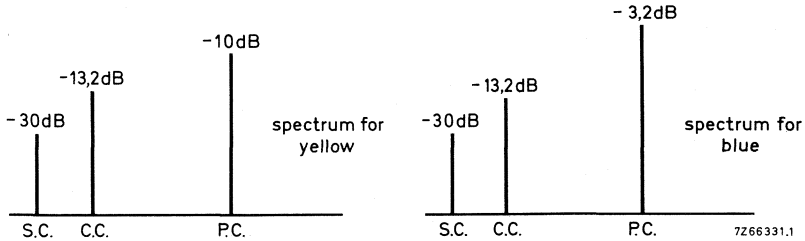
Obtainable output signals

Video output voltage (peak-to-peak value)	$V_{6-3; 10(p-p)}$	typ.	2,7	V ¹⁾
Zero signal output level	$V_{6-3; 10}$	typ.	6	V ²⁾
Top sync output level	$V_{6-3; 10}$	typ.	3	V

Performance

I. F. voltage gain control range	G_V	typ.	23	dB ³⁾
Signal-to-noise ratio at 23 dB a. g. c.	S/N	typ.	59	dB ⁴⁾
Differential gain	dG	<	10	%
Differential phase	$d\phi$	<	10 ^o	
Intermodulation at 1, 1 MHz		>	46	dB ⁵⁾
at 3, 3 MHz		>	46	dB ⁵⁾

Input conditions for intermodulation measurements:
 standard colour bar with 75% saturation and 75% contrast



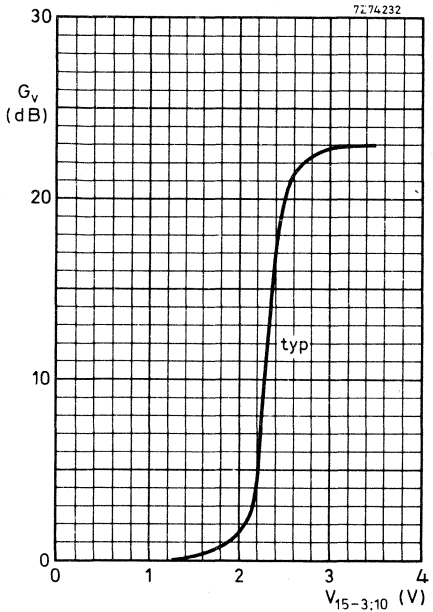
S. C. : sound carrier level
 C. C. : chrominance carrier level
 P. C. : picture carrier level

} with respect to top sync level

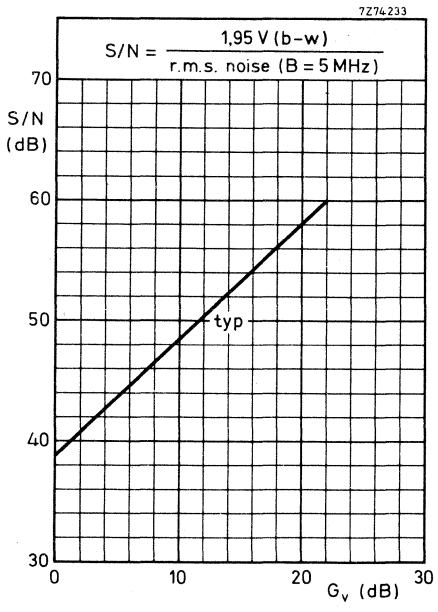
The sound-chrominance beat suppression is related to the B. W. amplitude with a peak-to-peak value of 2,7 V. Unmodulated carrier = 0 dB.

Bandwidth (3 dB)	B	>	4,5	MHz
Carrier frequency rejection at output		>	40	dB

- 1) The quoted i. f. input signal level is required to obtain the specified output.
- 2) The zero output level changes proportionally with the supply voltage.
- 3) See gain control graph on page 6.
- 4) See S/N graph on page 6.
- 5) See test set-up for intermodulation on page 6.

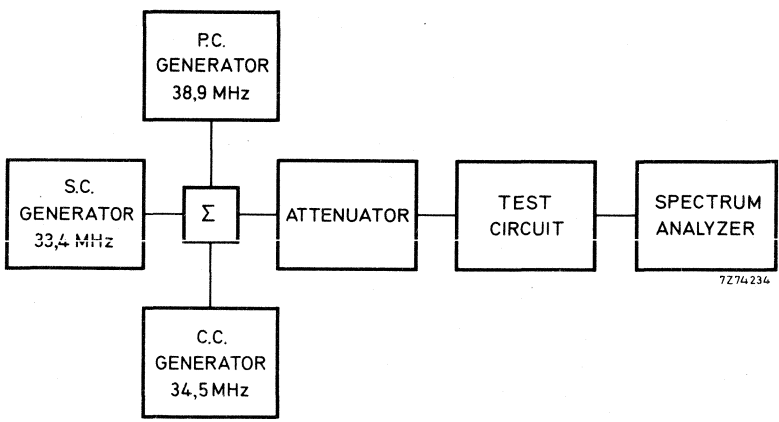


Gain control characteristic.



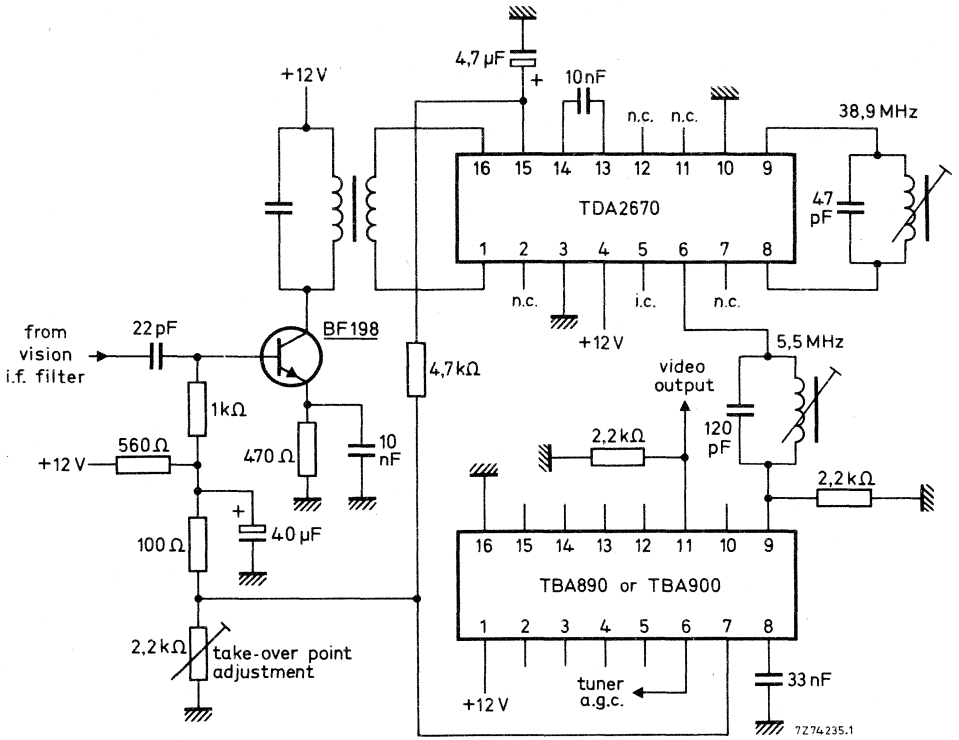
Signal-to-noise ratio as a function of gain control.

Test set-up for intermodulation



Intermodulation = $\frac{1,95 V (b-w)}{\text{peak-to-peak value of 1, 1 or 3,3 MHz beat}}$

APPLICATION INFORMATION



TELEVISION SIGNAL PROCESSING CIRCUIT

The TDA2680 is a silicon monolithic integrated signal processing circuit for mono-chrome and colour television receivers.

It combines the following functions:

- video pre-amplifier with emitter-follower output and short-circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator with sliding bias.
- automatic horizontal phase detector.
- vertical sync pulse separator.

The control stages in the i.f. amplifier and the tuner have to be equipped with n-p-n transistors. The equivalent circuit for tuners equipped with a p-n-p transistor is the TDA2690.

The circuit is intended for signals with negative modulation.

QUICK REFERENCE DATA

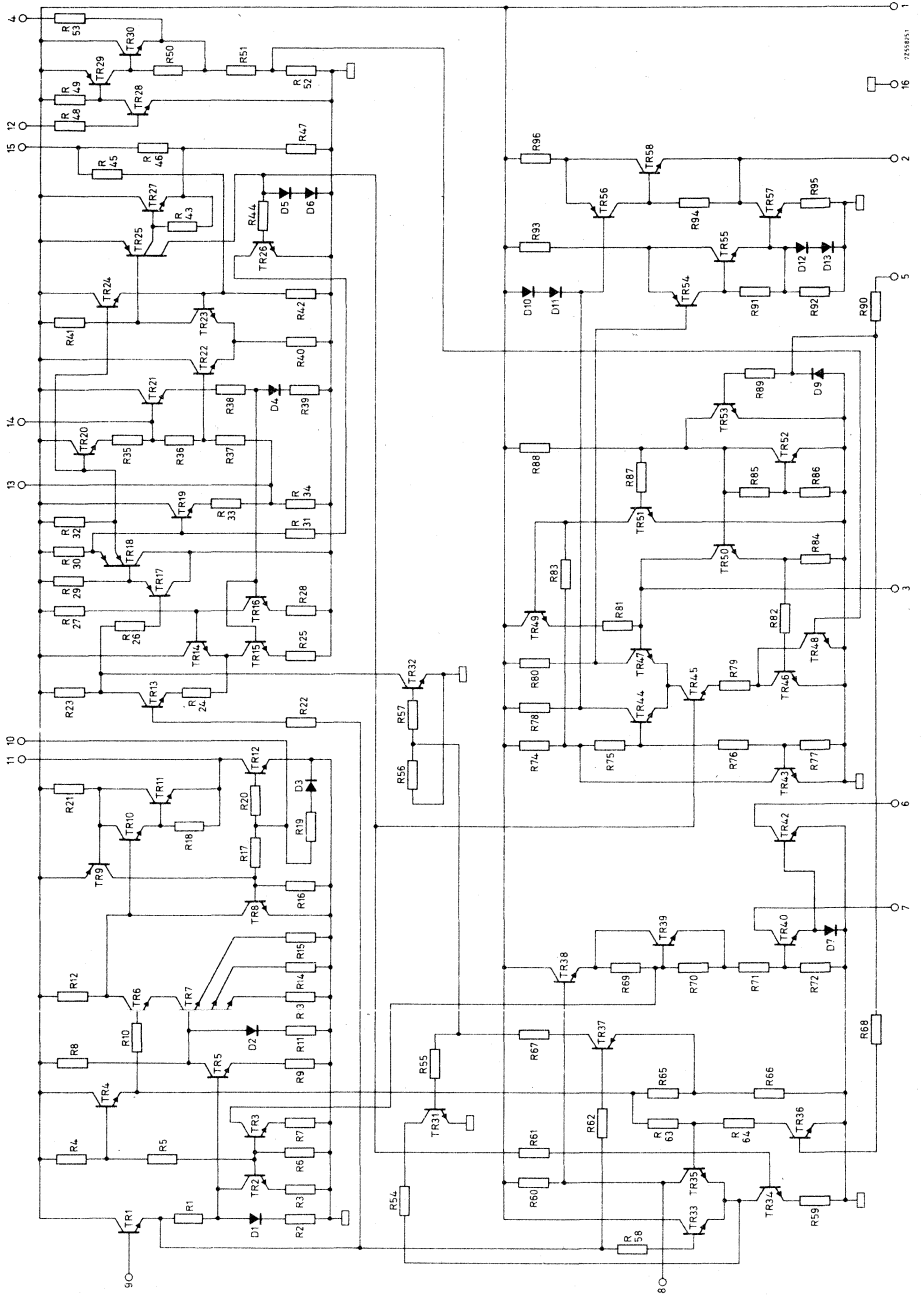
Supply voltage	V_{1-16}	typ.	12 V
Ambient temperature	T_{amb}	typ.	25 °C

Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7 V
Voltage gain of the video amplifier	G_v	typ.	7 dB
A.G.C. voltage for i.f. part	V_{7-16}		1,0 to 12 V
A.G.C. voltage for tuner	V_{6-16}		0,3 to 12 V
Output voltage range horizontal phase detector	V_{2-16}		±4 V
Vertical sync output voltage (positive going pulse: peak-to-peak value)	$V_{4-16(p-p)}$	typ.	11 V

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

TDA2680



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{1-16} max. 14 V

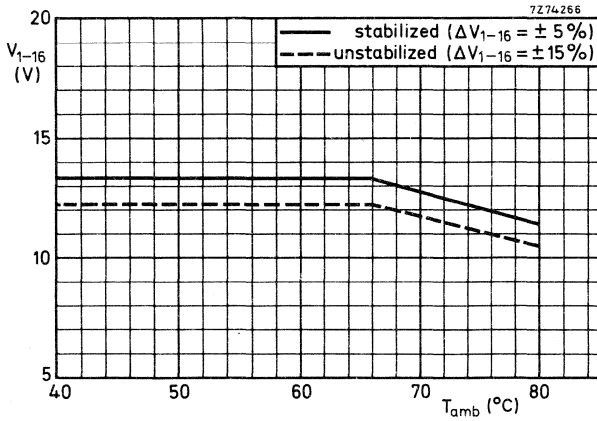
Power dissipation

Total power dissipation P_{tot} max. 980 mW

Temperatures

Storage temperature T_{stg} -25 to +125 °C

Operating ambient temperature T_{amb} -25 to +80 °C



Maximum permissible nominal supply voltage as a function of the maximum ambient temperature.

CHARACTERISTICS

Supply voltage range V_{1-16} See curves on page 3

The following characteristics are measured in the circuit on p. 7 at $T_{amb} = 25\text{ }^{\circ}\text{C}$;
 $V_{1-16} = 12\text{ V}$.

Video amplifier

Input resistance	R_{9-16}	>	30	$k\Omega$
Input capacitance	C_{9-16}	<	3	μF
Bandwidth (3 dB)	B	>	5	MHz
Linearity	m	>	0,9	
Rise time and fall time at the output	t_r, t_f	<	50	ns
Voltage gain	G_V	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7	V 1)
D.C. bias video detector voltage	V_{bias}	typ.	6	V 2)
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	V 1)
Black level at the output	V_{11-16}	typ.	5	V 3)
Available video output current (peak value)	I_{11M}	\leq	30	mA 4)

Tolerances on the video output voltages

IC processing spreads	$\pm\Delta V_{11-16}$	<	420	mV 5)
Temperature drift	$-\Delta V_{11-16}$	typ.	1,8	mV/ $^{\circ}\text{C}$
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	100	mV 6)
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_{1-16}}$	typ.	0,5	

1) Signal with negative-going sync ; this value is obtained when the input signal meets the C.C.I.R. standard (90% modulation depth).

2) When the bias is obtained from a resistive divider, resistors with a tolerance of 5% are required.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15\text{ mA}$.

5) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure.

6) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output

IC processing spreads	$\pm\Delta V_{11-16}$	<	420 mV	1)
Temperature drift	$-\Delta V_{11-16}$	typ.	1,7 mV/°C	
Spreads over a. g. c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	130 mV	2)
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_{1-16}}$	typ.	0,4	

Video blanking

Input voltage (peak-to-peak value)	$V_{10-16(p-p)}$		1 to 5 V	
Input resistance	R_{10-16}	typ.	1 k Ω	
Output voltage during blanking	V_{11-16}	<	500 mV	

A. G. C. circuit

Range of control voltage i. f. amplifier	V_{7-16}		1 to 12 V	3)
Range of control voltage tuner	V_{6-16}		0,3 to 12 V	3)
Signal expansion for full control of i. f. amplifier and tuner		typ.	0,5 dB	
Current i. f. control point	I_7	<	20 mA	
Current tuner control point	I_6	<	20 mA	
Current i. f. control point for tuner take-over	I_7		see note 4	
Keying input pulse (peak-to-peak value)	$V_{5-16(p-p)}$		see note 5	
Input resistance	R_{5-16}	typ.	2 k Ω	

1) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure.

2) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) This value depends on the ratio between the external impedances on pins 6 and 7. With equal impedances the current of the i. f. control point at tuner take-over will be about 16% from its maximum value (minimum control voltage).

5) Negative-going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit

Sync separator		see note 1		
Output voltage range of phase detector	V_{2-16}	± 4	V	2)
Control steepness	S_{φ}	typ. 2,5	$V/\mu s^3$	4)
Phase deviation between front edge sync pulse and front edge flyback pulse	φ_0	typ. 1,5	μs	4)
Variation φ_0 caused by internal spreads	$\pm \Delta \varphi_0$	typ. 0,5	μs	5)
Output voltage range as a frequency detector	V_{2-16}	± 2	V	6)

Vertical synchronization circuit

Output voltage vertical sync pulse generator	V_{4-16}	typ.	11	V
Output impedance	R_{4-16}	typ.	2	$k\Omega$
Output current	I_4	<	50	mA

1) The sync pulse is sliced about half way between top sync and black level. A sliding bias circuit makes the slicing level largely independent of the signal strength and sync pulse compression.

2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example $R_S = 56 \Omega$, $S_{\varphi} = 5 V/\mu s$ and $R_S = 0$, $S_{\varphi} \approx 25 V/\mu s$.

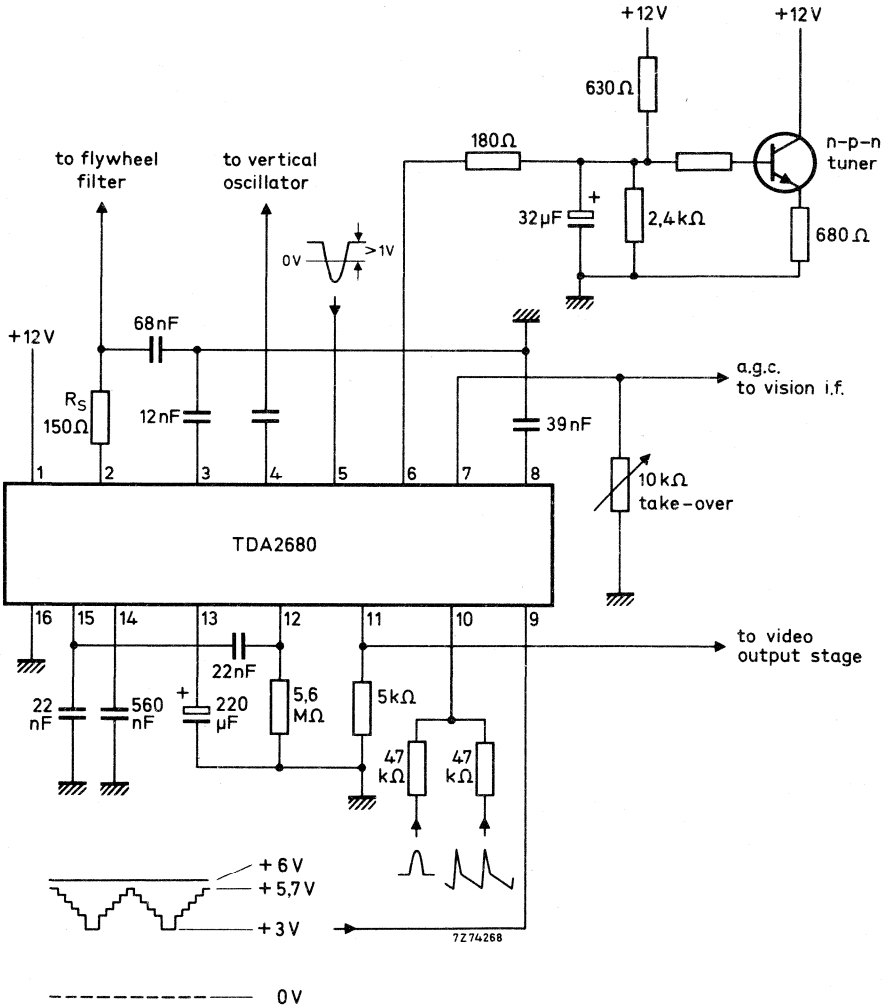
4) Measured in the circuit on page 7.

5) In addition to this figure $\pm 7\%$ of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0 .
This value of $\pm 7\%$ is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed $\pm 10\%$.

6) Nominal voltage 6 V.

The load impedance on pin 2 of the circuit on page 7 is about $50 k\Omega$.

APPLICATION INFORMATION



TELEVISION SIGNAL PROCESSING CIRCUIT

The TDA2690 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.

It combines the following functions:

- video pre-amplifier with emitter-follower output and short-circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator with sliding bias.
- automatic horizontal phase detector.
- vertical sync pulse separator.

The control stage in the i.f. amplifier has to be equipped with an n-p-n transistor and the tuner with a p-n-p transistor. The equivalent circuit for tuners equipped with an n-p-n transistor is the TDA2680.

The circuit is intended for signals with negative modulation.

QUICK REFERENCE DATA

Supply voltage	V_{1-16}	typ.	12	V
Ambient temperature	T_{amb}	typ.	25	°C

Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7	V
Voltage gain of the video amplifier	G_V	typ.	7	dB
A.G.C. voltage for i.f. part	V_{7-16}		1,0 to 12	V
A.G.C. voltage for tuner	V_{6-16}		0,3 to 12	V
Output voltage range horizontal phase detector	V_{2-16}		± 4	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{4-16(p-p)}$	typ.	11	V

PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{1-16} max. 14 V

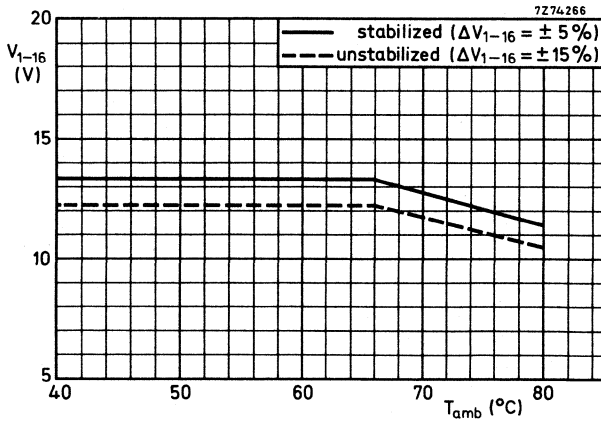
Power dissipation

Total power dissipation P_{tot} max. 980 mW

Temperatures

Storage temperature T_{stg} -25 to +125 °C

Operating ambient temperature T_{amb} -25 to +80 °C



Maximum permissible nominal supply voltage as a function of the maximum ambient temperature.

CHARACTERISTICS

Supply voltage range

V_{1-16}

See curves on page 3

The following characteristics are measured in the circuit on p. 7 at $T_{amb} = 25^{\circ}C$;
 $V_{1-16} = 12 V$.

Video amplifier

Input resistance	R_{9-16}	>	30	$k\Omega$
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity	m	>	0,9	
Rise time and fall time at the output	$t_r; t_f$	<	50	ns
Voltage gain	G_v	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2,7	V 1)
D. C. bias video detector voltage	V_{bias}	typ.	6	V 2)
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	V 1)
Black level at the output	V_{11-16}	typ.	5	V 3)
Available video output current (peak value)	I_{11M}	\leq	30	mA 4)

Tolerances on the video output voltages

IC processing spreads	$\pm \Delta V_{11-16}$	<	420	mV 5)
Temperature drift	$-\Delta V_{11-16}$	typ.	1,8	mV/ $^{\circ}C$
Spreads over a. g. c. expansion (entire range)	$\pm \Delta V_{11-16}$	<	100	mV 6)
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_{1-16}}$	typ.	0,5	

- 1) Signal with negative-going sync ; this value is obtained when the input signal meets the C. C. I. R. standard (90% modulation depth).
- 2) When the bias is obtained from a resistive divider, resistors with a tolerance of 5% are required.
- 3) Only valid if the video signal is in accordance with the C. C. I. R. standard.
- 4) The total load on pin 11 must be such that the d. c. output current $I_{11} \leq 15 mA$.
- 5) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure.
- 6) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)Tolerances on the black level at the output

IC processing spreads	$\pm \Delta V_{11-16}$	<	420	mV	1)
Temperature drift	$-\Delta V_{11-16}$	typ.	1,7	mV/°C	
Spreads over a.g.c. expansion (entire range)	$\pm \Delta V_{11-16}$	<	130	mV	2)
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_{1-16}}$	typ.	0,4		

Video blanking

Input voltage (peak-to-peak value)	$V_{10-16(p-p)}$		1 to 5	V	
Input resistance	R_{10-16}	typ.	1	k Ω	
Output voltage during blanking	V_{11-16}	<	500	mV	

A. G. C. circuit

Range of control voltage i. f. amplifier	V_{7-16}		1 to 12	V	3)
Range of control voltage tuner	V_{6-16}		0,3 to 12	V	4)
Signal expansion for full control of i. f. amplifier and tuner		typ.	0,5	dB	
Current i. f. control point	I_7	<	20	mA	
Current tuner control point	I_6	<	8	mA	
Current i. f. control point for tuner take-over	I_7	typ.	2	mA	
Keying input pulse (peak-to-peak value)	$V_{5-16(p-p)}$		see note 5		
Input resistance	R_{5-16}	typ.	2	k Ω	

1) The spreads of the voltage divider for the bias of the video detector of $\pm 5\%$ is included in this figure.

2) Variation about a nominal condition, the i. f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) Negative going at increasing input signal.

5) Negative-going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit

Sync separator		see note 1		
Output voltage range of phase detector	V_{2-16}	± 4	V	2)
Control steepness	S_{φ}	typ. 2,5	$V/\mu s$	3)4)
Phase deviation between front edge sync pulse and front edge flyback pulse	φ_0	typ. 1,5	μs	4)
Variation φ_0 caused by internal spreads	$\pm \Delta \varphi_0$	typ. 0,5	μs	5)
Output voltage range as a frequency detector	V_{2-16}	± 2	V	6)

Vertical synchronization circuit

Output voltage vertical sync pulse generator	V_{4-16}	typ. 11	V	
Output impedance	R_{4-16}	typ. 2	k Ω	
Output current	I_4	< 50	mA	

1) The sync pulse is sliced about half way between top sync and black level. A sliding bias circuit makes the slicing level largely independent of the signal strength and sync pulse compression.

2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example $R_S = 56 \Omega$, $S_{\varphi} = 5 V/\mu s$ and $R_S = 0$, $S_{\varphi} = \geq 25 V/\mu s$.

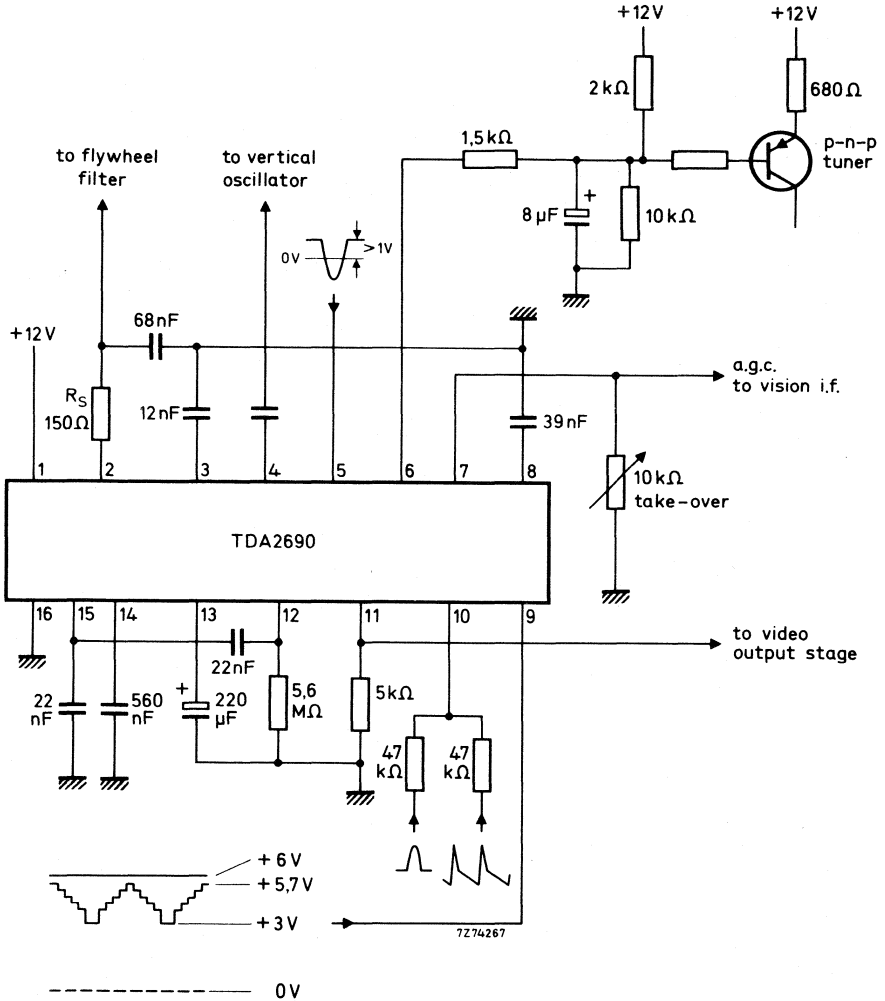
4) Measured in the circuit on page 7.

5) In addition to this figure $\pm 7\%$ of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0 . This value of $\pm 7\%$ is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed $\pm 10\%$.

6) Nominal voltage 6 V.

The load impedance on pin 2 of the circuit on page 7 is about 50 k Ω .

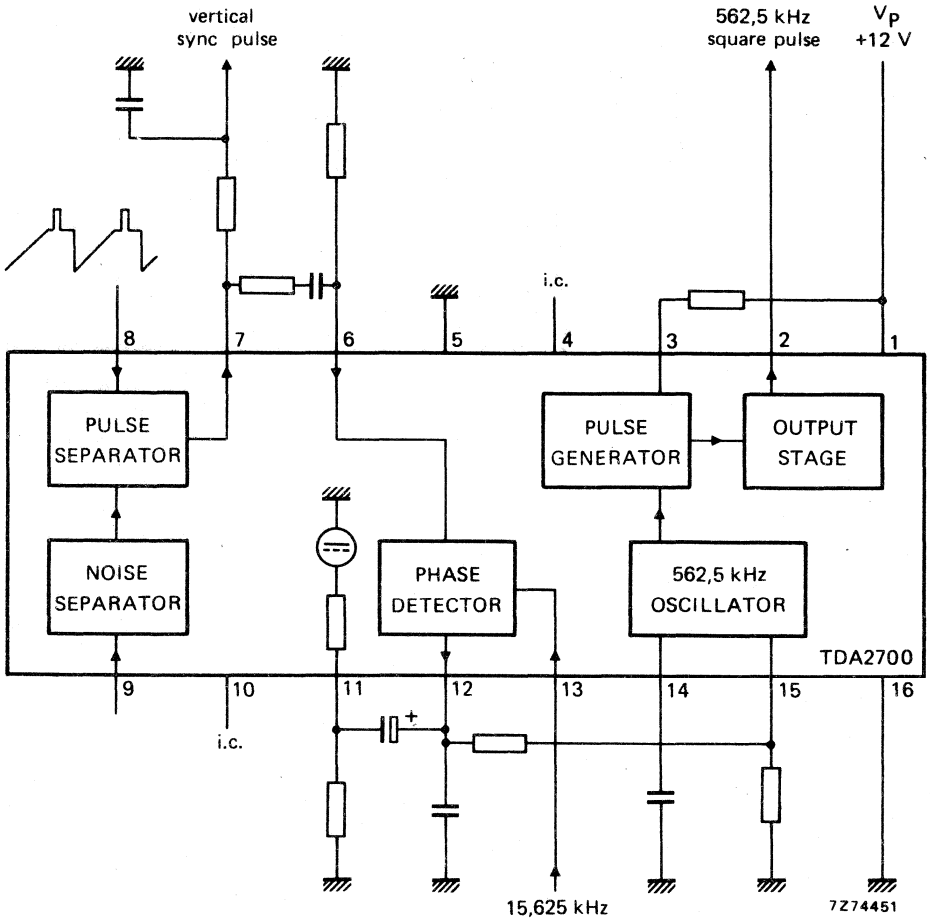
APPLICATION INFORMATION



OSCILLATOR FOR VIDEO RECORDERS

The TDA2700 is a monolithic integrated circuit for video recorders incorporating the following functions :

- 562,5 kHz oscillator
- pulse separator
- noise separator
- phase detector
- pulse generator
- low-ohmic output stage



PACKAGE OUTLINE 16-lead DIL; plastic (see general section).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage	V_{1-16}	max.	13,2	V
Pin 3	V_{3-16}		0 to V_{1-16}	V
Pin 8	$-V_{8-16}$	max.	12	V

Currents

Pin 2 (average value)	$-I_{2(AV)}$	max.	20	mA
(peak value)	$-I_{2M}$	max.	200	mA
Pin 6 (peak value)	$\pm I_{6M}$	max.	10	mA
Pin 7 (peak value)	$-I_{7M}$	max.	10	mA
Pin 8 (peak value)	I_{8M}	max.	10	mA
Pin 9 (peak value)	$\pm I_{9M}$	max.	10	mA

Power dissipation

Total power dissipation	P_{tot}	max.	600	mW
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Temperatures

Storage temperature	T_{stg}		-25 to +125	°C
Operating ambient temperature	T_{amb}		-20 to +60	°C

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C; measured in circuit on page 4

Inputs

Supply

Supply current at $I_2 = 0$	I_1	typ.	36	mA
-----------------------------	-------	------	----	----

Sync pulse separator

Negative video input signal (peak-to-peak value)	$V_{8-16(p-p)}$	typ.	3	V
			1 to 7	V
Input current (peak value)	I_{8M}	\geq	10	μ A
Input leakage current at $V_{8-16} = -3$ V	$-I_8$	\leq	1	μ A

Noise separator

Input voltage	V_{9-16}	typ.	0,7	V
Input current range	I_9		0,03 to 10	μ A
Input resistance	R_{9-16}	typ.	200	Ω

CHARACTERISTICS (continued)**Outputs**Sync pulse separator

Output voltage (peak-to-peak value)	V _{7-16(p-p)}	typ.	10 V
Output resistance: at leading edge of sync pulse at trailing edge of sync pulse	R ₇₋₁₆	typ.	50 Ω ¹⁾
	R ₇₋₁₆	typ.	2,2 kΩ
Additional external load resistance	R _{7-16(ext)}	≥	2 kΩ

Output stage

Output voltage (peak-to-peak value)	V _{2-16(p-p)}	typ.	10 V
Output resistance	R ₂₋₁₆	low-ohmic	
Duty factor of output pulse	δ	typ.	50 %

Phase detector

Input voltage	V ₆₋₁₆	typ.	1,5 V
Input current range	I ₆	0,03 to 3 mA	
Control voltage range	V ₁₂₋₁₆	1,3 to 5,5 V	
Output resistance in the control voltage range	R ₁₂₋₁₆	high-ohmic ²⁾	
Control current	±I ₁₂	typ.	7,5 mA
Input voltage range for I ₁₂ positive for I ₁₂ negative	V ₁₃₋₁₆	7,2 to 9 V	
	V ₁₃₋₁₆	0 to 5,5 V	
Input current at V ₁₃₋₁₆ ≥ 7,2 V at V ₁₃₋₁₆ ≤ 5,5 V	I ₁₃	<	6 μA
	I ₁₃	<	1 μA
Catching and holding range (based on 15,625 kHz)	Δf	typ.	±1 kHz ³⁾
D.C. level at pin 11	V ₁₁₋₁₆	typ.	3,1 V
Internal resistance at pin 11	R ₁₁₋₁₆	typ.	2 kΩ

Oscillator

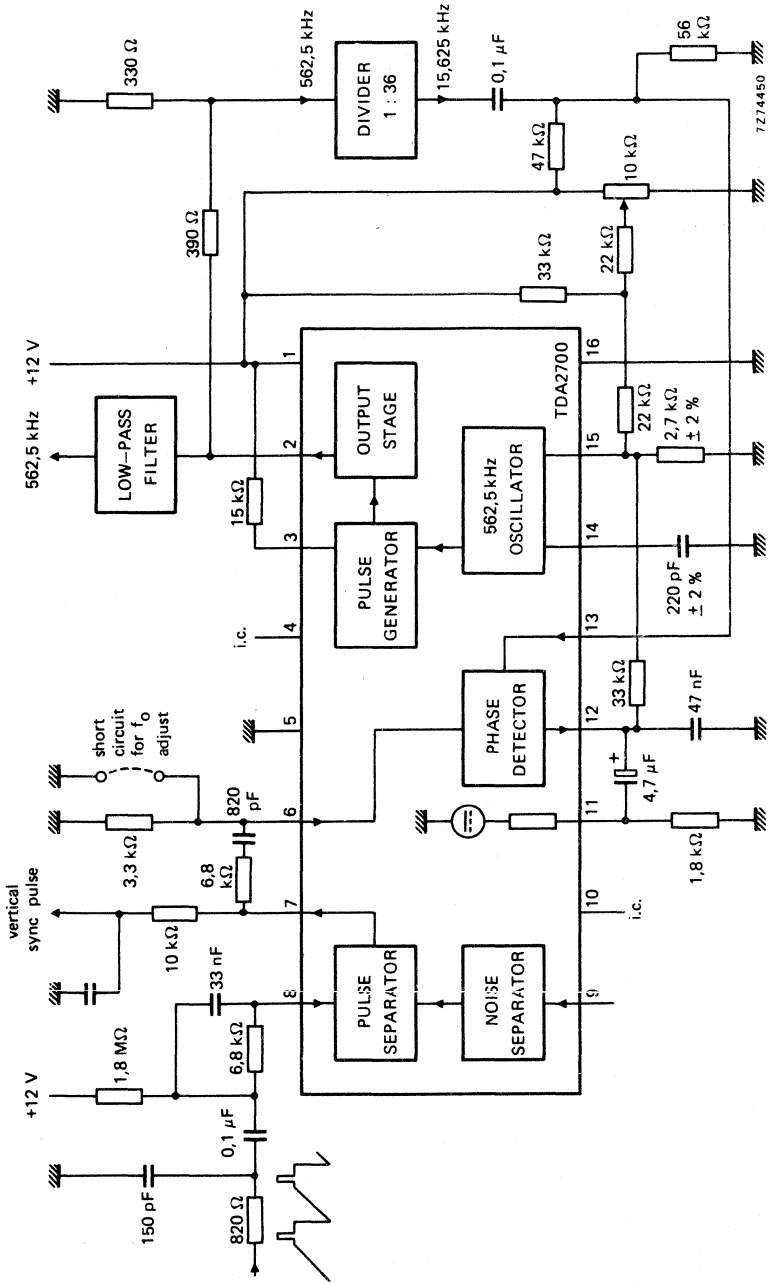
Output voltage (peak-to-peak value)	V _{14-16(p-p)}	typ.	3 V
Charge and discharge current	I ₁₄ = ±I ₁₅	typ.	0,94 mA
Voltage at pin 15	V ₁₅₋₁₆	typ.	3,1 V
Frequency; free running	f ₀	typ.	562,5 kHz
Frequency adjustment range	Δf ₀ /f ₀	typ.	10 %

1) Emitter follower.

2) Current source.

3) Adjustable with R_{12-15(ext)}.

APPLICATION INFORMATION

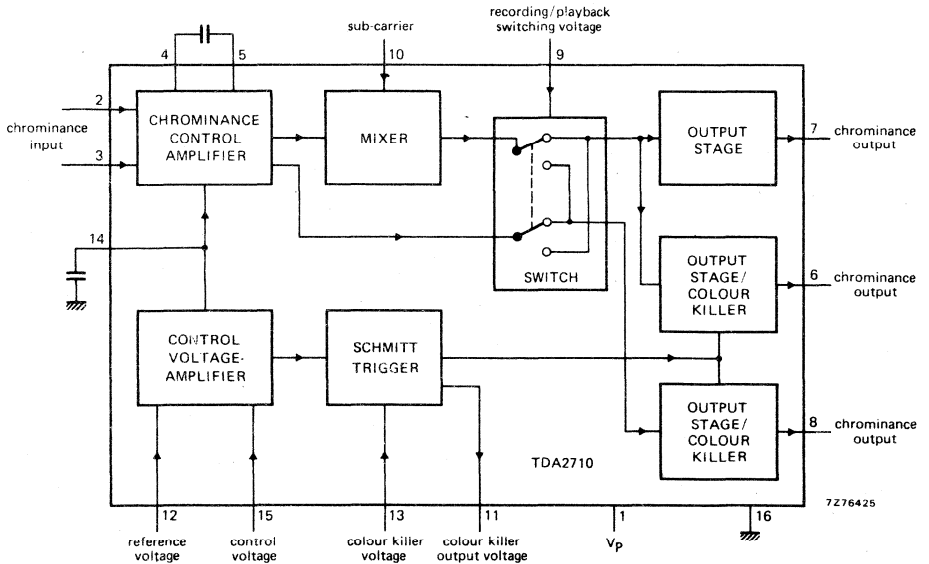


CHROMINANCE SIGNAL/MIXER FOR VIDEO RECORDERS

The TDA2710 is a monolithic integrated circuit for video recorders incorporating the following functions :

- controlled chrominance amplifier
- control voltage amplifier
- mixer for the chrominance signal
- electronic recording/playback switch
- Schmitt trigger for killing the chrominance signal
- colour killer output stage

BLOCK DIAGRAM



PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (pin 1)	$V_P (V_{1-16})$	0 to 13,2	V
At pin 4	V_{4-16}	0 to V_P	V
At pin 5	V_{5-16}	0 to V_P	V
At pin 12	V_{12-16}	0 to V_P	V
At pin 13	V_{13-16}	0 to V_P	V
At pin 15	V_{15-16}	0 to V_P	V
At pin 9	$\pm V_{9-16}$	max. 4	V

Currents

At pin 6	$-I_6$	max. 5	mA
At pin 7	$-I_7$	max. 5	mA
At pin 8	$-I_8$	max. 5	mA
At pin 11	I_{11}	max. 5	mA

Power dissipation

Total power dissipation	P_{tot}	max. 700	mW
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Temperatures

Storage temperature	T_{stg}	-25 to +125	°C
Operating ambient temperature	T_{amb}	-20 to +60	°C

CHARACTERISTICS at $V_P = 12$ V; $T_{amb} = 25$ °C; measured in circuit on page 4

Inputs

Chrominance input (pins 2 and 3)

Input resistance	$R_{2;3-16}$	typ. 3,3	k Ω
D.C. input voltage (without signal)	$V_{2;3-16}$	typ. 5,9	V
Input voltage range at a peak-to-peak burst of 0,5 V	$V_{2;3-16}$	2,5 to 75	mV

Sub-carrier (pin 10)

Input resistance	R_{10-16}	typ. 2	k Ω
D.C. input voltage (without signal)	V_{10-16}	typ. 4,4	V
Input voltage range (peak-to-peak value)	$V_{10-16(p-p)}$	60 to 500	mV

CHARACTERISTICS (continued)

Reference voltage (pin 12)

External reference voltage	V ₁₂₋₁₆	typ.	7 V
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Control voltage (pin 15)

Voltage at control voltage input

for colour on

V ₁₅₋₁₆	≤	5,7 V
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for colour off

V ₁₅₋₁₆	≥	6,1 V
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Colour killer input (pin 13)

Input voltage for colour off

V ₁₃₋₁₆	≥	6 V
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Recording/playback switch (pin 9)

Input resistance

R ₉₋₁₆	typ.	1 kΩ
-------------------	------	------

Input voltage : for recording

V ₉₋₁₆	≤	0,3 V
-------------------	---	-------

for playback

V ₉₋₁₆	≥	0,85 V
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OutputsColour killer output (pin 11)

Output resistance for colour on

R ₁₁₋₁	typ.	10 kΩ
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Output voltage for colour off

V ₁₁₋₁₆	≤	0,5 V
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Recording

Output voltages (peak-to-peak values)

at a peak-to-peak burst of 0,5 V

V _{6;7-16(p-p)}	typ.	0,5 V
--------------------------	------	-------

Output voltage at pin 8 (peak-to-peak value)

at V_{6-16(p-p)} = 0,5 V

V _{8-16(p-p)}	0,35 to 0,5 V
------------------------	---------------

Playback

Sub-carrier suppression at pins 6 and 7

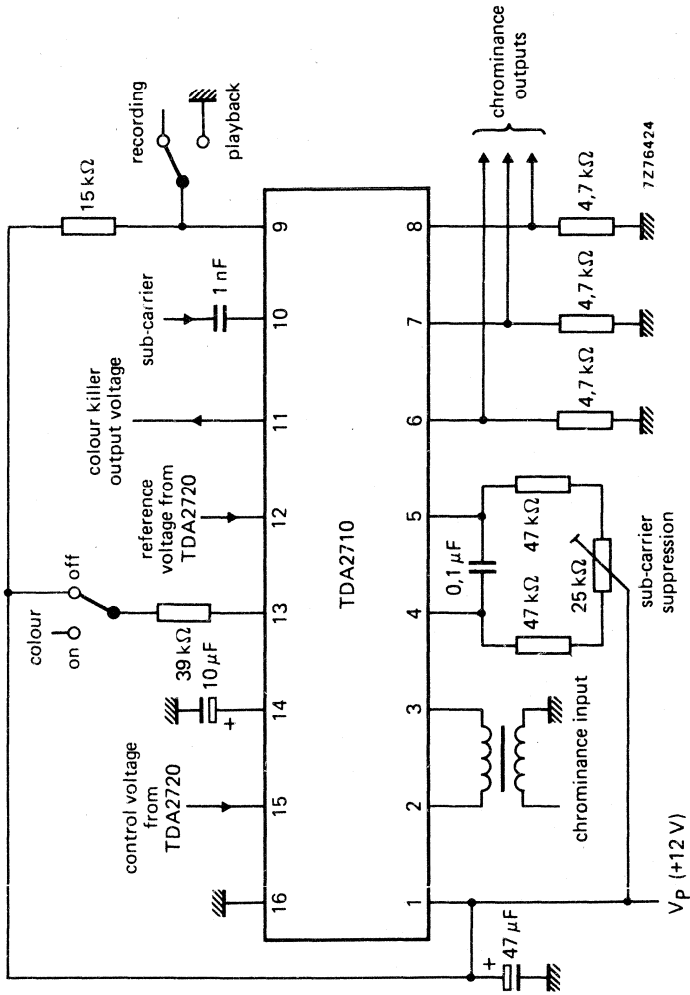
at V_{10-16(p-p)} = 300 mV; V_{6-16(p-p)} =V_{7-16(p-p)} = 1 V; sub-carrier suppression

at pins 4 and 5

≥	60 dB
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APPLICATION INFORMATION



DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not form part of our data handbook system and does not necessarily imply that the device will go into production

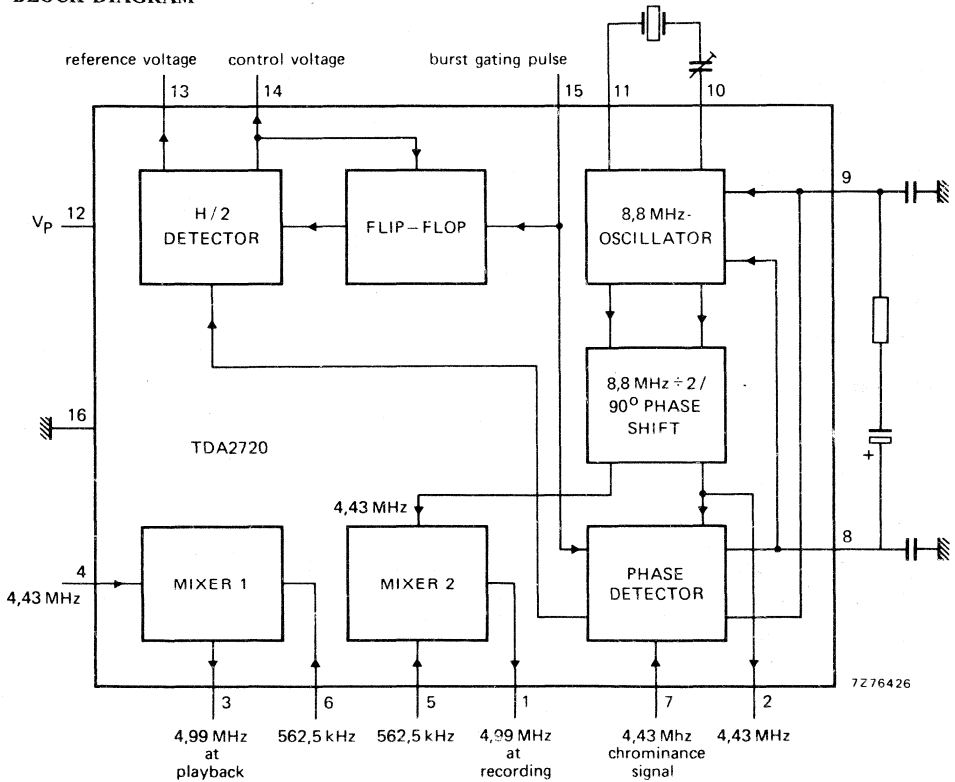
TDA2720

COLOUR SUB-CARRIER OSCILLATOR FOR VIDEO RECORDERS

The TDA2720 is a monolithic integrated circuit for video recorders incorporating the following functions :

- 8,8 MHz colour sub-carrier oscillator with divider stage
- keyed phase comparison for optimum noise behaviour
- a stage to obtain automatic chrominance control
- a stage to obtain a colour killer signal and an identification signal
- 2 mixer stages to obtain the 4,99 MHz sub-carrier frequency

BLOCK DIAGRAM



PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

TDA2720

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (pin 12)	V_P (V ₁₂₋₁₆)	max.	13,2	V
At pin 1	V_{1-16}		0 to V_P	V
At pin 2	V_{2-16}	min.	0	V
At pin 3	V_{3-16}		0 to V_P	V
At pins 5, 6, 7 and 11	$V_{5;6;7;11-16}$	min.	0	V
At pin 13	V_{13-16}		0 to V_P	V
At pin 14	V_{14-16}		0 to V_P	V
At pin 15	V_{15-16}		0 to V_P	V

Currents

At pins 2, 5 and 6	$I_{2;5;6}$	max.	5	mA
At pins 7, 11 and 13	$I_{7;11;13}$	max.	5	mA
At pin 10	$-I_{10}$	max.	2	mA

Power dissipation

Total power dissipation	P_{tot}	max.	750	mW
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Temperatures

Storage temperature	T_{stg}	-25 to +125	°C
Operating ambient temperature	T_{amb}	-20 to +60	°C

CHARACTERISTICS at $V_P = 12$ V; $T_{amb} = 25$ °C

<u>Supply current</u> (pin 12)	I_{12}	typ.	40	mA
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8, 8 MHz oscillator

Input resistance	R_{11-16}	typ.	270	Ω
Output resistance	R_{10-16}	typ.	200	Ω
Overall holding range	Δ_f	typ.	±500	Hz
Oscillator output voltage	V_{10-16}	typ.	10	V

CHARACTERISTICS (continued)

Reference voltage part

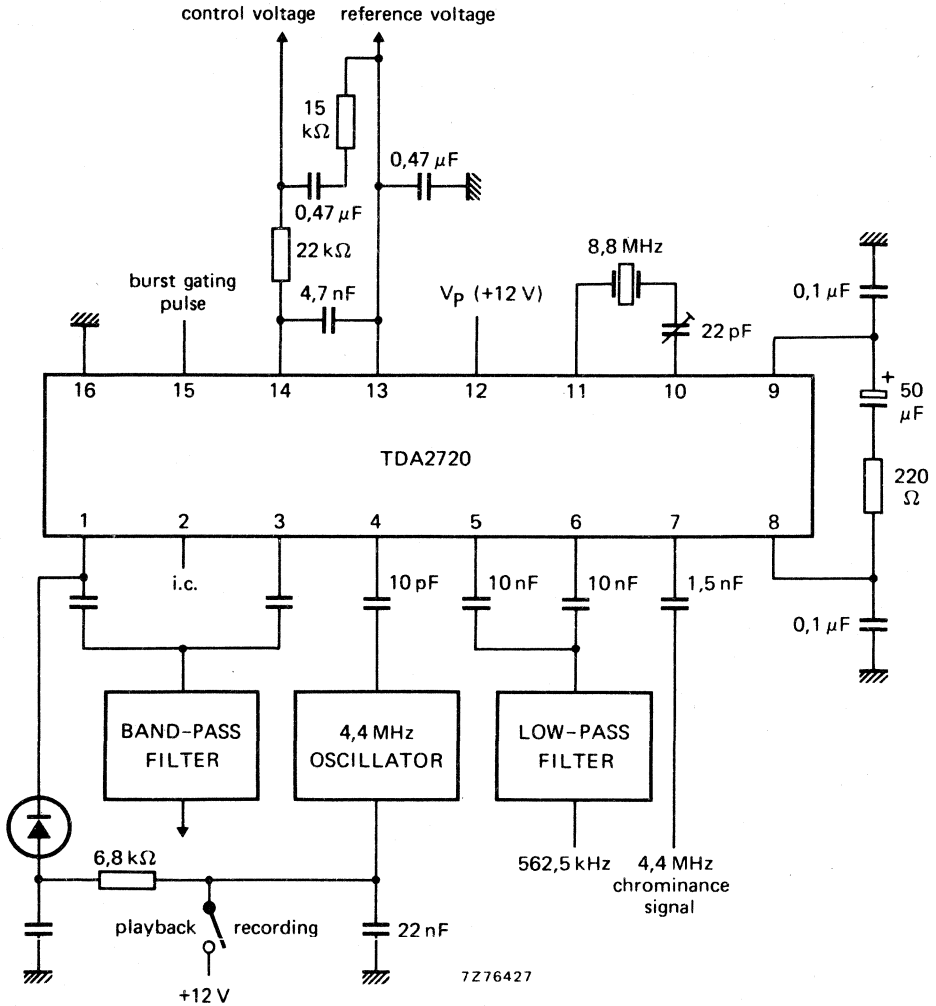
Burst signal (peak-to-peak value)	$V_{7-16(p-p)}$	typ.	0,5 V
Linear output voltage range (peak-to-peak value)	$V_{7-16(p-p)}$	\leq	1,5 V
D. C. voltage at pin 14 with a peak-to-peak burst of 0,5 V	V_{14-16}	typ.	5,5 V
without burst	V_{14-16}	typ.	7,0 V
Reference voltage	V_{13-16}	typ.	7,0 V
Burst keying pulse	V_{15-16}	\geq	2,0 V
Voltage at pin 2; 4, 4 MHz (peak-to-peak value)	$V_{2-16(p-p)}$	typ.	0,5 V

Mixer

Carrier suppression at 1 V peak-to-peak; 4,99 MHz ¹⁾			
Recording mixer		\geq	20 dB
Playback mixer		\geq	20 dB
Gain for both mixers	G	typ.	7
Gain variation	ΔG	\leq	3 dB
Gain difference of mixers	ΔG	\leq	3 dB
Linear output voltage range (peak-to-peak value) pin 5	$V_{5-16(p-p)}$	\leq	0,6 V
pin 6	$V_{6-16(p-p)}$	\leq	0,6 V
Voltage at pin 4; 4, 4 MHz (peak-to-peak value)	$V_{4-16(p-p)}$	typ.	0,4 V
D. C. voltage at pin 4	V_{4-16}	typ.	5,0 V
at pin 5	V_{5-16}	typ.	3,5 V
at pin 6	V_{6-16}	typ.	3,5 V

¹⁾ Pin 4 connected to pin 2 via a 1 nF capacitor.

APPLICATION INFORMATION



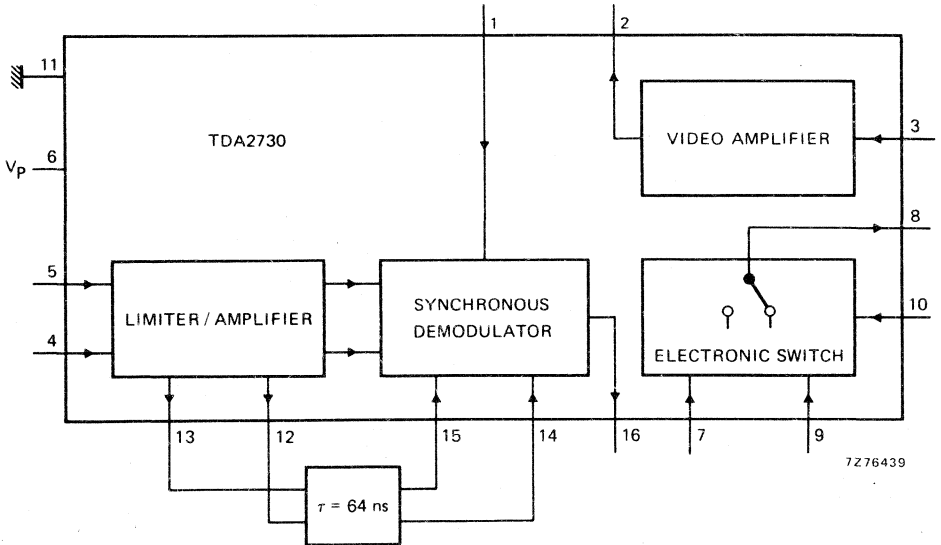
FM LIMITER/DEMODULATOR

The TDA2730 is a monolithic integrated circuit for use in audio-visual equipment, e. g. ; video recorders and video disc players.

The circuit comprises an f. m. limiter/demodulator for the playback signal, a video amplifier and an electronic switch, which can be used for drop-out elimination.

QUICK REFERENCE DATA			
Supply voltage	V ₆₋₁₁	typ.	12 V
Supply current	I ₆	typ.	42 mA
Input signal range (peak-to-peak value)	V _{4-5(p-p)}		30 to 2000 mV
Video output signal (peak-to-peak value)	V _{2-11(p-p)}	typ.	4 V

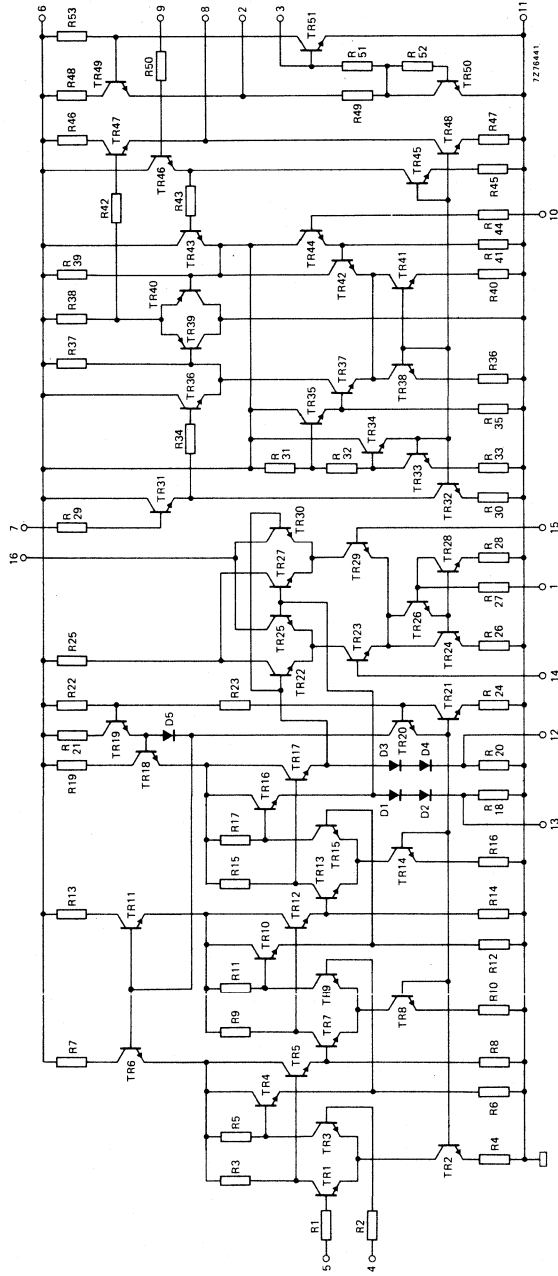
BLOCK DIAGRAM



PACKAGE OUTLINE (see general section)

16-lead DIL; plastic.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V_{6-11} max. 13 V

Power dissipation

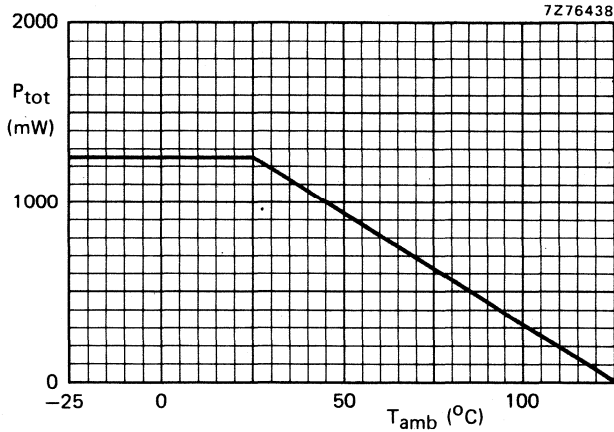
Total power dissipation
(see also derating curve below) P_{tot} max. 1.25 W

Temperatures

Storage temperature T_{stg} -65 to +125 °C

Operating ambient temperature see derating curve below

DEVELOPMENT SAMPLE DATA



CHARACTERISTICS measured in the circuit on page 7 (Fig. 1)

<u>Supply voltage range</u>	V_{6-11}	typ. 12 V 11 to 13 V
-----------------------------	------------	-------------------------

The following characteristics are measured at $V_{6-11} = 12$ V; $T_{amb} = 25$ °C

<u>Supply current</u>	I_6	typ. 42 mA 25 to 54 mA
-----------------------	-------	---------------------------

Limiters

Start of limiting (-3 dB) $f_0 = 4$ MHz; peak-to-peak value	$V_{4-5(p-p)}$	typ. 0,8 V
Input signal range for constant luminance output (peak-to-peak value)	$V_{4-5(p-p)}$	30 to 2000 mV
Output voltage (peak-to-peak value)	$V_{12-13(p-p)}$	typ. 750 mV
Available output voltage at an external load of 1 k Ω ; peak-to-peak value	$V_{12-13(p-p)}$	> 5 V

Demodulator

Measured at $I_1 = 4$ mA; $|Z_{16-11}| = 1,5$ k Ω ; delay time $\tau = 64$ ns; $\Delta f = 1,4$ MHz
($f_L = 3,0$ MHz, $f_H = 4,4$ MHz)

Current ratio	I_1/I_{16}	typ. 1
Output voltage (peak-to-peak value)	V_{16-11}	typ. 540 mV

Drop-out switch

Input drive voltage range	$V_{7;9-11}$	6,5 to 12 V
Voltage drop between input and output for signal flow from pin 7 to pin 8	V_{7-8}	typ. 1,5 V
for signal flow from pin 9 to pin 8	V_{9-8}	typ. 1,5 V
Input offset voltage	$ V_{7-8} - V_{9-8} $	< 20 mV
Switch actuating input voltage for signal flow from pin 7 to pin 8	V_{10-11}	0 to 2,7 V
for signal flow from pin 9 to pin 8	V_{10-11}	3,7 to 6,0 V
Output impedance at 1,5 mA by internal load	Z_{8-11}	emitter follower

CHARACTERISTICS (continued)**Video amplifier**

Input voltage level	V_{3-11}	typ.	730	mV
Output voltage level	V_{2-11}	typ.	5,5	V
Open loop gain	G	typ.	43	dB
Bandwidth (3 dB)	B	typ.	8,8	MHz
Output voltage (peak-to-peak value; see note)	$V_{2-11(p-p)}$	typ.	4	V

Note

The gain of the amplifier is determined by the feedback network comprising the impedances between pins 2 and 3, and pins 8 and 3. The values quoted apply to the circuit on page 7 (Fig. 1).

PINNING

- | | |
|--------------------------------|------------------------------|
| 1. Current setting demodulator | 9. Switch input |
| 2. Video amplifier output | 10. Switch actuating input |
| 3. Video amplifier input | 11. Negative supply (ground) |
| 4. F.M. signal input | 12. Limiter output |
| 5. F.M. signal input | 13. Limiter output |
| 6. Positive supply | 14. Demodulator input |
| 7. Switch input | 15. Demodulator input |
| 8. Switch output | 16. Demodulator output |

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Current setting of demodulator

The current into this pin directly **determines** the amplitude and the d. c. level of the demodulator output. At $I_1 = 4$ mA, optimum temperature compensation is obtained.

2. Video amplifier output

A signal up to 4 V peak-to-peak is available from this output (Fig. 1).

This can be the video signal (Fig. 1) or the f. m. signal to the delay line (drop-out elimination; Fig. 2).

3. Video amplifier input

The demodulator output signal is the input signal to this pin (Fig. 1) or the f. m. modulated signal (Fig. 2).

4. F. M. signal input (in conjunction with pin 5)

A frequency modulated signal of 1 V peak-to-peak is applied between pins 4 and 5. D. C. feedback from the limiter output is applied to stabilize the operation.

5. F. M. signal input

See pin 4.



APPLICATION INFORMATION (continued)6. Positive supply

Correct operation can be obtained in the range 11 to 13 V.

7. Switch input

The signal applied to pin 7 or to pin 9 is transferred to pin 8, depending on the switch position. For an input level between 0 and 2,7 V at pin 10, the signal at pin 7 is transferred to pin 8, and when between 3,7 and 6 V the input signal at pin 9 is transferred to pin 8.

The signal at pin 7 or pin 9 may vary from 6,5 to 12 V.

The signal at pin 8 is 1,5 V below the value at pin 7 or 9.

The difference in input level at pins 7 and 9, to obtain equal output at pin 8, will be less than 20 mV.

8. Switch output

See pin 7.

9. Switch input

See pin 7.

10. Switch actuating input

See pin 7.

11. Negative supply (ground)12. Limiter output

A balanced signal is available between pins 12 and 13. The signal amplitude is limited to 750 mV at both outputs.

13. Limiter output

See pin 12.

14. Demodulator input

A phase shifted signal (with respect to the internally applied signal) is applied between pins 14 and 15.

15. Demodulator input

See pin 14.

16. Demodulator output

The output signal is proportional to :

- current into pin 1
- slope of the phase characteristic of the network between pins 12 and 13, and pins 14 and 15
- impedance level at the output
- the sweep (Δf) of the f. m. signal.

A signal of typically 540 mV is available at this pin when using the component values in Fig. 1 and $\Delta f = 1,4$ MHz.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION (continued)

Test circuit

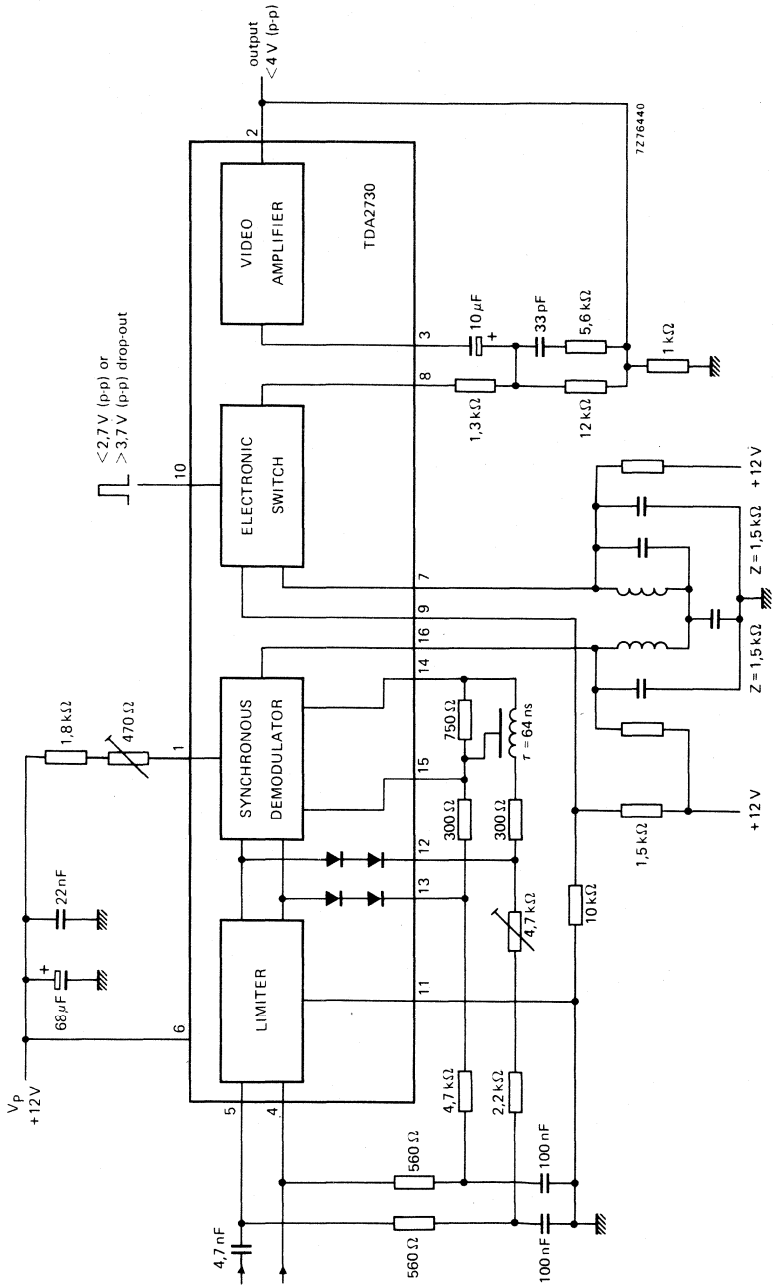


Fig. 1



INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

Type no.	Section	Type no.	Section	Type no.	Section	Type no.	Section
OM200/S2	RA	TBA900Q	TV	TDA1028	RA	TDA2610	TV
SAJ110	RA	TBA920	TV	TDA1029	RA	TDA2610A	TV
TAA263	RA	TBA920Q	TV	TDA2611	RA	TDA2620	TV
TAA320	RA	TBA920S	TV	TDA2611A	RA	TDA2620Q	TV
TAA320A	RA	TBA990	TV	TDA2500	TV	TDA2630	TV
TAA550	TV	TBA990Q	TV	TDA2500Q	TV	TDA2630Q	TV
TAA630S	TV	TCA270S	TV	TDA2510	TV	TDA2631	TV
TAA630T	TV	TCA270SQ	TV	TDA2510Q	TV	TDA2631Q	TV
TBA510	TV	TCA290A	RA	TDA2520	TV	TDA2640	TV
TBA510Q	TV	TCA420A	RA	TDA2520Q	TV	TDA2640Q	TV
TBA520	TV	TCA450A	RA	TDA2522	TV	TDA2670	TV
TBA520Q	TV	TCA530	RA	TDA2522Q	TV	TDA2680	TV
TBA530	TV	TCA540	TV	TDA2523	TV	TDA2690	TV
TBA530Q	TV	TCA540Q	TV	TDA2523Q	TV	TDA2700	TV
TBA540	TV	TCA640	TV	TDA2530	TV	TDA2710	TV
TBA540Q	TV	TCA650	TV	TDA2530Q	TV	TDA2720	TV
TBA550	TV	TCA660B	TV	TDA2540	TV	TDA2730	TV
TBA550Q	TV	TCA730	RA	TDA2540Q	TV		
TBA560C	TV	TCA740	RA	TDA2541	TV		
TBA570CQ	TV	TCA750	RA	TDA2541Q	TV		
TBA570A	RA	TCA760B	RA	TDA2560	TV		
TBA570AQ	RA	TCA800	TV	TDA2560Q	TV		
TBA700	RA	TCA820	TV	TDA2571	TV		
TBA720A	TV	TDA1002	RA	TDA2571Q	TV		
TBA720AQ	TV	TDA1003A	RA	TDA2581	TV		
TBA750A	TV	TDA1004A	RA	TDA2581Q	TV		
TBA750AQ	TV	TDA1005	RA	TDA2590	TV		
TBA890	TV	TDA1006	RA	TDA2590Q	TV		
TBA890Q	TV	TDA1009	RA	TDA2600	TV		
TBA900	TV	TDA1010	RA	TDA2600Q	TV		

RA = Radio - Audio

TV = Television

MAINTENANCE TYPE LIST

The type numbers listed below are not included in this handbook except for those marked with an asterisk.

Detailed information will be supplied on request.

- TAA310A
- TAA370A
- TBA500N; NQ
- TBA500P; PQ
- TCA160B (successor type : TCA760B)
- TCA160C
- TCA490
- * TBA550; Q

General

Radio - Audio

Television

Index and maintenance type list

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